A New Direction in Mixed-Signal

# XR1009, XR2009

## 0.2mA, 35MHz Rail-to-Rail Amplifiers

## General Description

The XR1009 (single) and XR2009 (dual) are ultra-low power, low cost, voltage feedback amplifiers. These amplifiers use only 208µA of supply current and are designed to operate from a supply range of 2.5V to 5.5V (±1.25 to ±2.75). The input voltage range extends 300mV below the negative rail and 1.2V below the positive rail.

The XR1009 and XR2009 offer superior dynamic performance with a 35MHz small signal bandwidth and 27V/µs slew rate. The combination of low power, high bandwidth, and rail-to-rail performance make the XR1009 and XR2009 well suited for battery-powered communication/ computing systems.

### FEATURES

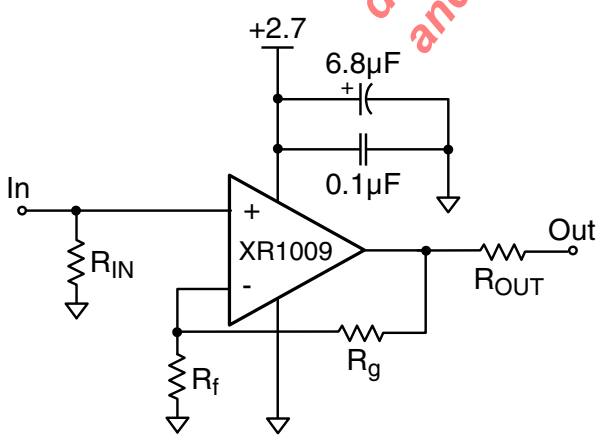
- 208µA supply current
- 35MHz bandwidth
- Input voltage range with 5V supply: -0.3V to 3.8V
- Output voltage range with 5V supply: 0.08V to 4.88V
- 27V/µs slew rate
- 21nV/√Hz input voltage noise
- 13mA linear output current
- Fully specified at 2.7V and 5V supplies
- Replaces MAX4281

### APPLICATIONS

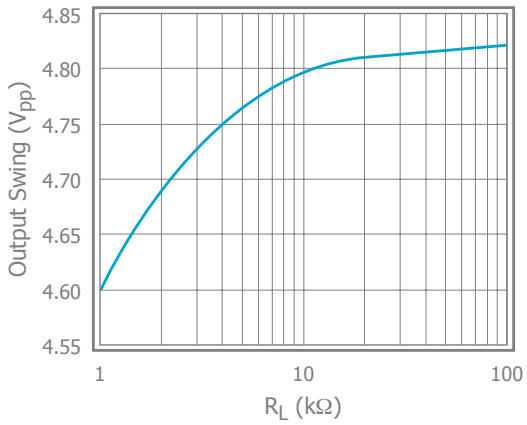
- Portable/battery-powered applications
- Mobile communications, cell phones, pagers
- ADC buffer
- Active filters
- Portable test instruments
- Signal conditioning
- Medical equipment
- Portable medical instrumentation
- Interactive whiteboards



## Frequency Response




## Output Swing vs. $R_L$



## Absolute Maximum Ratings

Stresses beyond the limits listed below may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

$V_S$ ..... 0V to 6V

$V_{IN}$ ..... $-V_S$ - 0.5V to $+V_S$ +0.5V

Continuous Output Current..... -30mA to +30mA

## Operating Conditions

Supply Voltage Range .....2.5 to 5.5V

Operating Temperature Range .....-40°C to 125°C

Junction Temperature .....150°C

Storage Temperature Range.....-65°C to 150°C

Lead Temperature (Soldering, 10s) .....260°C

## Package Thermal Resistance

$\theta_{JA}$ (TSOT23-5) .....215°C/W

$\theta_{JA}$ (SOIC-8) .....150°C/W

$\theta_{JA}$ (MSOP-8) ..... 200°C/W

Package thermal resistance ($\theta_{JA}$), JEDEC standard, multi-layer test boards, still air.

## ESD Protection

XR1009 (HBM) .....2kV

XR2009 (HBM) .....2.5kV

ESD Rating for HBM (Human Body Model).

## Electrical Characteristics at +2.7V

$T_A$ = 25°C, $V_S$ = +2.7V, $R_f$ = $R_g$ = 2.5kΩ, $R_L$ = 2kΩ to $V_S$/2; G = 2; unless otherwise noted.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Frequency Domain Response | | | | | | |
| $UGBW_{SS}$ | Unity Gain -3dB Bandwidth | G = +1, $V_{OUT}$ = 0.05$V_{pp}$, $R_f$ = 0 | | 28 | | MHz |
| $BW_{SS}$ | -3dB Bandwidth | G = +2, $V_{OUT}$ < 0.2$V_{pp}$ | | 15 | | MHz |
| $BW_{LS}$ | Large Signal Bandwidth | G = +2, $V_{OUT}$ = 2$V_{pp}$ | | 7 | | MHz |
| GBWP | Gain Bandwidth Product | G = +11, $V_{OUT}$ = 0.2$V_{pp}$ | | 16 | | MHz |
| Time Domain Response | | | | | | |
| $t_R$, $t_F$ | Rise and Fall Time | $V_{OUT}$ = 0.2V step; (10% to 90%) | | 16 | | ns |
| $t_S$ | Settling Time to 0.1% | $V_{OUT}$ = 1V step | | 140 | | ns |
| OS | Overshoot | $V_{OUT}$ = 1V step | | 1 | | % |
| SR | Slew Rate | G = -1, 2V step | | 20 | | V/µs |
| Distortion/Noise Response | | | | | | |
| HD2 | 2nd Harmonic Distortion | 100kHz, $V_{OUT}$ = 1$V_{pp}$ | | -85 | | dBc |
| HD3 | 3rd Harmonic Distortion | 100kHz, $V_{OUT}$ = 1$V_{pp}$ | | -63 | | dBc |
| THD | Total Harmonic Distortion | 100kHz, $V_{OUT}$ = 1$V_{pp}$ | | 62 | | dB |
| $e_n$ | Input Voltage Noise | >10kHz | | 23 | | nV/√Hz |
| XTALK | Crosstalk | 100kHz, $V_{OUT}$ = 0.2$V_{pp}$ | | 98 | | dB |
| DC Performance | | | | | | |
| $V_{IO}$ | Input Offset Voltage | | | 0.8 | | mV |
| $d_{VIO}$ | Average Drift | | | 11 | | µV/°C |
| $I_B$ | Input Bias Current | | | 0.37 | | µA |
| $dI_B$ | Average Drift | | | 1 | | nA/°C |
| $I_{OS}$ | Input Offset Current | | | 8 | | nA |
| PSRR | Power Supply Rejection Ratio | DC | 56 | 60 | | dB |
| $A_{OL}$ | Open Loop Gain | $V_{OUT}$ = $V_S$ / 2 | | 65 | | dB |
| $I_S$ | Supply Current | per channel | | 185 | | µA |
| Input Characteristics | | | | | | |
| $R_{IN}$ | Input Resistance | Non-inverting | | >10 | | MΩ |
| $C_{IN}$ | Input Capacitance | | | 1.4 | | pF |
| CMIR | Common Mode Input Range | | | -0.3 to 1.5 | | V |
| CMRR | Common Mode Rejection Ratio | DC, $V_{CM}$ = 0V to $V_S$ - 1.5V | | 92 | | dB |
| Output Characteristics | | | | | | |
| $V_{OUT}$ | Output Voltage Swing | $R_L$ = 2kΩ to $V_S$ / 2 | | 0.08 to 2.6 | | V |
| | | $R_L$ = 10kΩ to $V_S$ / 2 | | 0.06 to 2.62 | | V |
| $I_{OUT}$ | Output Current | | | ±8 | | mA |
| $I_{SC}$ | Short Circuit Current | | | ±12.5 | | mA |

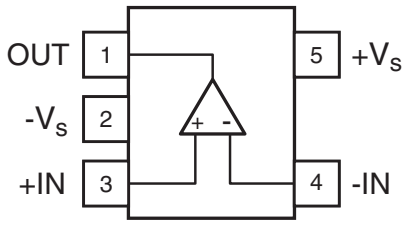
## Electrical Characteristics at +5V

$T_A$ = 25°C, $V_S$ = +5V, $R_f$ = $R_g$ = 2.5kΩ, $R_L$ = 2kΩ to $V_S$/2; G = 2; unless otherwise noted.

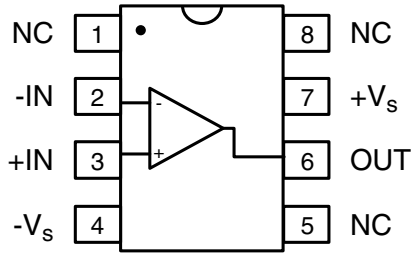
| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Frequency Domain Response | | | | | | |
| $UGBW_{SS}$ | Unity Gain -3dB Bandwidth | G = +1, $V_{OUT}$ = 0.05$V_{pp}$, $R_f$ = 0 | | 35 | | MHz |
| $BW_{SS}$ | -3dB Bandwidth | G = +2, $V_{OUT}$ < 0.2$V_{pp}$ | | 18 | | MHz |
| $BW_{LS}$ | Large Signal Bandwidth | G = +2, $V_{OUT}$ = 2$V_{pp}$ | | 8 | | MHz |
| GBWP | Gain Bandwidth Product | G = +11, $V_{OUT}$ = 0.2$V_{pp}$ | | 20 | | MHz |
| Time Domain Response | | | | | | |
| $t_R$, $t_F$ | Rise and Fall Time | $V_{OUT}$ = 0.2V step; (10% to 90%) | | 13 | | ns |
| $t_S$ | Settling Time to 0.1% | $V_{OUT}$ = 1V step | | 140 | | ns |
| OS | Overshoot | $V_{OUT}$ = 1V step | | 1 | | % |
| SR | Slew Rate | G = -1, 2V step | | 27 | | V/µs |
| Distortion/Noise Response | | | | | | |
| HD2 | 2nd Harmonic Distortion | 100kHz, $V_{OUT}$ = 2$V_{pp}$ | | -78 | | dBc |
| HD3 | 3rd Harmonic Distortion | 100kHz, $V_{OUT}$ = 2$V_{pp}$ | | -66 | | dBc |
| THD | Total Harmonic Distortion | 100kHz, $V_{OUT}$ = 2$V_{pp}$ | | 65 | | dB |
| $e_n$ | Input Voltage Noise | >10kHz | | 21 | | nV/√Hz |
| XTALK | Crosstalk | 100kHz, $V_{OUT}$ = 0.2$V_{pp}$ | | 98 | | dB |
| DC Performance | | | | | | |
| $V_{IO}$ | Input Offset Voltage | | -5 | -1.5 | 5 | mV |
| $d_{VIO}$ | Average Drift | | | 20 | | µV/°C |
| $I_B$ | Input Bias Current | | -1.3 | 0.37 | 1.3 | µA |
| $dI_B$ | Average Drift | | | 1 | | nA/°C |
| $I_{OS}$ | Input Offset Current | | | 7 | 130 | nA |
| PSRR | Power Supply Rejection Ratio | DC | 56 | 60 | | dB |
| $A_{OL}$ | Open Loop Gain | $V_{OUT}$ = $V_S$ / 2 | 56 | 62 | | dB |
| $I_S$ | Supply Current | per channel | | 208 | 260 | µA |
| Input Characteristics | | | | | | |
| $R_{IN}$ | Input Resistance | Non-inverting | | >10 | | MΩ |
| $C_{IN}$ | Input Capacitance | | | 1.2 | | pF |
| CMIR | Common Mode Input Range | | | -0.3 to 3.8 | | V |
| CMRR | Common Mode Rejection Ratio | DC, $V_{CM}$ = 0V to $V_S$ - 1.5V | 65 | 95 | | dB |
| Output Characteristics | | | | | | |
| $V_{OUT}$ | Output Voltage Swing | $R_L$ = 2kΩ to $V_S$ / 2 | 0.2 to 4.7 | 0.1 to 4.8 | | V |
| | | $R_L$ = 10kΩ to $V_S$ / 2 | | 0.08 to 4.88 | | V |
| $I_{OUT}$ | Output Current | | | ±8.5 | | mA |
| $I_{SC}$ | Short Circuit Current | | | ±13 | | mA |

## XR1009 Pin Configurations

### TSOT-5




### SOIC-8




## XR1009 Pin Assignments

### TSOT-5

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | OUT | Output |
| 2 | $-V_S$ | Negative supply |
| 3 | +IN | Positive input |
| 4 | -IN | Negative input |
| 5 | $+V_S$ | Positive supply |

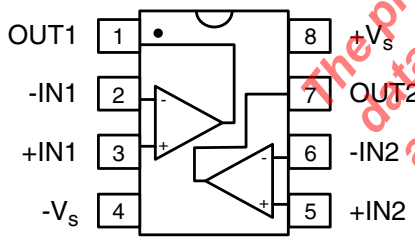
### SOIC-8

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | NC | No Connect |
| 2 | -IN | Negative input |
| 3 | +IN | Positive input |
| 4 | $-V_S$ | Negative supply |
| 5 | NC | No Connect |
| 6 | OUT | Output |
| 7 | $+V_S$ | Positive supply |
| 8 | NC | No Connect |



## XR2009 Pin Configuration

### SOIC-8 / MSOP-8




## XR2009 Pin Assignments

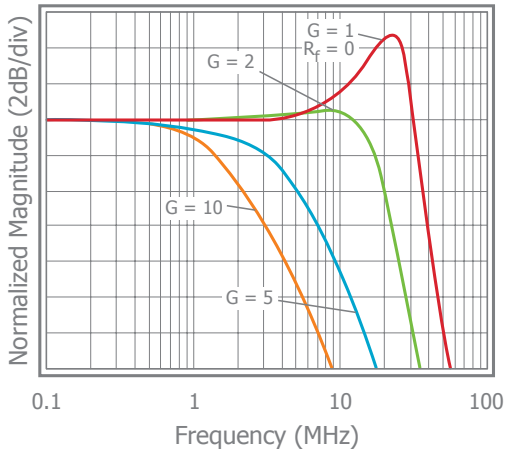
### SOIC-8 / MSOP-8

| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | OUT1 | Output, channel 1 |
| 2 | -IN1 | Negative input, channel 1 |
| 3 | +IN1 | Positive input, channel 1 |
| 4 | $-V_S$ | Negative supply |
| 5 | +IN2 | Positive input, channel 2 |
| 6 | -IN2 | Negative input, channel 2 |
| 7 | OUT2 | Output, channel 2 |
| 8 | $+V_S$ | Positive supply |

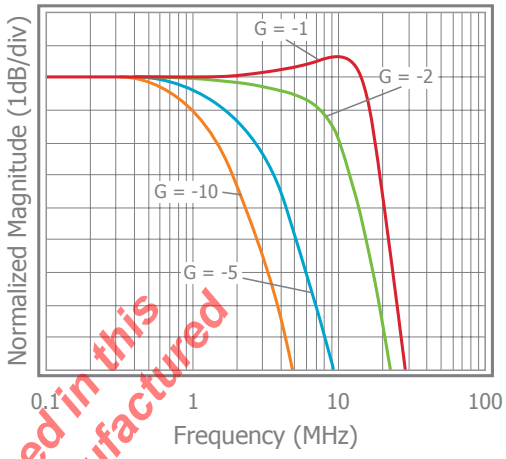
## Typical Performance Characteristics

$T_A$ = 25°C, $V_S$ = +5V, $R_f$ = $R_g$ = 2.5kΩ, $R_L$ = 2kΩ to $V_S$/2; G = 2; unless otherwise noted.

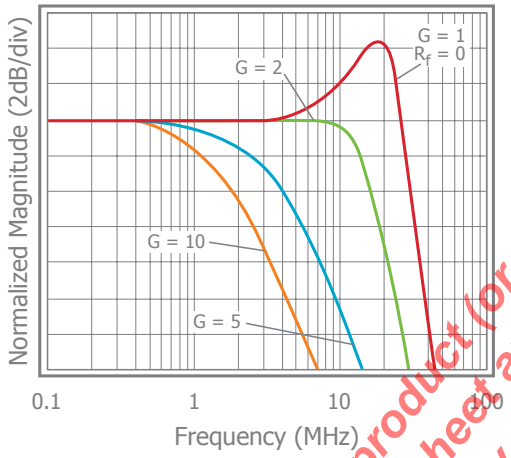
Non-Inverting Frequency Response at $V_S$ = 5V



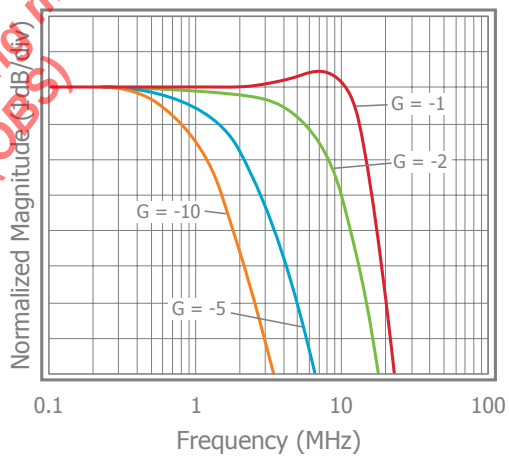

Inverting Frequency Response at $V_S$ = 5V



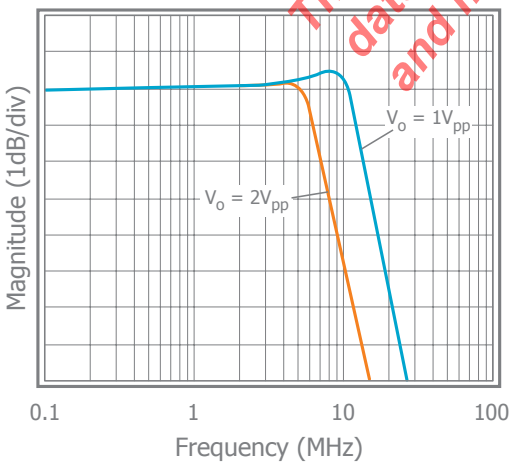

Non-Inverting Frequency Response at $V_S$ = 2.7V



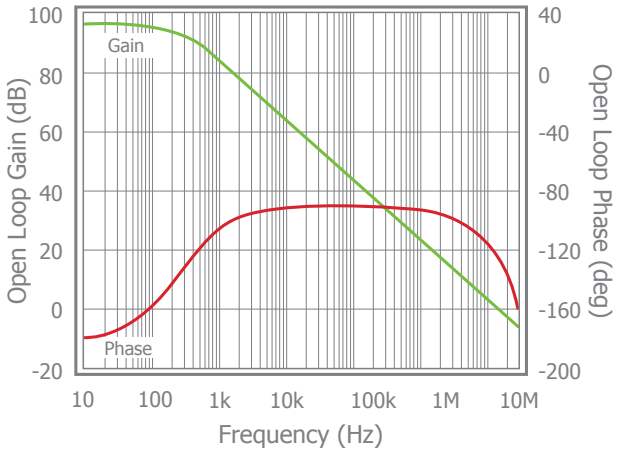

Inverting Frequency Response at $V_S$ = 2.7V




Frequency Response vs. $V_{OUT}$



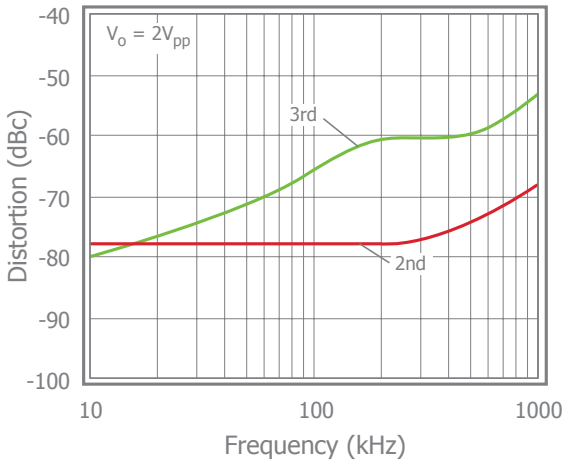

Open Loop Gain & Phase vs. Frequency



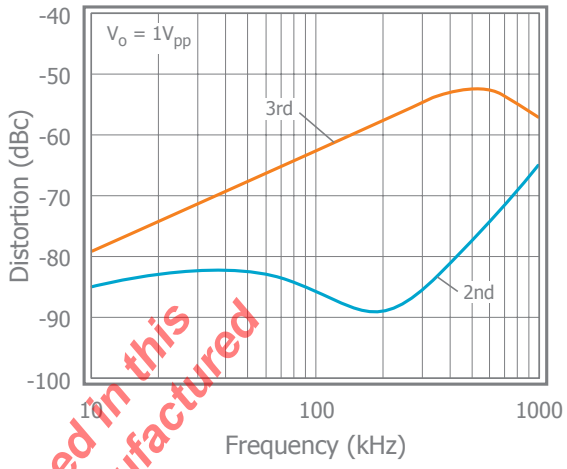
## Typical Performance Characteristics

$T_A$ = 25°C, $V_S$ = +5V, $R_f$ = $R_g$ = 2.5kΩ, $R_L$ = 2kΩ to $V_S$/2; G = 2; unless otherwise noted.

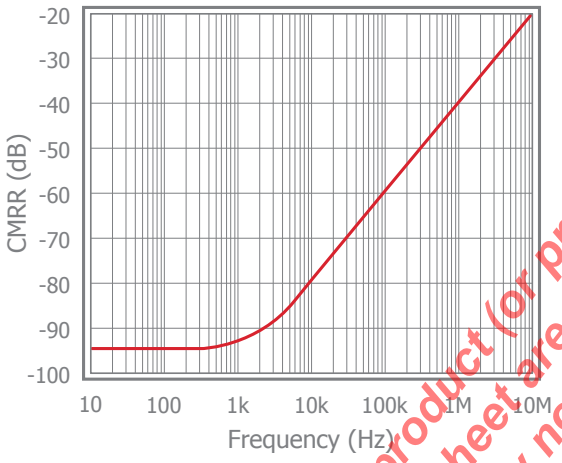
2nd & 3rd Harmonic Distortion at $V_S$ = 5V



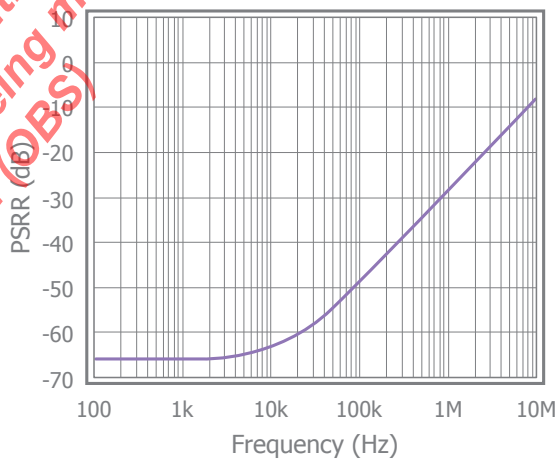

2nd & 3rd Harmonic Distortion at $V_S$ = 2.7V



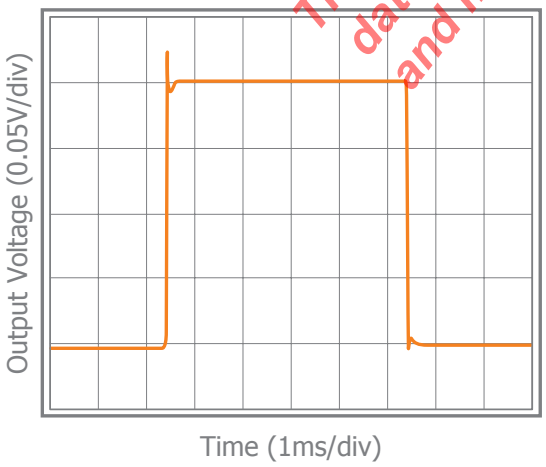

CMRR



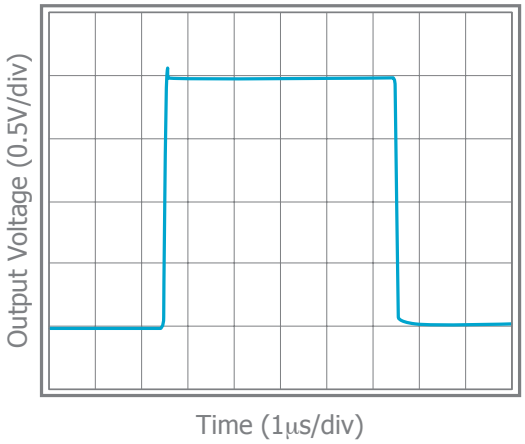

PSRR




Small Signal Pulse Response



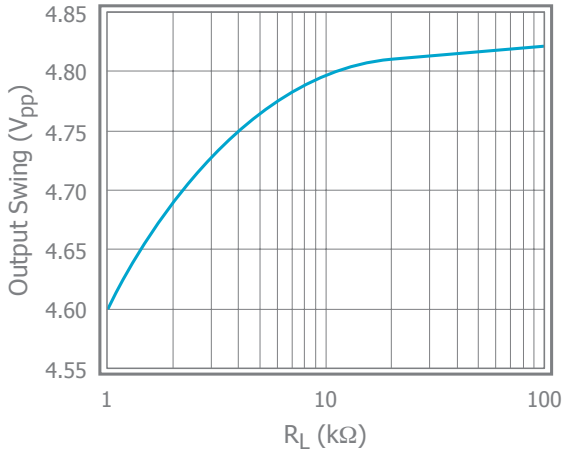

Large Signal Pulse Response



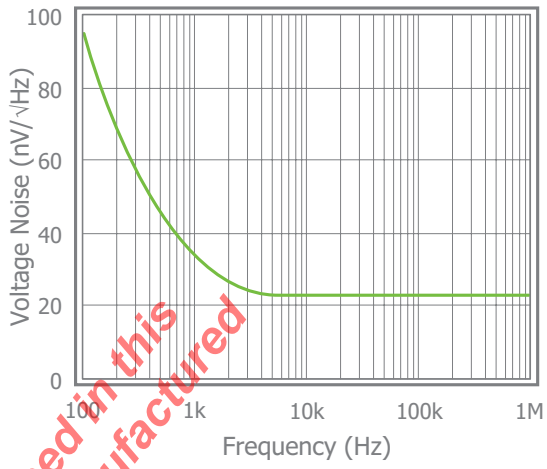
## Typical Performance Characteristics

$T_A$ = 25°C, $V_S$ = +5V, $R_f$ = $R_g$ = 2.5kΩ, $R_L$ = 2kΩ to $V_S$/2; G = 2; unless otherwise noted.

Output Swing vs. $R_L$




Input Voltage Noise



## Application Information

### General Description

The XR1009 and XR2009 are a single supply, general purpose, voltage-feedback amplifiers fabricated on a complementary bipolar process. The XR1009 offers 35MHz unity gain bandwidth, 27V/µs slew rate, and only 208µA supply current. It features a rail-to-rail output stage and is unity gain stable.

The design utilizes a patent pending topology that provides increased slew rate performance. The common mode input range extends to 300mV below ground and to 1.2V below Vs. Exceeding these values will not cause phase reversal. However, if the input voltage exceeds the rails by more than 0.5V, the input ESD devices will begin to conduct. The output will stay at the rail during this overdrive condition.

The design uses a Darlington output stage. The output stage is short circuit protected and offers “soft” saturation protection that improves recovery time.

Figures 1, 2, and 3 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations. Figure 4 shows the typical non-inverting gain circuit for single supply applications.

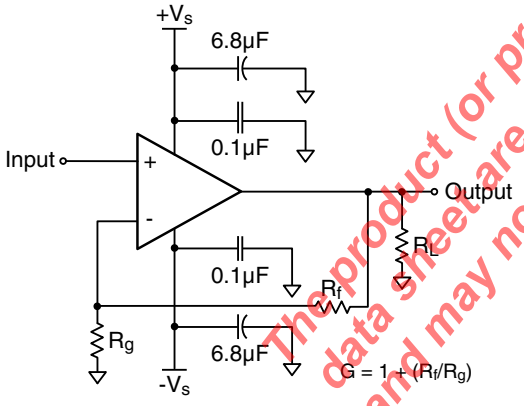



Figure 1: Typical Non-Inverting Gain Circuit

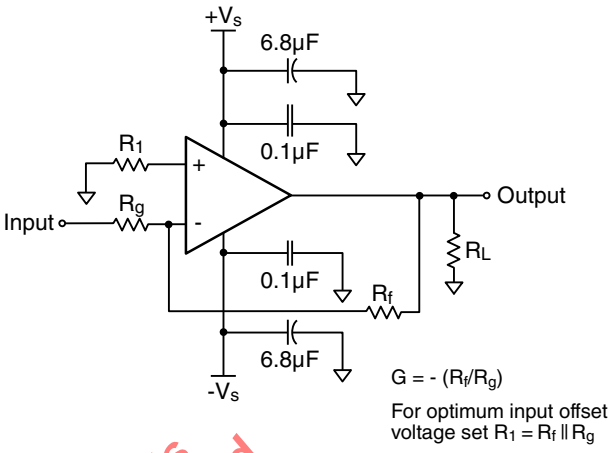



Figure 2: Typical Inverting Gain Circuit

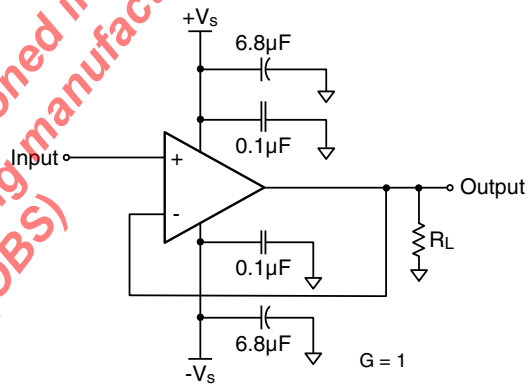



Figure 3: Unity Gain Circuit

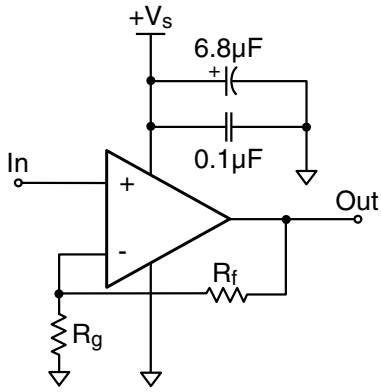



Figure 4: Single Supply Non-Inverting Gain Circuit

## Power Dissipation

Power dissipation should not be a factor when operating under the stated 2kΩ load condition. However, applications with low impedance, DC coupled loads should be analyzed to ensure that maximum allowed junction temperature is not exceeded. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond it's intended operating range.

Maximum power levels are set by the absolute maximum junction rating of 150°C. To calculate the junction temperature, the package thermal resistance value $Theta_{JA}$ ($\theta_{JA}$) is used along with the total die power dissipation.

$$T_{Junction} = T_{Ambient} + (\theta_{JA} \times P_D)$$

Where $T_{Ambient}$ is the temperature of the working environment.

In order to determine $P_D$, the power dissipated in the load needs to be subtracted from the total power delivered by the supplies.

$$P_D = P_{supply} - P_{load}$$

Supply power is calculated by the standard power equation.

$$P_{supply} = V_{supply} \times I_{RMSsupply}$$

$$V_{supply} = V_{S+} - V_{S-}$$

Power delivered to a purely resistive load is:

$$P_{load} = ((V_{load})_{RMS}^2)/Rload_{eff}$$

The effective load resistor ($Rload_{eff}$) will need to include the effect of the feedback network. For instance,

$Rload_{eff}$ in Figure 3 would be calculated as:

$$R_L \parallel (R_f + R_g)$$

These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here, $P_D$ can be found from

$$P_D = P_{Quiescent} + P_{Dynamic} - P_{load}$$

Quiescent power can be derived from the specified $I_S$ values along with known supply voltage, $V_{supply}$. Load power can be calculated as above with the desired signal amplitudes using:

$$(V_{load})_{RMS} = V_{peak} / \sqrt{2}$$

$$(I_{load})_{RMS} = (V_{load})_{RMS} / Rload_{eff}$$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$$P_{Dynamic} = (V_{S+} - V_{load})_{RMS} \times (I_{load})_{RMS}$$

Assuming the load is referenced in the middle of the power rails or $V_{supply}/2$.

The XR1009 is short circuit protected. However, this may not guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. Figure 5 shows the maximum safe power dissipation in the package vs. the ambient temperature for the packages available.

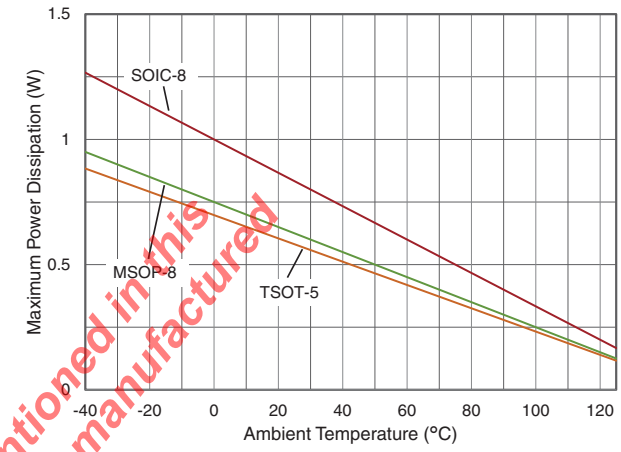



Figure 5. Maximum Power Derating

## Driving Capacitive Loads

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance, $R_S$, between the amplifier and the load to help improve stability and settling performance. Refer to Figure 6.

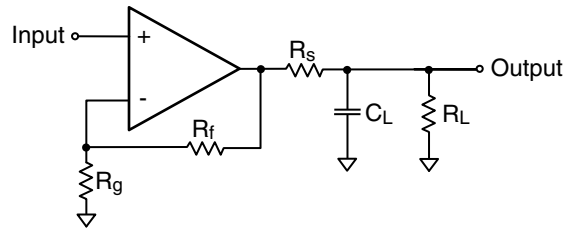



Figure 6. Addition of $R_S$ for Driving Capacitive Loads

## Overdrive Recovery

For an amplifier, an overdrive condition occurs when the output and/or input ranges are exceeded. The recovery time varies based on whether the input or output is overdriven and by how much the ranges are exceeded. The XR1009, and XR2009 will typically recover in less than 20ns from an overdrive condition.

## Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. Exar has evaluation boards to use as a guide for high frequency layout and as an aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8µF and 0.1µF ceramic capacitors for power supply decoupling
- Place the 6.8µF capacitor within 0.75 inches of the power pin
- Place the 0.1µF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

## Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

| Evaluation Board # | Products |
|---|---|
| CEB002 | XR1009 in TSOT |
| CEB003 | XR1009 in SOIC |
| CEB006 | XR2009 in SOIC |
| CEB010 | XR2009 in MSOP |

## Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 9-18 These evaluation boards are built for dual-supply operation. Follow these steps to use the board in a single-supply application:

1. Short $-V_S$ to ground.
2. Use C3 and C4, if the $-V_S$ pin of the amplifier is not directly connected to the ground plane.

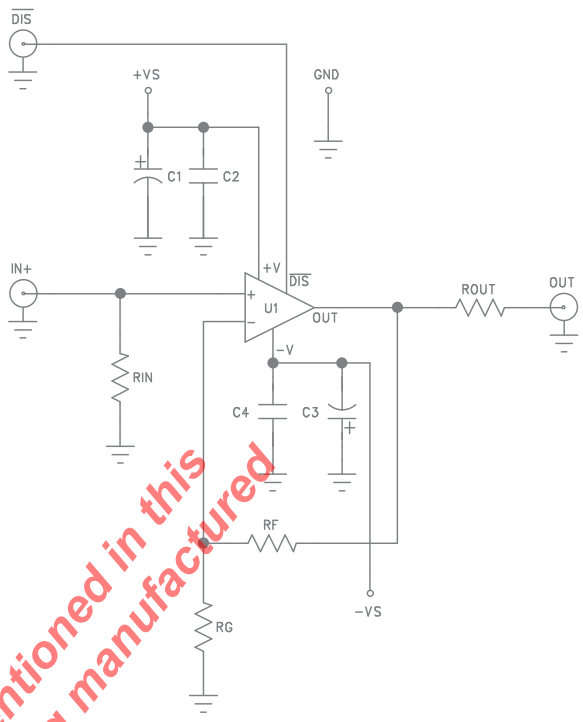



Figure 9. CEB002 & CEB003 Schematic

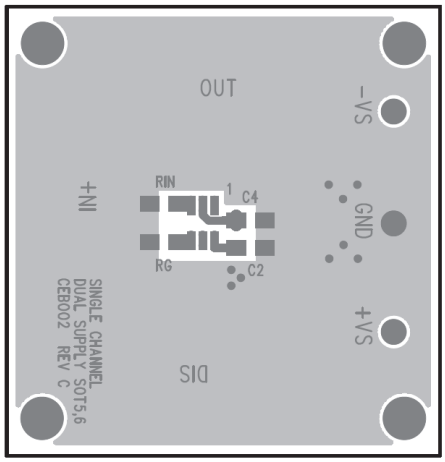



Figure 10. CEB002 Top View

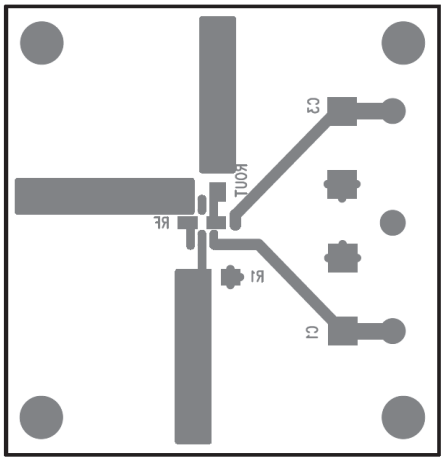



Figure 11. CEB002 Bottom View

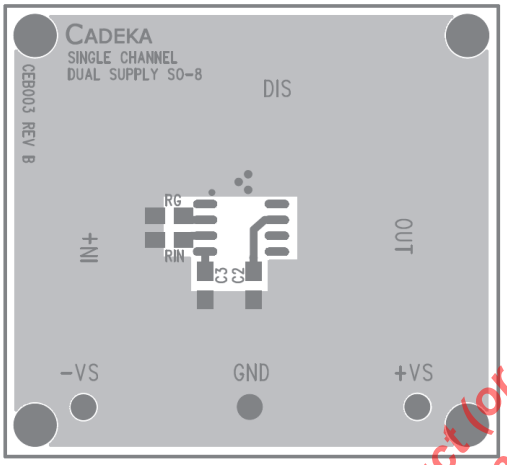



Figure 12. CEB003 Top View

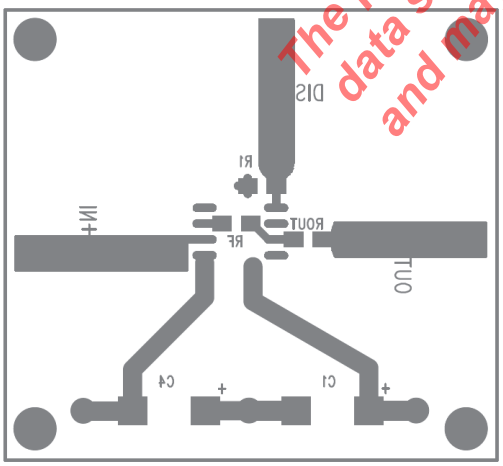



Figure 13. CEB003 Bottom View

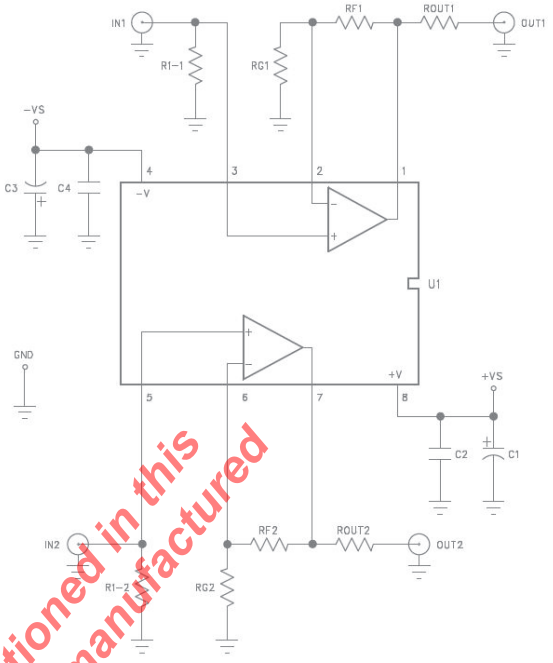



Figure 14. CEB006 & CEB010 Schematic

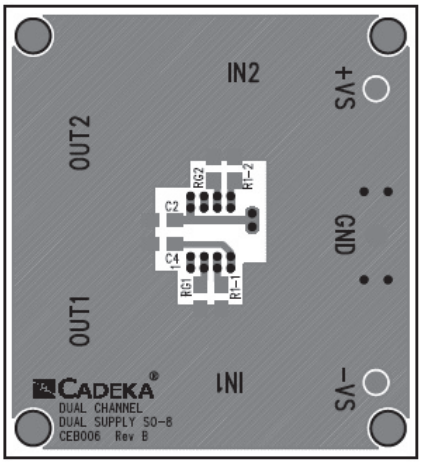



Figure 15. CEB006 Top View

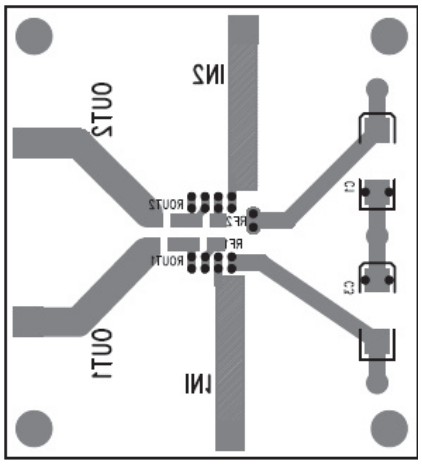



Figure 16. CEB006 Bottom View

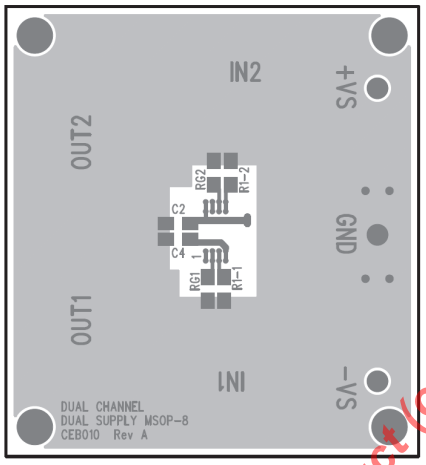



Figure 17. CEB010 Top View

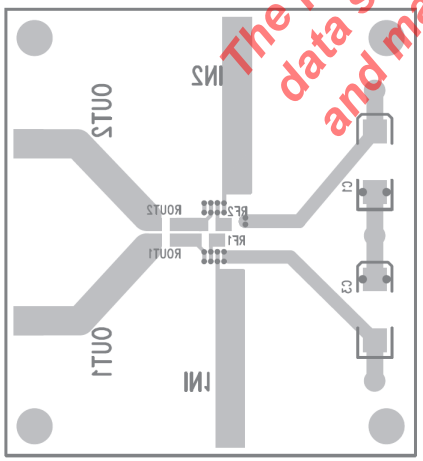
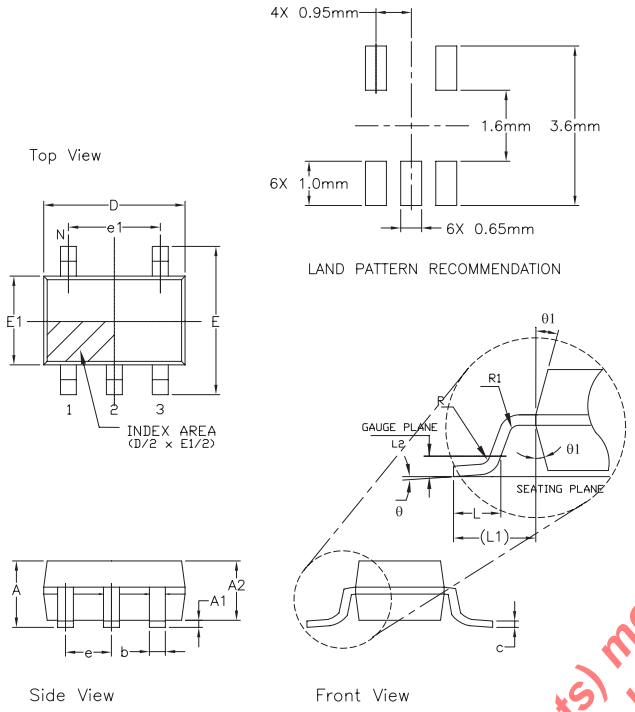



Figure 18. CEB010 Bottom View

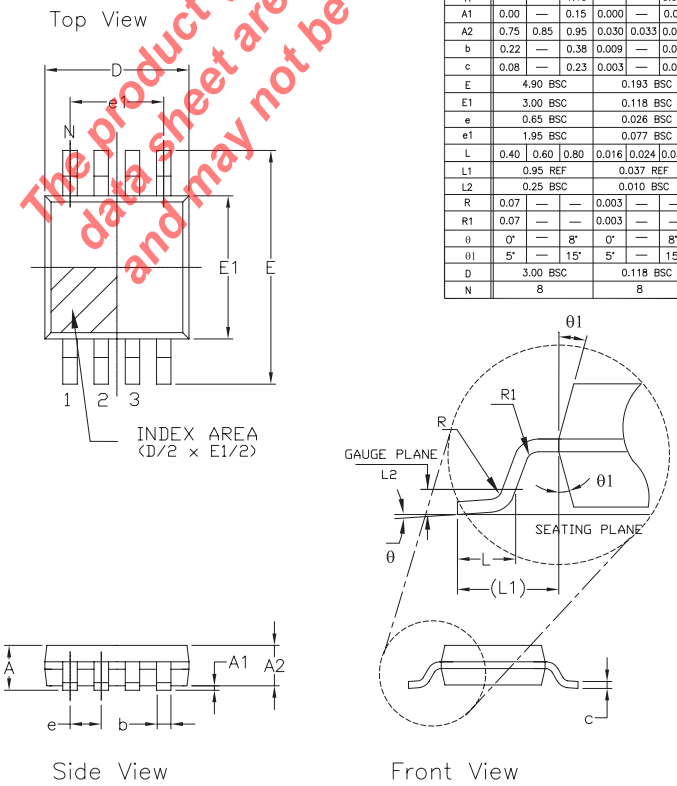
# Mechanical Dimensions

## TSOT-5 Package



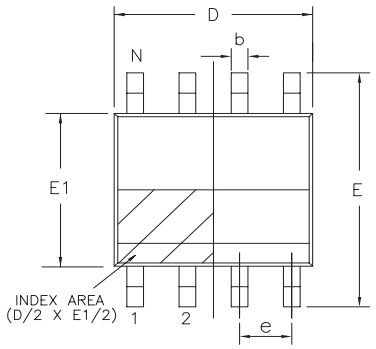

| 5 Pin TSOT (OPTION 2) | | | | | | |
|---|---|---|---|---|---|---|
| SYMBOLS | DIMENSION IN MM (Control Unit) | | | DIMENSION IN INCH (Reference Unit) | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.75 | — | 0.80 | 0.030 | — | 0.031 |
| A1 | 0.00 | — | 0.05 | 0.000 | — | 0.002 |
| A2 | 0.70 | 0.75 | 0.78 | 0.028 | 0.030 | 0.031 |
| b | 0.35 | — | 0.50 | 0.012 | — | 0.020 |
| c | 0.10 | — | 0.20 | 0.003 | — | 0.008 |
| D | 2.90 BSC | | | 0.114 BSC | | |
| E | 2.80 BSC | | | 0.110 BSC | | |
| E1 | 1.60 BSC | | | 0.063 BSC | | |
| e | 0.95 BSC | | | 0.038 BSC | | |
| e1 | 1.90 BSC | | | 0.075 BSC | | |
| L | 0.37 | 0.45 | 0.60 | 0.012 | 0.018 | 0.024 |
| L1 | 0.60 REF | | | 0.024 REF | | |
| L2 | 0.25 BSC | | | 0.010 BSC | | |
| R | 0.10 | — | — | 0.004 | — | — |
| R1 | 0.10 | — | 0.25 | 0.004 | — | 0.010 |
| θ | 0° | 4° | 8° | 0° | 4° | 8° |
| θ1 | 4° | 10° | 12° | 4° | 10° | 12° |
| N | 5 | | | 5 | | |

## MSOP-8 Package

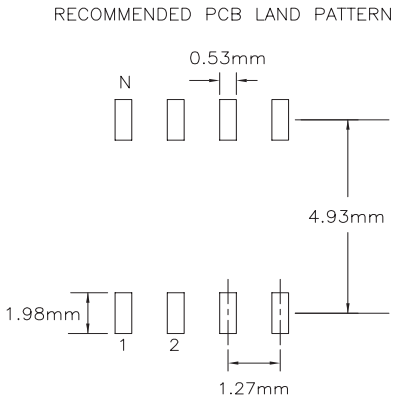


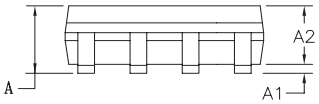

| 8 Pin MSOP JEDEC MO-187 Variation AA | | | | | | |
|---|---|---|---|---|---|---|
| SYMBOLS | DIMENSIONS IN MM (Control Unit) | | | DIMENSIONS IN INCH (Reference Unit) | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | — | — | 1.10 | — | — | 0.043 |
| A1 | 0.00 | — | 0.15 | 0.000 | — | 0.006 |
| A2 | 0.75 | 0.85 | 0.95 | 0.030 | 0.033 | 0.037 |
| b | 0.22 | — | 0.38 | 0.009 | — | 0.015 |
| c | 0.08 | — | 0.23 | 0.003 | — | 0.009 |
| E | 4.90 BSC | | | 0.193 BSC | | |
| E1 | 3.00 BSC | | | 0.118 BSC | | |
| e | 0.65 BSC | | | 0.026 BSC | | |
| e1 | 1.95 BSC | | | 0.077 BSC | | |
| L | 0.40 | 0.60 | 0.80 | 0.016 | 0.024 | 0.031 |
| L1 | 0.95 REF | | | 0.037 REF | | |
| L2 | 0.25 BSC | | | 0.010 BSC | | |
| R | 0.07 | — | — | 0.003 | — | — |
| R1 | 0.07 | — | — | 0.003 | — | — |
| θ | 0° | — | 8° | 0° | — | 8° |
| θ1 | 5° | — | 15° | 5° | — | 15° |
| D | 3.00 BSC | | | 0.118 BSC | | |
| N | 8 | | | 8 | | |

## SOIC-8 Package

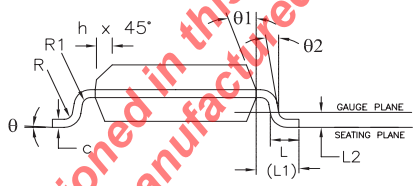



Top View




Side View




Front View

| 8 Pin SOICN JEDEC MS-012 Variation AA | | | | | | |
|---|---|---|---|---|---|---|
| SYMBOLS | DIMENSIONS IN MM (Control Unit) | | | DIMENSIONS IN INCH (Reference Unit) | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 1.35 | — | 1.75 | 0.053 | — | 0.069 |
| A1 | 0.10 | — | 0.25 | 0.004 | — | 0.010 |
| A2 | 1.25 | — | 1.65 | 0.049 | — | 0.065 |
| b | 0.31 | — | 0.51 | 0.012 | — | 0.020 |
| c | 0.17 | — | 0.25 | 0.007 | — | 0.010 |
| E | 6.00 BSC | | | 0.236 BSC | | |
| E1 | 3.90 BSC | | | 0.154 BSC | | |
| e | 1.27 BSC | | | 0.050 BSC | | |
| h | 0.25 | — | 0.50 | 0.010 | — | 0.020 |
| L | 0.40 | — | 1.27 | 0.016 | — | 0.050 |
| L1 | 1.04 REF | | | 0.041 REF | | |
| L2 | 0.25 BSC | | | 0.010 BSC | | |
| R | 0.07 | — | — | 0.003 | — | — |
| R1 | 0.07 | — | — | 0.003 | — | — |
| θ | 0° | — | 8° | 0° | — | 8° |
| θ1 | 5° | — | 15° | 5° | — | 15° |
| θ2 | 0° | — | — | 0° | — | — |
| D | 4.90 BSC | | | 0.193 BSC | | |
| N | 8 | | | 8 | | |

## Ordering Information

| Part Number | Package | Green | Operating Temperature Range | Packaging Quantity | Marking |
|---|---|---|---|---|---|
| XR1009 Ordering Information | | | | | |
| XR1009IST5X | TSOT-5 | Yes | -40°C to +125°C | 2.5k Tape & Reel | UC |
| XR1009IST5MTR | TSOT-5 | Yes | -40°C to +125°C | 250 Tape & Reel | UC |
| XR1009IST5EVB | Evaluation Board | N/A | N/A | N/A | N/A |
| XR1009ISO8X | SOIC-8 | Yes | -40°C to +125°C | 2.5k Tape & Reel | XR1009 |
| XR1009ISO8MTR | SOIC-8 | Yes | -40°C to +125°C | 250 Tape & Reel | XR1009 |
| XR1009ISO8EVB | Evaluation Board | N/A | N/A | N/A | N/A |
| XR2009 Ordering Information | | | | | |
| XR2009ISO8X | SOIC-8 | Yes | -40°C to +125°C | 2.5k Tape & Reel | XR2009 |
| XR2009ISO8MTR | SOIC-8 | Yes | -40°C to +125°C | 250 Tape & Reel | XR2009 |
| XR2009ISO8EVB | Evaluation Board | N/A | N/A | N/A | N/A |
| XR2009IMP8X | MSOP-8 | Yes | -40°C to +125°C | 2.5k Tape & Reel | 2009 |
| XR2009IMP8MTR | MSOP-8 | Yes | -40°C to +125°C | 250 Tape & Reel | 2009 |
| XR2009IMP8EVB | Evaluation Board | N/A | N/A | N/A | N/A |

Moisture sensitivity level for all parts is MSL-1.

## Revision History

| Revision | Date | Description |
|---|---|---|
| 1A | June 2014 | Initial Release [ECN 1426-10 I 06/24/14] |
| 1B | Sept 2014 | Added XR1009 ESD, increased operating temperature range, updated package outline drawings, and removed Preliminary note on XR1009. [ECN 1436-03 I 09/04/14] |



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A New Direction in Mixed-Signal

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