INTRODUCTION TO CALLER ID

The Caller ID feature is an on-hook capability that provides the user with information about the caller before actually answering the call. The information displayed is a data message sent from the central office to the CPE using simplex VDI-1 (Voice Band Digital Interface) before the first 20Hz ringing burst. The data contains the date (month and day), time (hour and minutes), and calling party number information in one of three forms:

a) 2 to 10 digit extension

b) privacy indication for those calling parties which do not want their number displayed

c) out-of-area indication if the calling number cannot be recovered for an on-screen display

VDI-1 is specified in terms of three architectural layers (physical, datalink and presentation layers). The XR-2211 is primarily concerned with the physical layer interface requirements, which refers to the electrical and procedural characteristics that the CO uses to physically connect to the CPE. It is concerned solely with transmitting a stream of bits, without regards to meaning or structure. The data link layer provides the procedural characteristics that allow the CO to transfer complete units of information to the CPE and the presentation layer defines the general content and syntax needed to transmit recognizable information.

MESSAGE FORMAT

Caller ID information is sent to the CPE after the line reversal and before the first ring. The central office waits 100mS after the line reversal before starting transmission of the tone alert followed with the data, and completes the transmission 200mS prior to the ringing signal.

FSK data is sent to the CPE as a single or multiple message format (see *Figure 1* & *Figure 2*). All caller ID messages are preceded by a 250msec channel seizure sequence (01010101 pattern). This signal is sent at the beginning of each message to alert the CPE of the coming information. This is then followed by a 150msec of ones (1300Hz), intended to aid in "conditioning" the receiver for data. The message begins with the message type in one byte sequence (see *Table 1*). After that, a message length or data word count value, specifies the number of data words that are going to be transmitted following this word. This number does not include the check sum word which follows the last data word. Caller ID information bits are grouped into 8-bit characters preceded by a start bit (logical 0) and followed by a stop bit (logical 1)(see *Figure 1*). Data words are sent as ASCII characters without parity. The first eight words of data contain date (month and day) and local time (hour and minutes) two characters each. Word 15 through 24 carries the calling party information. The calling party information can be a 2 to 10 digit number or an ASCII alpha character indicating "P" for privacy or "O" for out of area. The last byte is a check sum word which is used by the CPE to insure the integrity of the received data. The check sum word consists of 2's complement of the module 256 sum of all the words transmitted from the CO including the message type, message length and data words. The CPE then derives the sum and adds this to the check sum. Any result other than zero indicates that the information was not received correctly. (See *Table 1.*)

Multiple data message formats include additional parameter information. Each parameter is a series of data words specifying parameter type, parameter length and parameter data as described in *Figure 2.*

EXAR Corporation, 48720 Kato Road, Fremont, CA 94538 ◆ (510) 668-7000 ◆ FAX (510) 668-7017

Word #	Signification	Binary Contents 7 6 5 4 3 2 1 0	Description	Dec Value	Hex Value	Mod. 256 in Hex
1	Msg. Type	1 0 0 0 0 0 0 0	Multi-format	128	80	80
2	Msg. Length	0 0 0 1 1 0 0 1	Total Msg.	25	19	99
3	Date Parameter	0 0 0 0 0 0 0 1	Parameter	1	01	9A
4	Date Field Length	0 0 0 0 1 0 0 0	Length	8	08	A2
5	Month	0 0 1 1 0 0 0 0	0	48	30	D2
6		0 0 1 1 0 1 0 0	4	52	34	06
7	Day	0 0 1 1 0 0 1 0	2	50	32	38
8		0 0 1 1 0 0 0 0	8	56	38	70
9	Hour	0 0 1 1 0 0 0 1	1	49	31	A1
10		0 0 1 1 0 0 1 1	3	51	33	D4
11	Minutes	0 0 1 1 0 0 1 0	2	50	32	06
12		0 0 1 1 0 0 0 0	0	48	30	36
13	Number Parameter	0 0 0 0 0 0 1 0	Parameter	2	02	38
14	# Field Length	0 0 0 0 1 0 1 0	Length	10	0A	42
15	Calling Number	0 0 1 1 0 1 0 0	4	52	34	76
16		0 0 1 1 0 0 0 0	0	48	30	A6
17		0 0 1 1 1 0 0 0	8	56	38	DE
18		0 0 1 1 0 1 0 0	4	52	34	12
19		0 0 1 1 0 0 1 1	3	51	33	45
20		0 0 1 1 0 1 0 0	4	52	34	79
21		0 0 1 1 0 1 1 0	6	54	36	AF
22		0 0 1 1 0 1 0 0	4	52	34	E3
23		0 0 1 1 0 0 0 0	0	48	30	13
24		0 0 1 1 0 0 0 0	0	48	30	43
25		0 0 0 0 1 0 0 0	Parameter	8	08	4B
26	Name Field Length	0 0 0 0 0 0 0 1	Length	1	01	4C
27	Reason Not Present	0 1 1 1 0 0 0 0	Private	112	70	**BC**
28	Checksum	0 1 0 0 0 1 0 0	Checksum	68	**44**	

Calculated Checksum + Received Checksum = 0 BC + 44 = 0 Mod 256

Table 1. Example of Caller Identification Coding

Link Type	Simplex
Modulation	FSK
Mark (logic 1)	1300Hz ±1.5%
Space (logic 0)	2100Hz ±1.5%
Received Signal Level for Mark	-8dBV to -40dBV
Received Signal Level for Space	The received signal levels space may differ by up to 6dB for mark and space.
Unwanted Signals	Total power of extraneous signals in the voice band (300-3400Hz) is at least 20dB below the signal levels.
Transmission Rate	1200 baud ±1%
Data Format	Serial binary asyncronous (1 start bit first, then 8 data bits with least significant bit first, followed by 1 stop bit minimum, up to 10 stop bits maximum). Start bit = 0, Stop bit = 1.

Table 2. V.23 Specifications

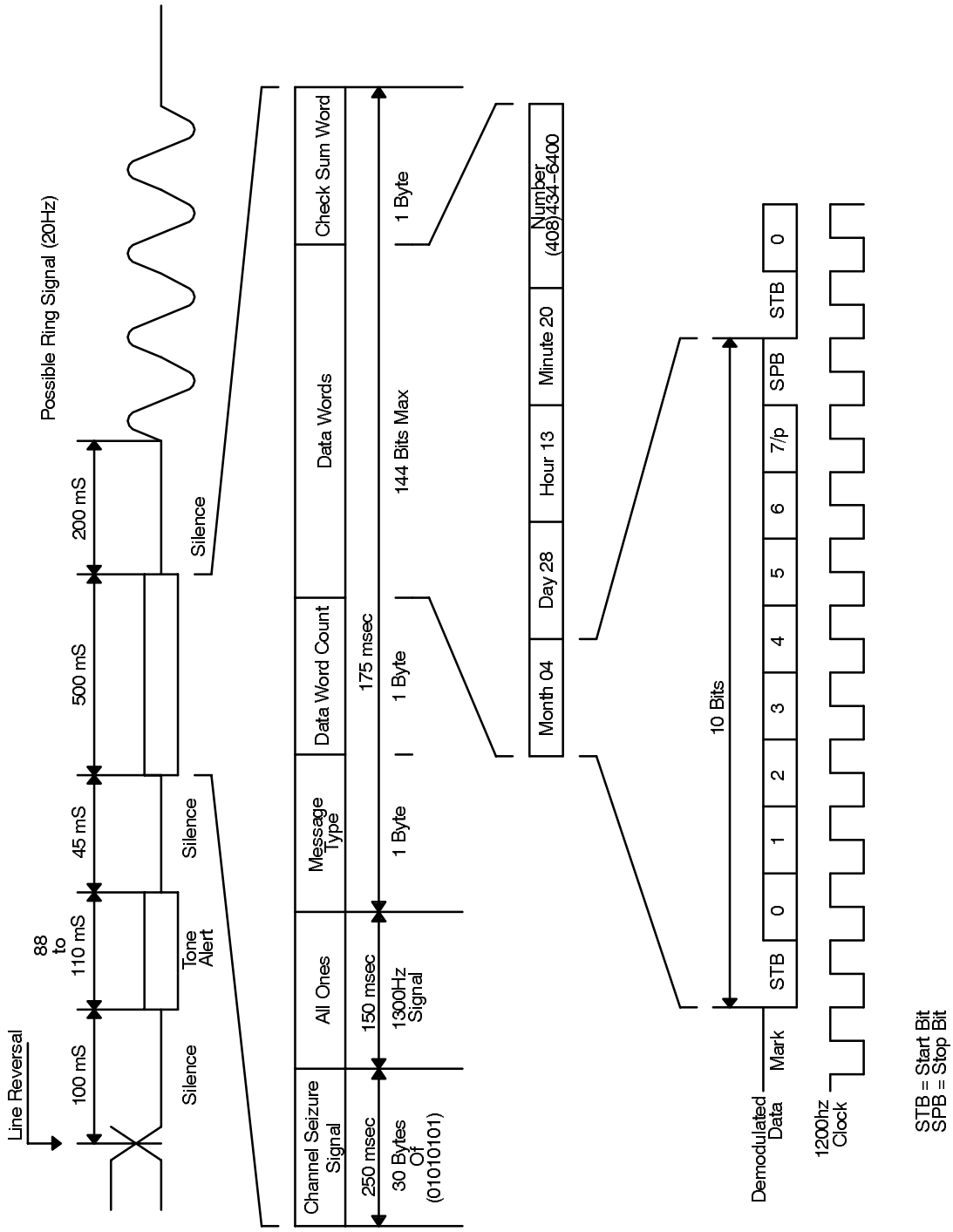


Figure 1. Multiple Data Message Format

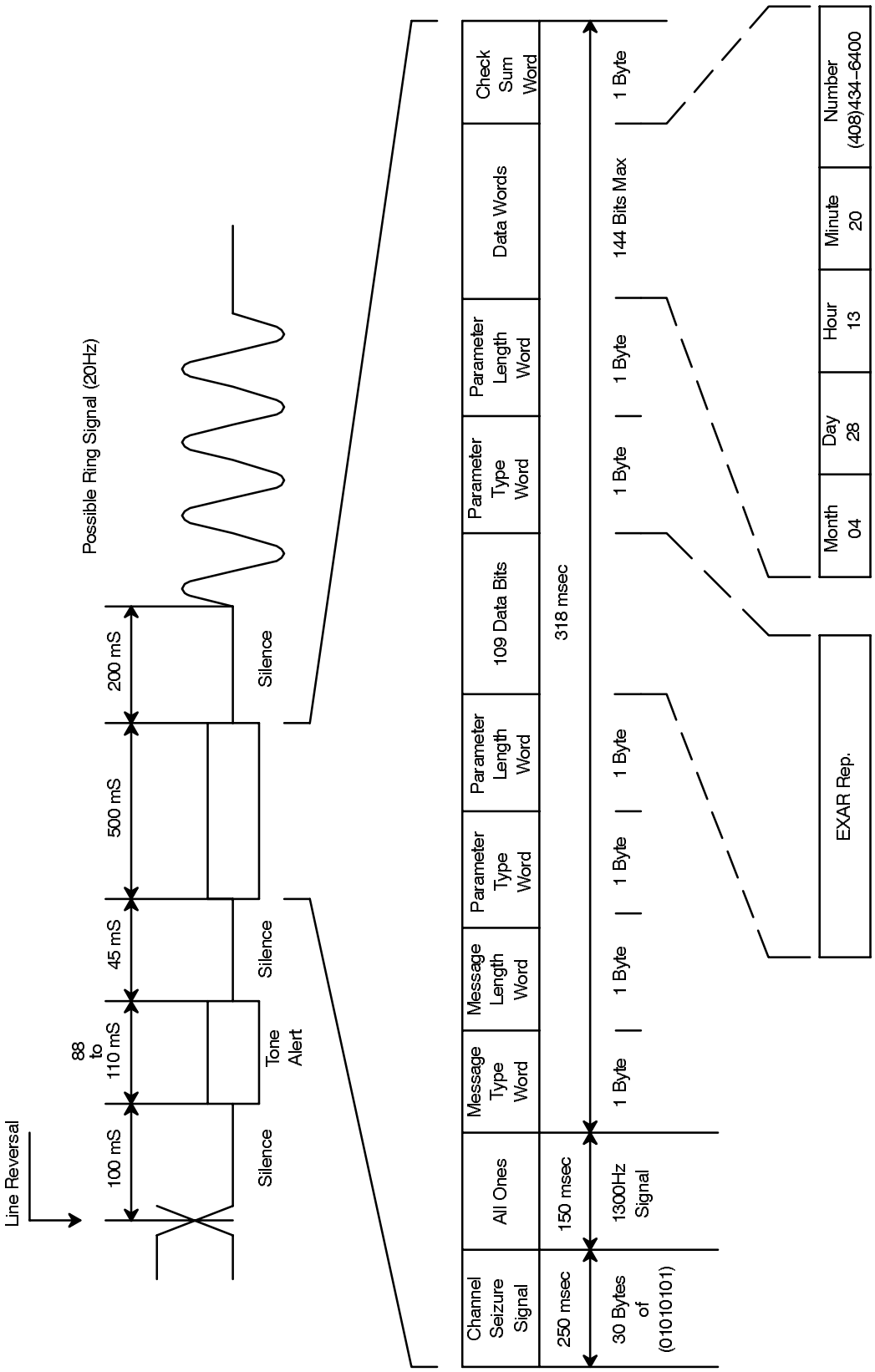


Figure 2. Multiple Data Message Format

DESIGN INSTRUCTIONS

The Caller ID demo-board design described herein is a "how to" example on building the basic components required to interface to the telephone line and extract the CO (Central Office) supplied CID (Caller ID) information. The kit includes a set of schematics describing how to interface to the telephone line and extract the CID information. The kit also includes a small executable program that upon receiving the CO provided CID information, converts this information into a form that can be displayed onto a PC's CRT. The program when used in conjunction with British Telecom (BT) SIN-242 specification is a useful reference when designing your own user interface. The schematics and software discussed herein were built, tested and proven to be functional. For U.S specifications, see TAN-008.

EQUIPMENT REQUIRED

The equipment requirement for this user interface is a PC 386 or greater, having an RS-232 port. The executable program provided with the demo-board design runs under a DOS environment.

General operation

The CID information provided by the CO to the CID demo-board is, after being decoded by the demo-board, routed directly into the PC via the RS-232 port. The PC is used to control whether or not power is applied to the demo board, as well as display the CID information.

While waiting for a CID signal most of the demo board is powered off. The first event in this sequence to occur is a Line Reversal and Tone Alert. This initiates the second event which, by way of the software program powers-up most of the demo-board, (this requires that the software program be running). The demo-board is now ready to receive the FSK encoded data sent by the CO. Once the data is demodulated, the information is then sent from the demo-board via a cable to the PC's RS-232 port. The program first captures and then displays the data on the PC's CRT.

After the CID information has been displayed, while still under software control, the demo-board is then returned to the powered down state.

POWER SUPPLIES

The demo-board design operates on a 6V supply. This supply is broken down into 3 separate sub-supplies, also 6V supplies. The line reversal circuit is connected to one of these supplies. This supply is directly connected to 6V and is always connected. A 6V supply was chosen here but a supply voltage between 5V and 12V can be used as well with no changes to the demo board design.

The balance of the demo-board (excluding the RS-232 interface, the MAXIM-235) is powered by a switched supply. The switched supply is activated by the line reversal. The MAXIM-235 is powered by the third supply. This scheme allows for easy measurement of the power consumed by each of the 3 blocks in both the powered-down and in the active modes. The total current consumed must be less than 20ma in an off-hook condition, to prevent the CO from sending a dial tone. The on-hook condition must consume less than 5μa which is 1 ringer equivalent.

INPUT STAGE AND DAA

The first stage (see *Figure 4*) of the demo-board design is the Input Stage. This stage includes the DAA function and the line reversal detector. The DAA provides the required isolation between the demo-board and telephone line while maintaining the ability to extract the data sent by the CO. The DAA optimally terminates the telephone line providing the proper Tip and Ring impedance.

The isolation provided by the DAA is required to prevent the full Ring Indicator voltage (max. 300V peak to peak on top of the max. 48V already provided by the CO battery), from damaging the low voltage components of the demo-board. At the same time, the DAA must reject any voltage less than the minimum 26V ring voltage as a not valid ring signal. Non-flammable fuse resistors, 10 ohms in value, are the first demo-board components to come into contact with the phone line, providing a fuse protection in case of over voltage.

In preparing to send CID information, the CO first sends a line reversal, which puts the demo-board on notice that it is about to receive CID information. The line reversal is used to power up the powered down portions of the demo-board.

The input stage also has an RC high pass filter which does not have any appreciable effect on the bandwidth of the filter stage. The demo-board has an AC impedance as

seen by the CO of more than 7,000 ohms. The only DC input resistance is created by the leakage of the input capacitors, which results in less than 5μa, the 1 ringer equivalent specification. Too small of a DC input resistance can potentially result in spurious low frequency noise inadvertently powering up the demo board. The input stage acts in part as a DC blocking stage. In addition, the input stage also applies both a DC and an AC load on Tip and Ring lines during the period after line reversal and before line seizure. Note that devices on the input stage must be able to withstand a maximum potential of 348V.

FILTER STAGE

The second stage (see *Figure 5*) of the demo-board design is a filtering stage that consists of a band pass filter and an amplifier. The bandpass function is composed of a 2nd order Low Pass Active Butterworth filter and a 3rd order High Pass Active Butterworth filter. This results in an effective -3db bandpass fre-uency range of 970 to 3750 Hertz, (see *Figure 10*). While an LM-324 was utilized as the gain element, it should be noted that almost any amplifier with a reasonably large gain (e.g. >10,000), relatively high input impedance and a moderately high bandwidth (e.g. >100,000 Hertz) can be used. The Output Drive strength should also be large enough to drive the filter load impedance. The bandpass response and the gain achieved by the filter can be altered by the following equations. In addition, a gain versus frequency plot of the low pass filter and of the high pass filter are provided in *Figure 8.*

The computer program provided in Reference [2], *Figure 27* was used to calculate order and component values of the Butterworth filters.

Order of the filter is calculated by:

$$N = INT\left(Log\frac{10\text{^}(AMAX\ /\ 10\text{-}1}{2((10\text{^}.3)\text{-}1)\ Log(Wn))}\right) + 1$$

AMAX: Attenuation at the stopband frequency.
Wn = F1 / F2 for low pass filter calculation and
Wn = FC /F1 for a high pass filter.
F1 = Stopband frequency.
FC = Cutoff frequency

Depending whether the values of N are even or odd, a different set of equations will be used. The program will execute an “For...Next” instruction until all the RC values are calculated. Gain at the passband will be unity.

Reference [1], Chapter 8 gives some basic theory about active filters.

Reference [3], explains some basic circuit theory.

The net result can be viewed as a bandpass filter with a 3 pole rolloff (60db/decade) on the low frequency side and a 2 pole rolloff (40db/decade) on the high frequency side. An additional requirement placed on the first and second stages is to filter out the 20 Hertz ring signal and the 60 or 50 Hertz electric line noise. The demo-board design achieves this by attenuating a 60 Hertz signal by at least 70db. To assure good filter characteristics 1% resistor and 5% capacitors should be used. If the input stage were to also be utilized for its high pass characteristics it too should have similarly controlled resistor and capacitor values.

GAIN STAGE

The third stage (see *Figure 5*) of the demo-board design is a wide band amplifier. The gain is chosen such that with the worst case signal, 3.0 mVrms (-48dBm), the PLL FSK decoder will still be working and the system will be able to extract the CID information. This stage also utilizes an LM-324 as the gain element.

The controlling equations for the gain stage follow.

$$Gain = \frac{Rfb}{Rin}$$

Rfb: is the resistor connected from the output to the inverting input of the operational amplifier.

Rin: is the resistor from the signal source to the inverting input of the amplifier.

PLL, FSK DECODER

The fourth stage (see *Figure 6*) of the demo-board design is the FSK decoder and Carrier detect stage. This stage tracks the phone line signal that passes through the bandpass filter stage. This stage performs two tasks. First it simply detects if a frequency exists in a specific band. If so, the Energy Detect signal becomes active. Second it demodulates the 1300 baud FSK modulation of a frequency in the band from 1200Hz to 2100Hz. This

demodulated data constitutes the CID information modulated by the CO. Note that Energy Detect must be valid before any CID information can be considered valid. This stage utilizes the XR-2211 PLL to perform this function. The XR-2211 center VCO frequency should be adjusted by use of a potentiometer to a geometric mean frequency of 1625 Hertz.

A note, while it was not done in this demo-board design it may be possible to eliminate the amplifier in the filter stage and utilize the XR-2211 as the principal gain stage. This may require extracting more gain from the filter stages or running the risk of not having enough sensitivity to process low level, -48 (dBm), signals. Equations for PLL calculations follow:

$$C0 = \frac{1}{f0 * R0}$$

$$f0 = \frac{f1 + f2}{2}$$

f1,f2: are the mark and space frequencies.

R0: is the frequency control resistor connected at pin 12 of XR-2211.

$$R1 = \frac{f0 * R0 * 2}{f2 - f1}$$

R1: is the resistor connected from pin 12 to pin 11.

$$\varsigma = \sqrt{\frac{1.25 * C0}{R1 * C1}}$$

ς : is the Damping Factor. R1 in KOhms.

$$V_{REF} = \frac{V_{CC}}{2} - .650$$

V_{REF}: is the reference voltage at pin 10.

$$K_0 = \left| \frac{2 * \pi}{V_{REF} * C0 * R1} \right|$$

K0: VCO Conversion Factor in Radians per second per volt.

$$K_d = \frac{V_{REF} * R1}{10 * \pi}$$

Kd: Phase Detector Gain in Volts per Radian. R1 in KOhms.

For more information on choosing components for use with the XR-2211 in an FSK application, contact EXAR and ask for the XR-2211 Application Program and Application Note.

TONE ALERT DETECT

In the BT version an additional tone alert decoding function, requiring an additional XR-2211 is incorporated into the demo board design. This tone decoder detects a 2130Hz +/- 100Hz signal that lasts for at least 30 ms. BT CO's use tone Alert to put the demo board on notice that CID information is about to be sent. Since BT CO's routinely perform line reversal for their own testing purposes, it makes it necessary that a Tone Alert signal also be sent to ensure that the CID information is in fact about to be sent. While the Line Reversal is powered up at all times, the Tone Alert circuitry is powered up only after a Line Reversal condition.

RS-232 ENCODER

The fifth stage of the demo board consists of a MAXIM-235. The 235 takes the decoded data provided by the XR-2211 and converts the voltage level provided by the XR-2211 to a level that is required by the RS-232 port of the PC.

To ensure proper operation, the RS-232 registers contained within the PC must be available in a timely manner to be able to begin downloading the CID information stream. An extremely slow computer can cause problems, it will look as if there is a problem with the demo board design. It is recommended that a CPU, with a faster clock frequency, be tried if this occurs.

Once the board detects a line reversal the Carrier Detect signal becomes active and sends information to the PC through the RS-232 interface, then the PC program responds by turning on the unpowered part of the board, again using the RS-232 interface. Then the system is ready to process the information sent by CO.

After receiving the data the program will perform the checksum test. It will turn off the originally unpowered section of the demo-board and will show on the screen the CID data or a message if the transmission was unsuccessful.

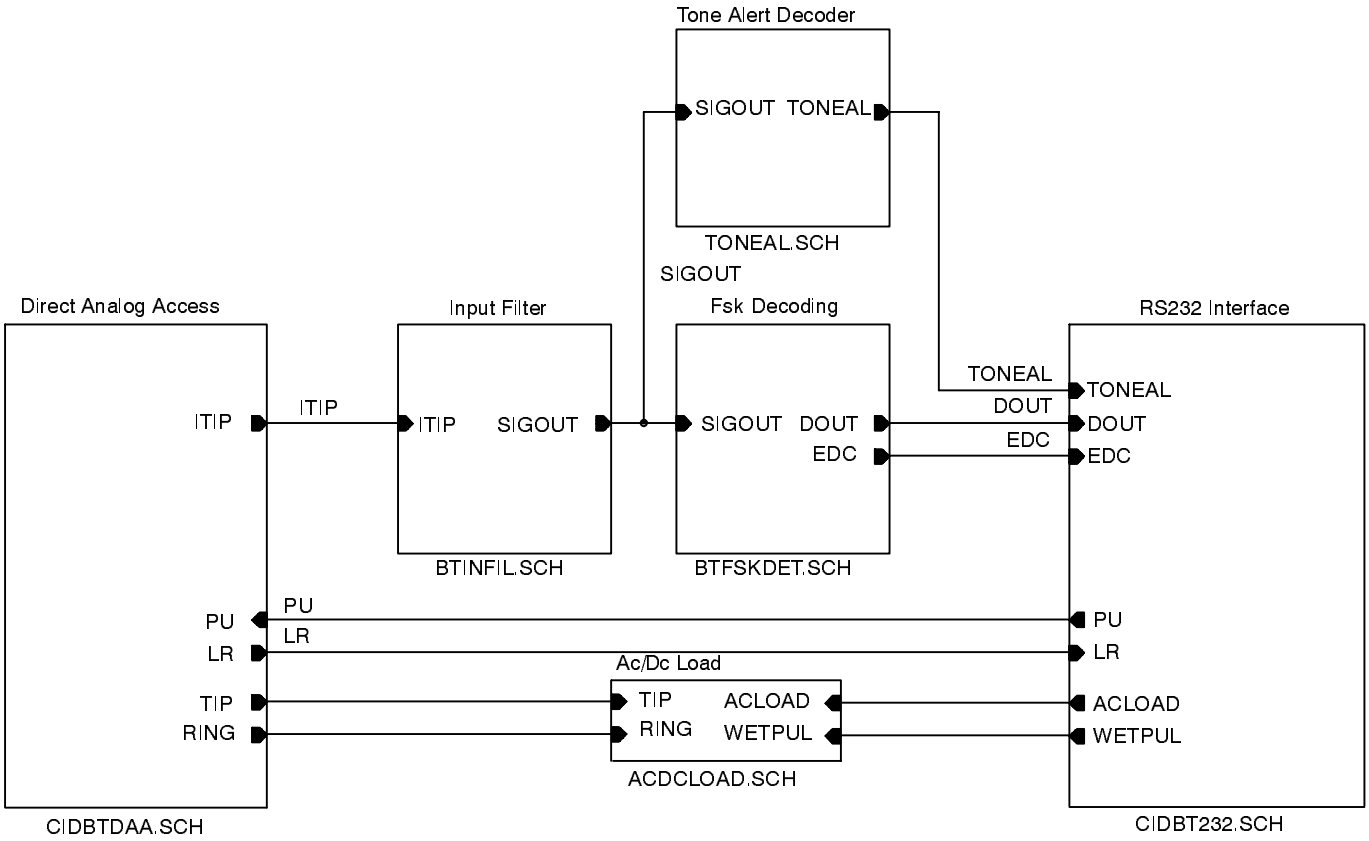


Figure 3. CID for the BT Using XR-2211

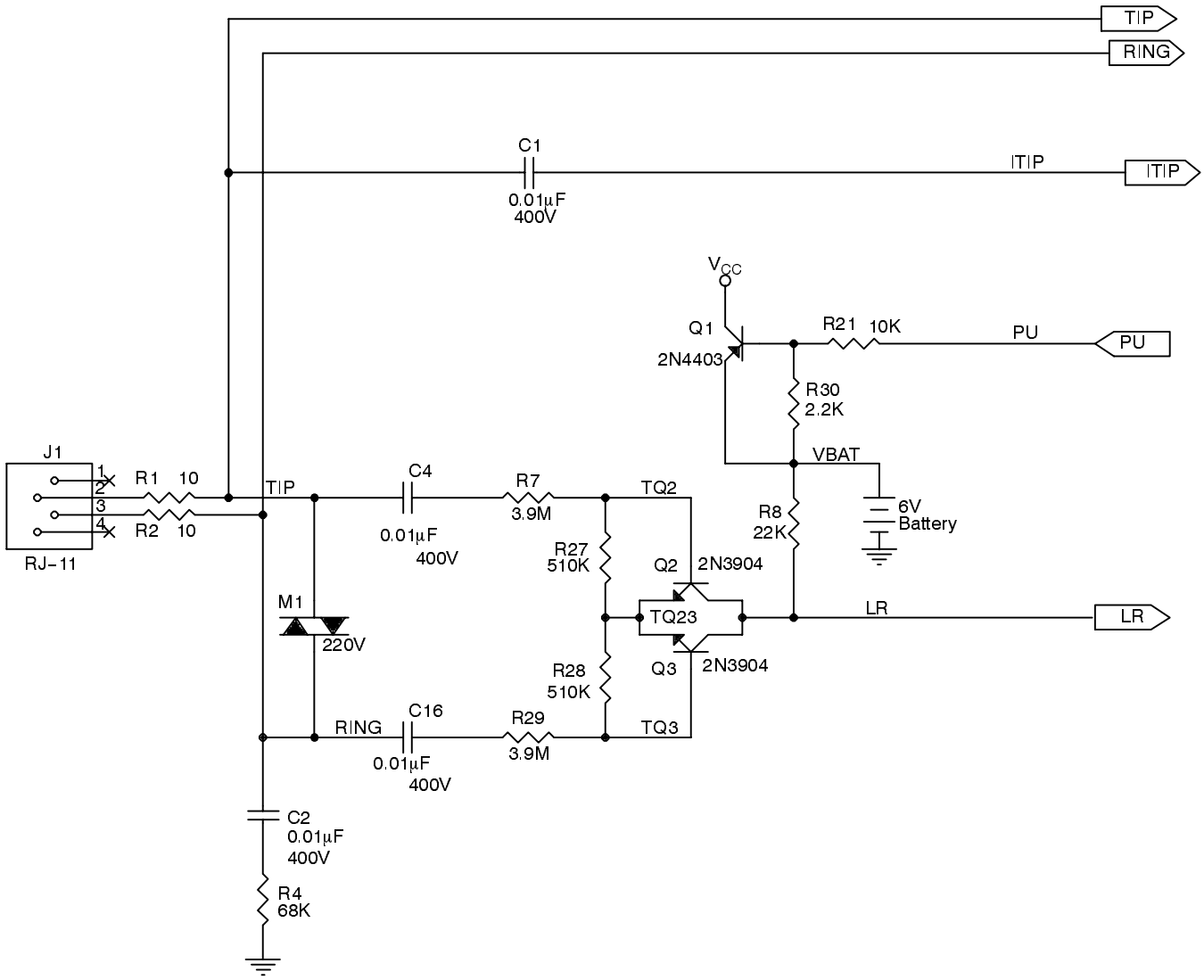


Figure 4. DAA for B.T.

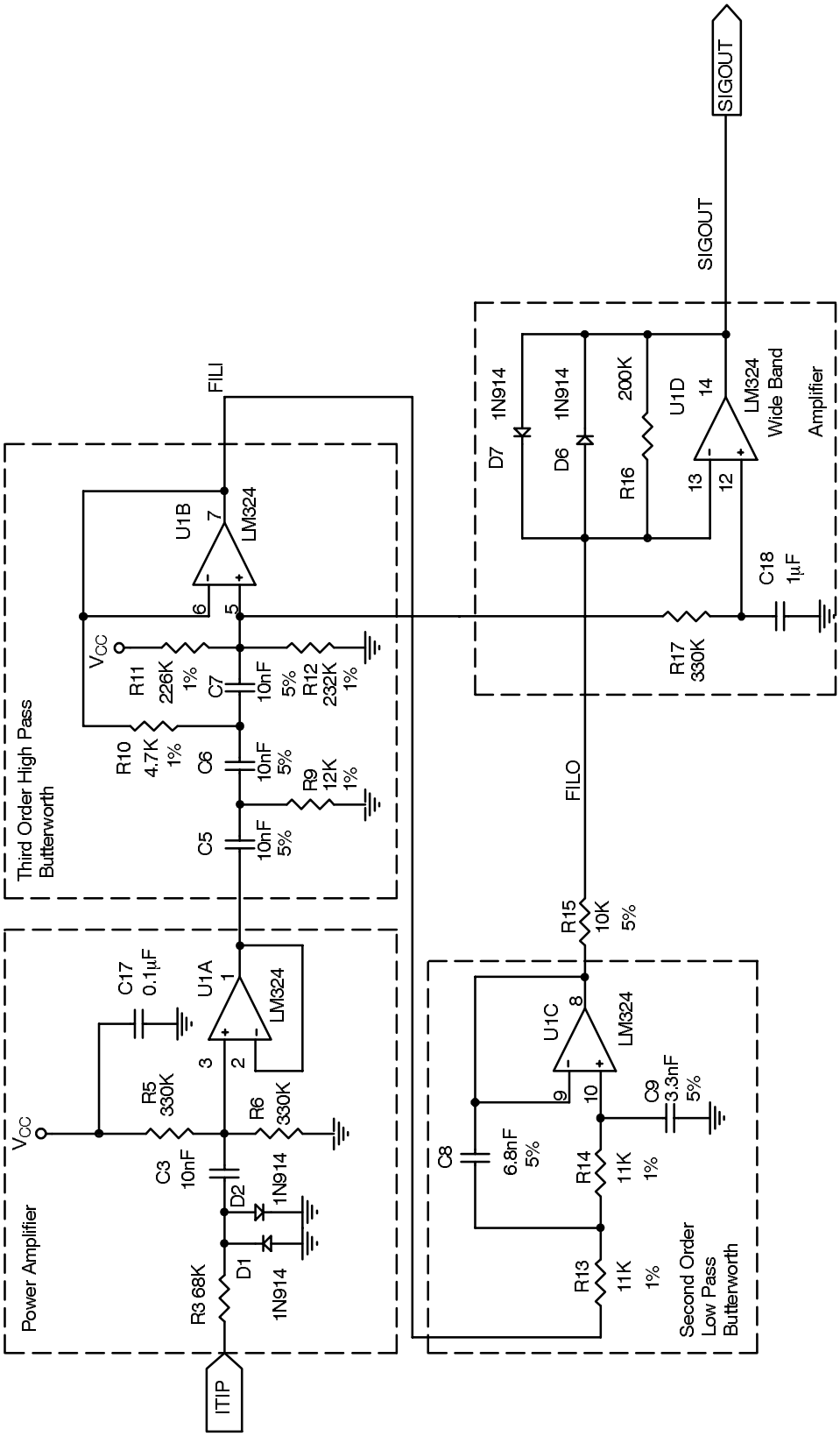


Figure 5. Input Filter for B.T. Implementation

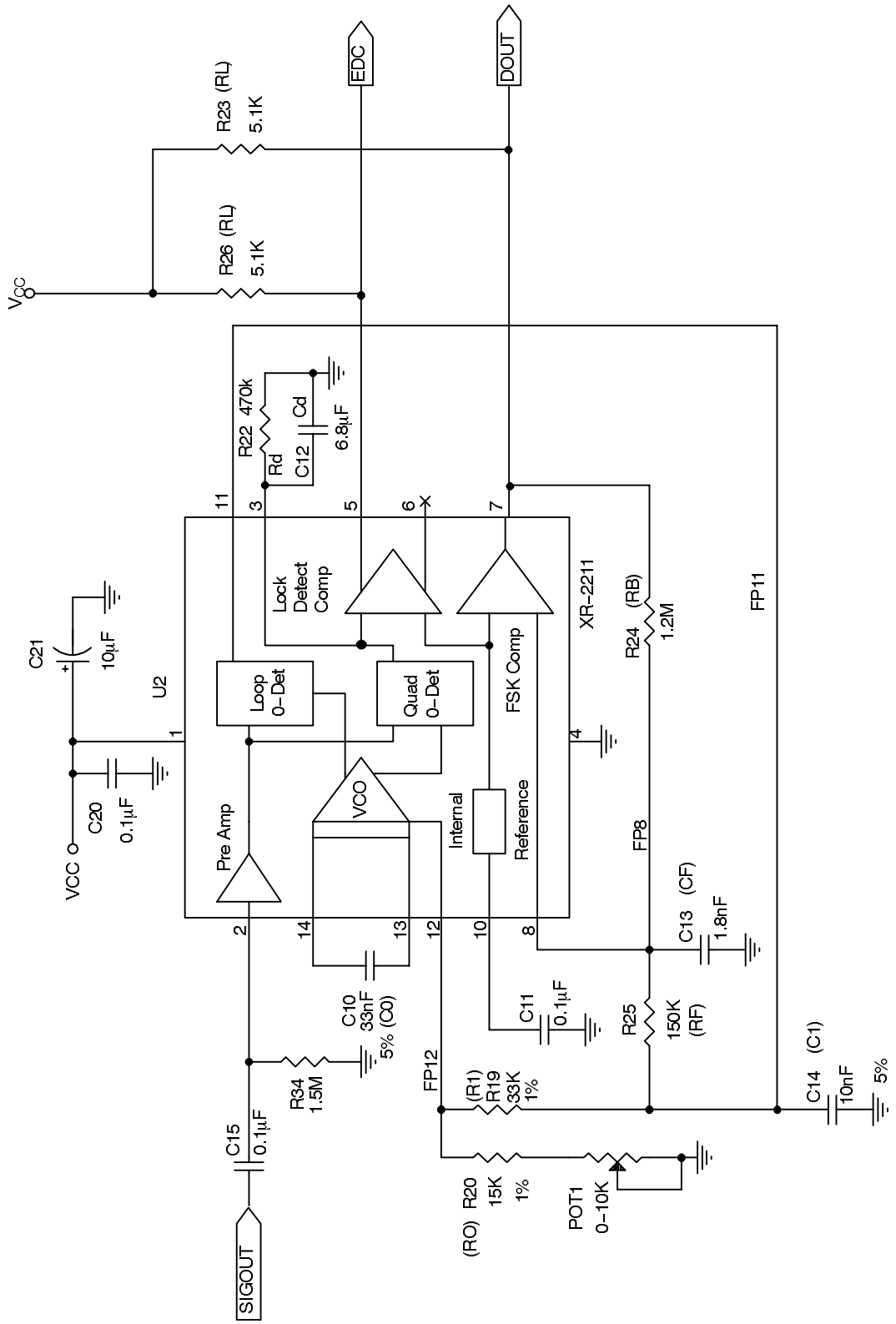


Figure 6. FSK Demodulator

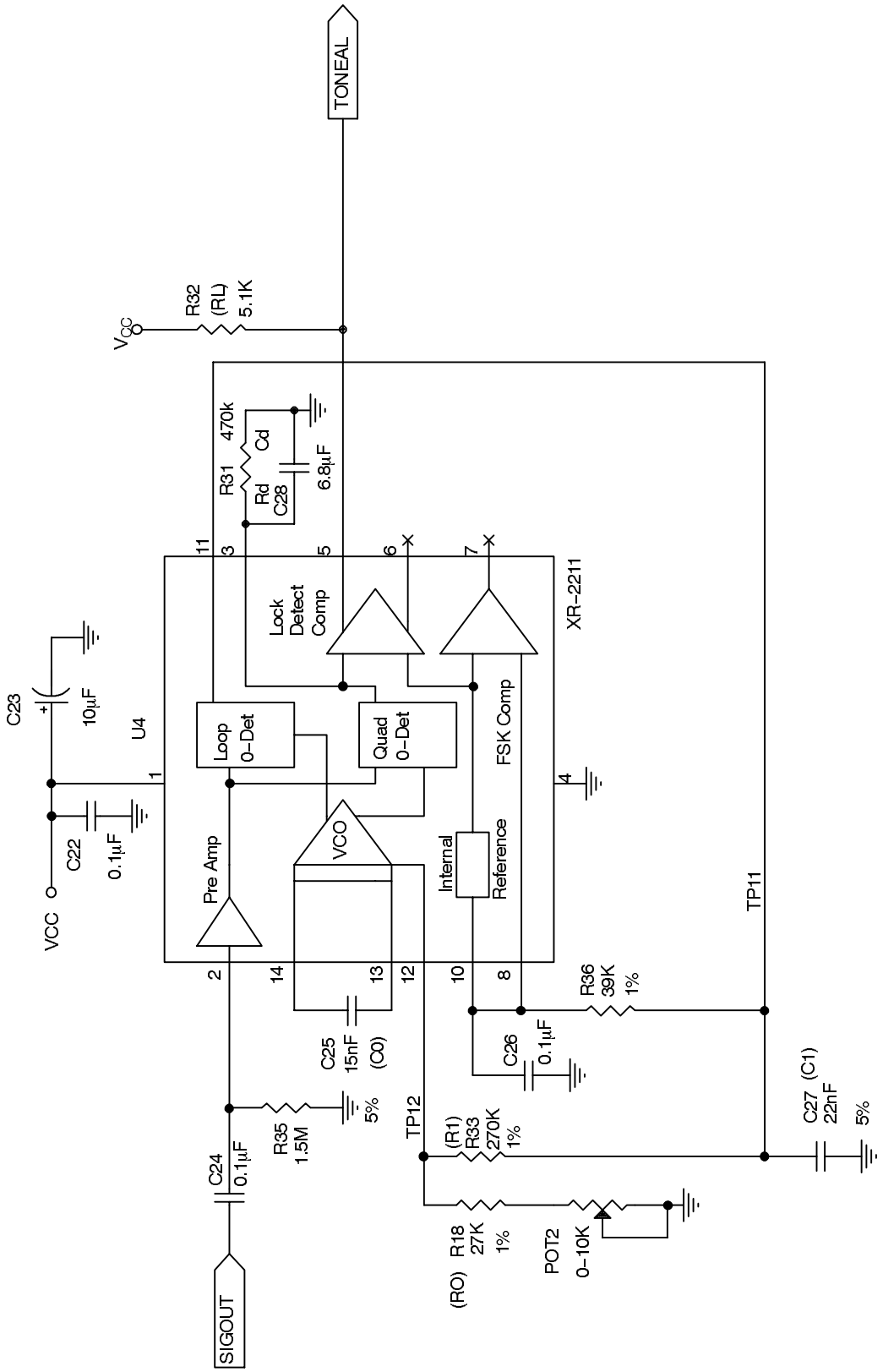


Figure 7. Tone Alert Decoder

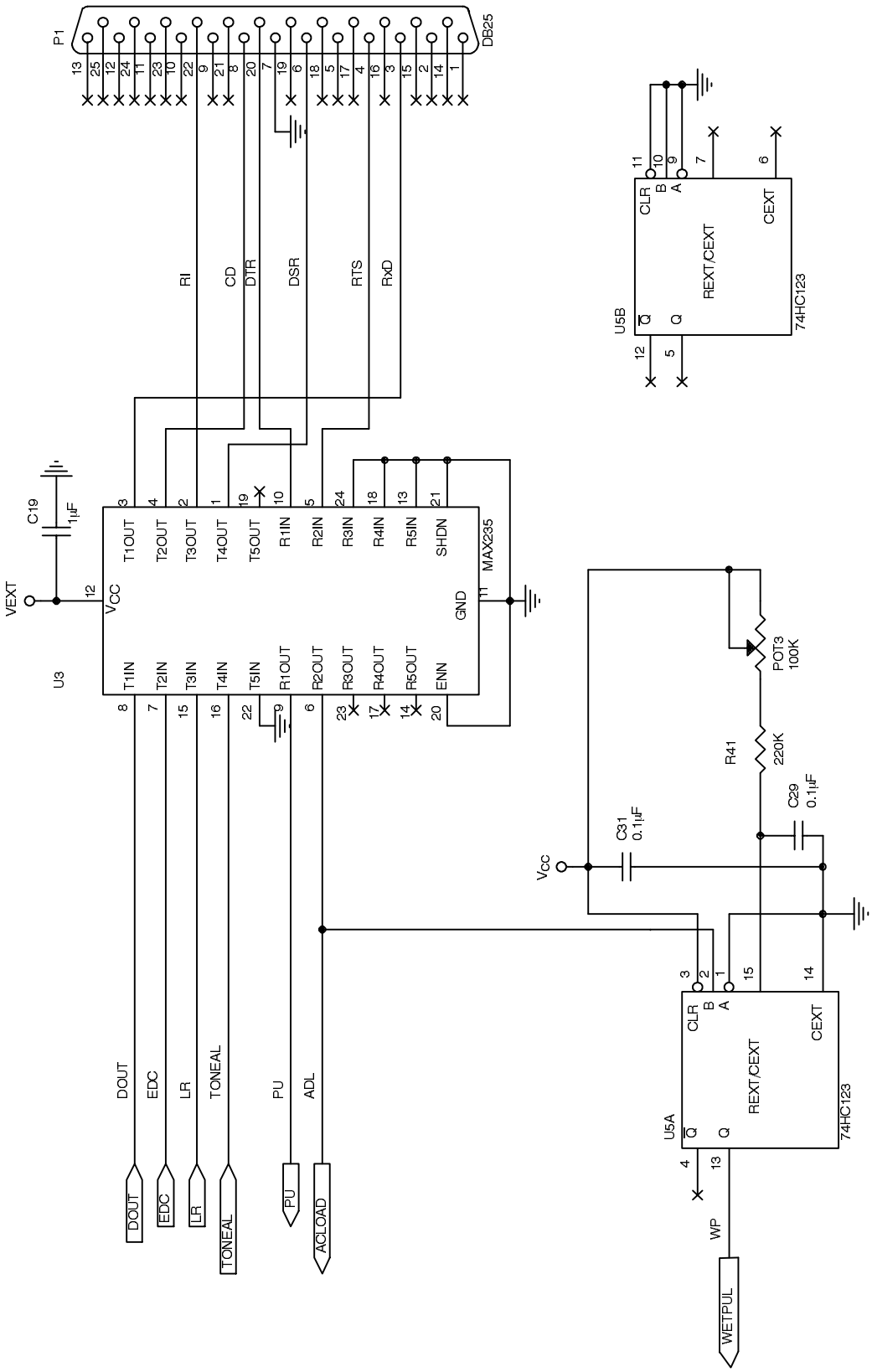


Figure 8. RS232 Interface for CID B.T.

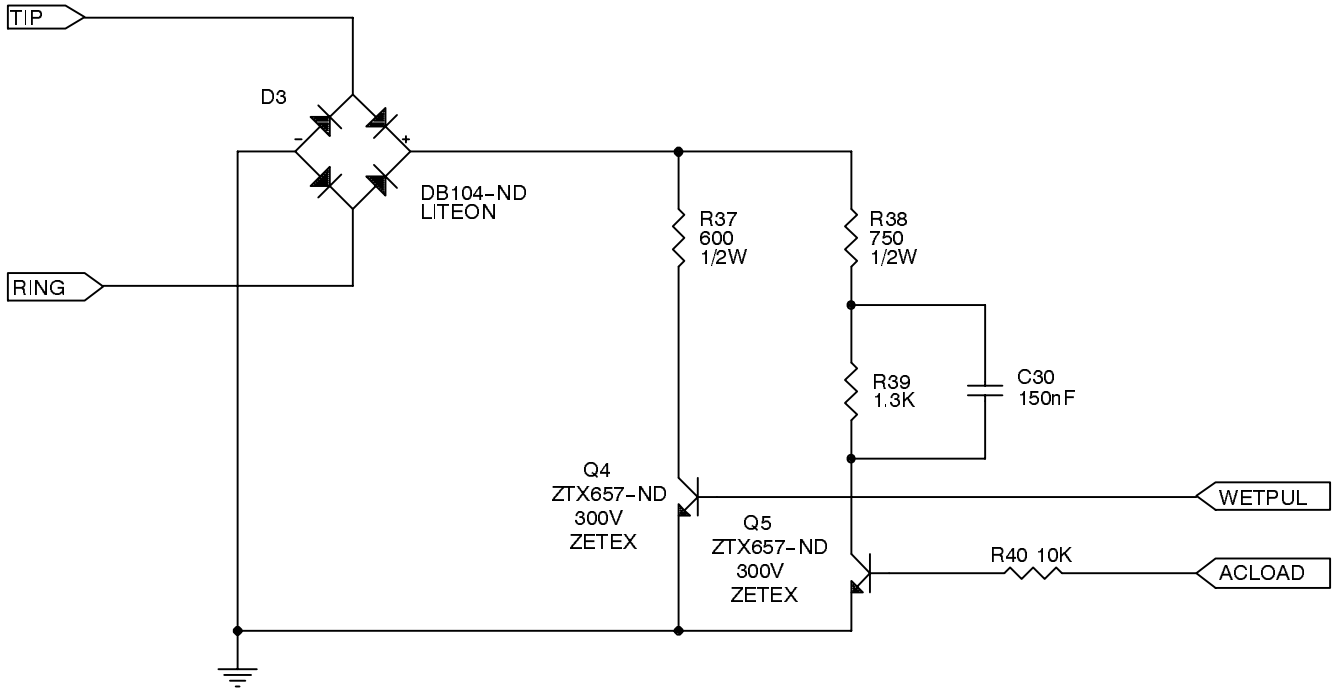
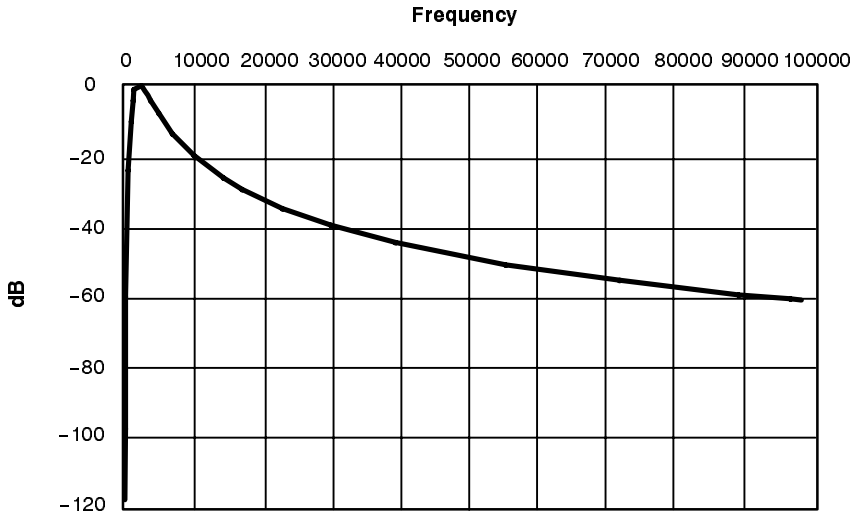
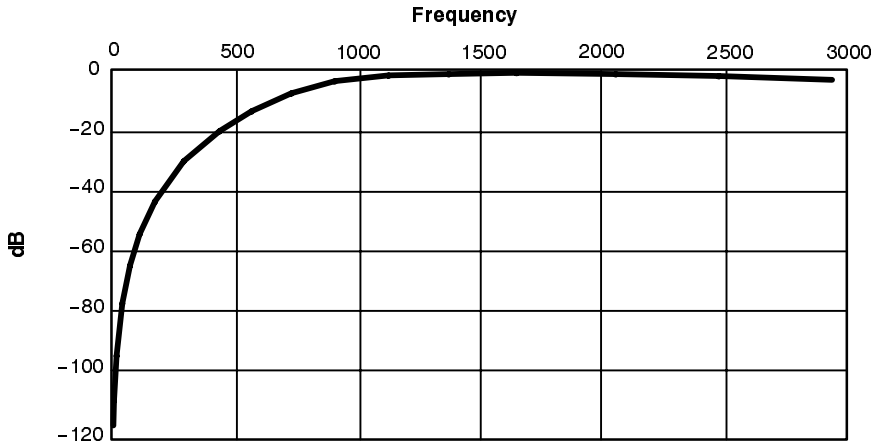


Figure 9. AC/DC Load and Wetting Pulse

A)



B)



C)

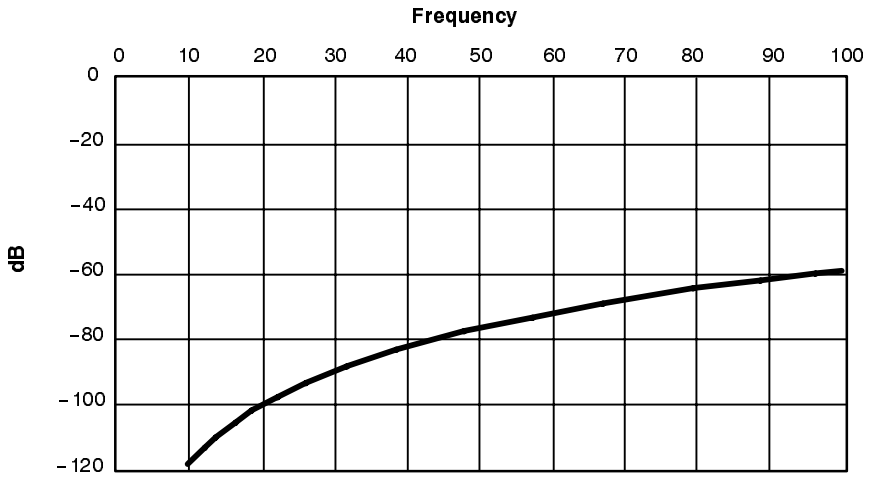


Figure 10. Frequency Response of Input Signal

BILL OF MATERIALS

DAA FOR B.T.

Item	Quantity	Reference	Part	Tolerance
1	4	C1,C2,C4,C16	0.01µF	400V
2	1	J1	RJ-11	
3	1	M1	MOV	220V
4	1	Q1	2N4403	
5	2	Q2,Q3	2N3904	
6	2	R1,R2	10	0.5W
7	1	R4	68K	
8	2	R7, R29	3.9M	
9	1	R8	22K	
10	1	R21	10K	
11	2	R27,R28	510K	
12	1	R30	2.2K	
13	1	6V	BATTERY	

Input Filter for BT Implements

Item	Quantity	Reference	Part	Tolerance
1	1	C3	10nF	
2	3	C5,C6,C7	10nF	5%
3	1	C8	6.8nF	5%
4	1	C9	3.3nF	5%
5	1	C17	0.1UF	
6	1	C18	1uF	
7	2	D1,D2,D6,D7	1N914	
8	1	R3	68K	
9	3	R5,R6,R17	330K	
10	1	R9	12K	1%
11	1	R10	4.7K	1%
12	1	R11	160K	1%
13	1	R12	180K	1%
14	2	R13,R14	11K	1%
15	1	R15	10K	1%
16	1	R16	200K	
17	1	U1	LM324	

BILL OF MATERIALS (CONT'D)

FSK Demodulator

Item	Quantity	Reference	Part	Tolerance
1	1	C10	33nF	5%
2	3	C11,C15,C20	0.1uF	
3	1	C12	68nF	
4	1	C13	1.5nF	5%
5	1	C14	10nF	5%
6	1	C21	10uF	
7	1	POT1	0-10K	
8	1	R19	33K	1%
9	1	R20	15K	1%
10	1	R22	470k	
11	2	R23,R26	5.1K	
12	1	R24	1.2M	
13	1	R25	150K	
14	1	R34	1.5M	
15	1	U2	XR-2211	

RS232 Interface for CID B.T.

Item	Quantity	Reference	Part
1	1	C19	1µF
2	2	C23,C31	0.1µF
3	1	POT3	100K
4	1	P1	DB25
5	1	R41	220K
6	1	U3	MAX235
7	1	U5	74HC123

AC/DC Load and Wetting Pulse

Item	Quantity	Reference	Part	Tolerance
1	1	C30	150nF	
2	1	D3	DB104-ND	
3	2	Q4,Q5	ZTX657-ND	300V
4	1	R37	600	1/2V
5	1	R38	750	1/2V
6	1	R39	1.3K	
7	1	R40	10K	

BILL OF MATERIALS (CONT'D)

Tone Alert Decoder

Item	Quantity	Reference	Part	Tolerance
1	3	C22,C24,C26	0.1µF	
2	1	C23	10µF	
3	1	C25	15nF	5%
4	1	C27	22nF	5%
5	1	C28	6.8µF	
6	1	POT2	1-10K	
7	1	R18	27K	1%
8	1	R31	470K	
9	1	R32	5.1K	
10	1	R33	270K	1%
11	1	R35	1.5K	
12	1	R36	39K	1%
13	1	U4	XR-2211	

NET LIST OF BOARD

/FILI-3	R10(2) U1(6) U1(7) R13(1);
/N00002	R10(1) C6(2) C7(1);
/N00003	R5(2) C3(2) U1(3) R6(1);
/N00004	R3(2) D1(CATHODE) D2(ANODE) C3(1);
/N00005	R11(2) C7(2) R17(1) R12(1) U1(5);
/N00006	U1(1) U1(2) C5(1);
/N00007	C5(2) R9(1) C6(1);
/N00008	C8(1) R13(2) R14(1);
/N00008	C8(1) R13(2) R14(1);
/N00009	C8(2) U1(9) U1(8) R15(1);
/FILO-3	R15(2) D7(CATHODE) D6(ANODE) R16(1) U1(13);
/N00011	R14(2) C9(1) U1(10);
/N00012	R17(2) U1(12) C18(1);
/TP11-5	R36(2) R33(2) C27(1) U4(11);
/N00014	C24(2) R35(1) U4(2);
/N00015	U4(3) C28(1) R31(1);
/N00016	U4(14) C25(2);
/N00017	C25(1) U4(13);
/TP12-5	R18(1) R33(1) U4(12);
/N00019	C26(1) U4(8) U4(10) R36(1);
/N00020	R18(2) POT2(B);
/N00021	R19(2) R25(1) U2(11) C14(1);
/N00022	C15(2) R34(1) U2(2);
/N00023	U2(3) C12(1) R22(1);
/N00024	U2(14) C10(2);
/N00025	C10(1) U2(13);
/FP12-4	R20(1) R19(1) U2(12);
/N00027	U2(10) C11(1);
/N00028	R20(2) POT1(B);
/FP8-4	U2(8) R25(2) C13(1) R24(1);
/RDX-6	U3(3) P1(3);
/CD-6	U3(4) P1(8);

/RI-6	U3(2) P1(22);
/DSR-6	U3(1) P1(6);
/DTR-6	U3(10) P1(20);
/RTS-6	U3(5) P1(4);
/N00036	U5(15) C29(1) R41(2);
/N00037	R41(1) POT3(A);
/N00038	Q1(BASE) R30(1) R21(1);
/VBAT-2	R30(2) Q1(EMITTER) 6V(+) R8(1);
/N00040	J1(2) R1(1);
/N00041	C4(2) R7(1);
/TQ2-2	R7(2) R27(1) Q2(BASE);
/N00043	J1(3) R2(1);
/TQ23-2	Q2(EMITTER) R27(2) R28(1) Q3(EMITTER);
/TQ3-2	R28(2) R29(2) Q3(BASE);
/N00046	C16(2) R29(1);
/N00047	C2(1) R4(1);
/N00048	D3(+DC) R37(1) R38(1);
/N00049	R37(2) Q4(COLLECTOR);
/N00050	R38(2) C30(1) R39(1);
/N00051	C30(2) R39(2) Q5(COLLECTOR);
/N00052	Q5(BASE) R40(1);
/SIGOUT-1	D7(ANODE) D6(CATHODE) R16(2) U1(14) C24(1) C15(1);
/TONEAL-1	R32(2) U4(5) U3(16);
/ITIP-1	R3(1) C1(1);
/DOUT-1	U2(7) R24(2) R23(2) U3(8);
/EDC-1	R26(2) U2(5) U3(7);
/PU-1	U3(9) R21(2);
/LR-1	U3(15) R8(2) Q2(COLLECTOR) Q3(COLLECTOR);
/N00060	U5(2) U3(6) R40(2);
/N00061	U5(13) Q4(BASE);
/N00062	C1(2) R1(2) R2(2) C4(1) C2(2) C16(1) D3(AC1) D3(AC2);

NET LIST OF BOARD (CONT'D)

/VCC	U1(4) R11(1) C17(2) R5(1) R32(1) C22(1) U4(1) C23(1), C20(1) U2(1) C21(1) R23(1) R26(1) U5(16) U5(3) POT3(WIPER), POT3(B) C31(1) Q1(COLLECTOR);
/GND	C18(2) C9(2) R12(2) R9(2) R6(2) D2(CATHODE) D1(ANODE) U1(11), C17(1) C27(2) POT2(A) POT2(WIPER) U4(4) C26(2) R35(2) R31(2), C28(2) C22(2) C23(2) C14(2) C13(2) POT1(A) POT1(WIPER) U2(4), C11(2) R34(2) R22(2) C12(2) C20(2) C21(2) U5(1) U5(14), C31(2) C29(2) U5(11) U5(10) U5(9) U5(8) U3(11) U3(20), U3(24) U3(18) U3(13) U3(21) P1(7) U3(22) C19(2) R4(2), 6V(-) Q4(EMITTER) D3(-DC) Q5(EMITTER);
/VEXT	C19(1) U3(12)

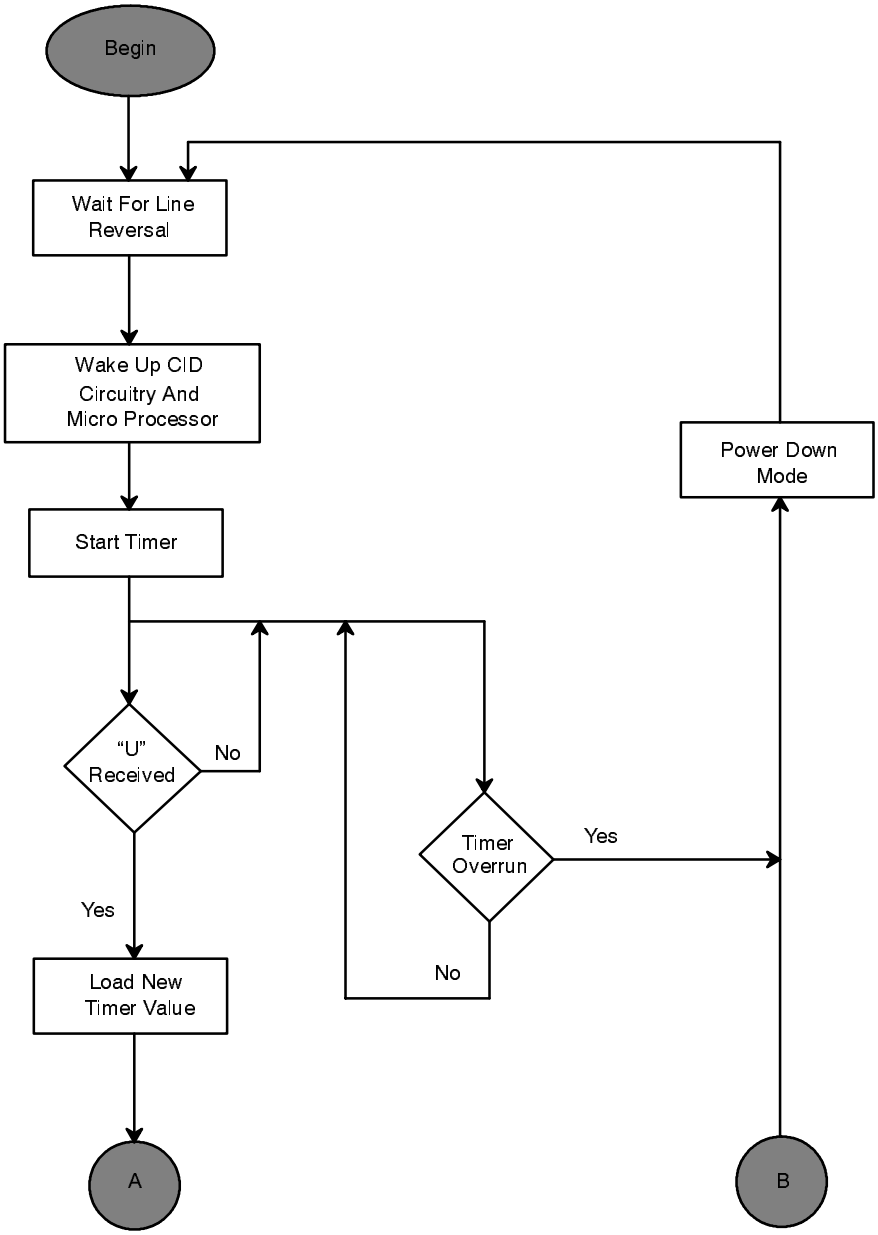


Figure 12. Micro Controller Firmware Flow Chart

The following pages are a description in the form of a flow chart, of a typical program that handles a Caller Identification Delivery Recovery.

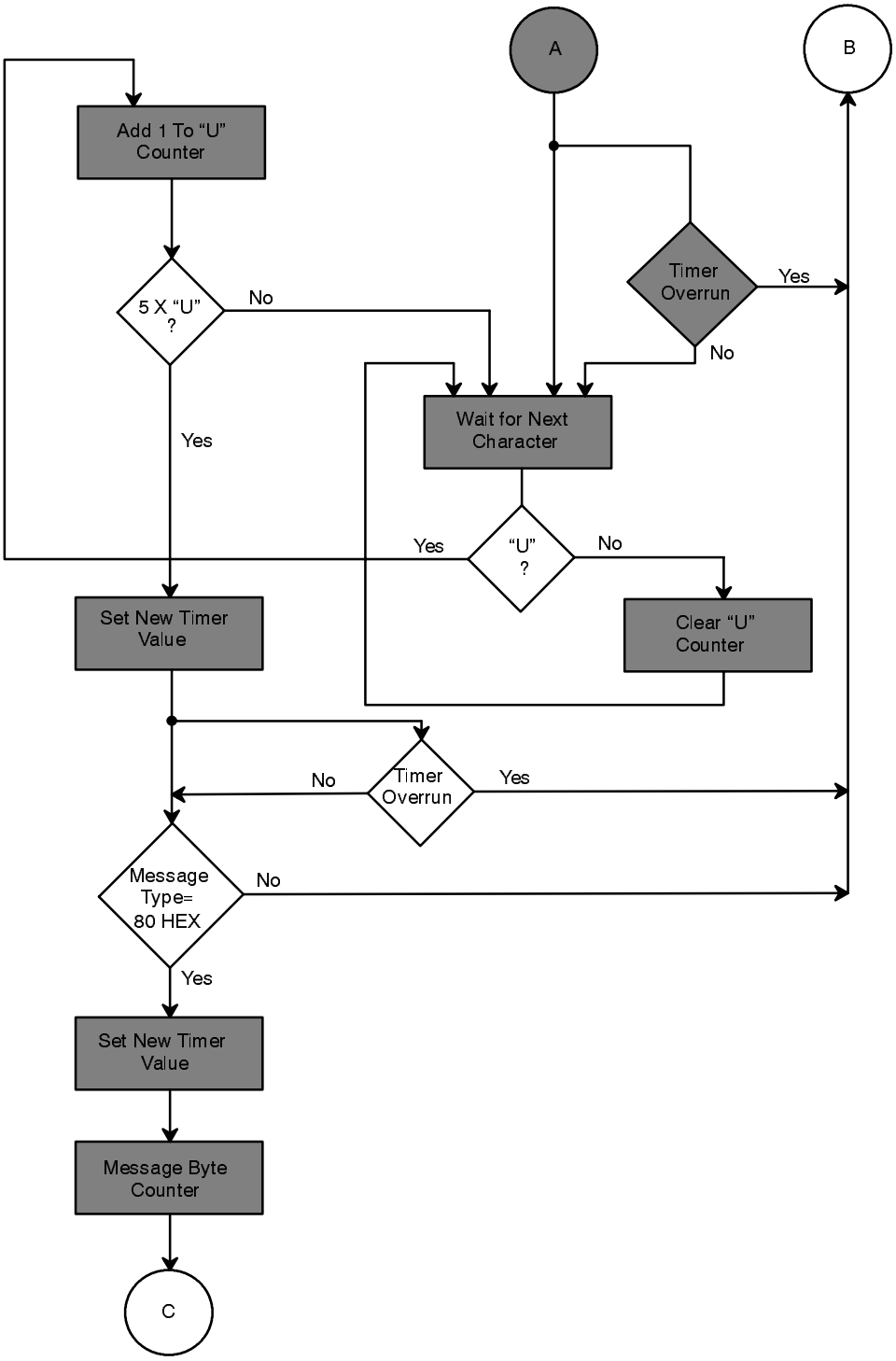


Figure 13. Flow Chart for Caller ID Processing (Con't)

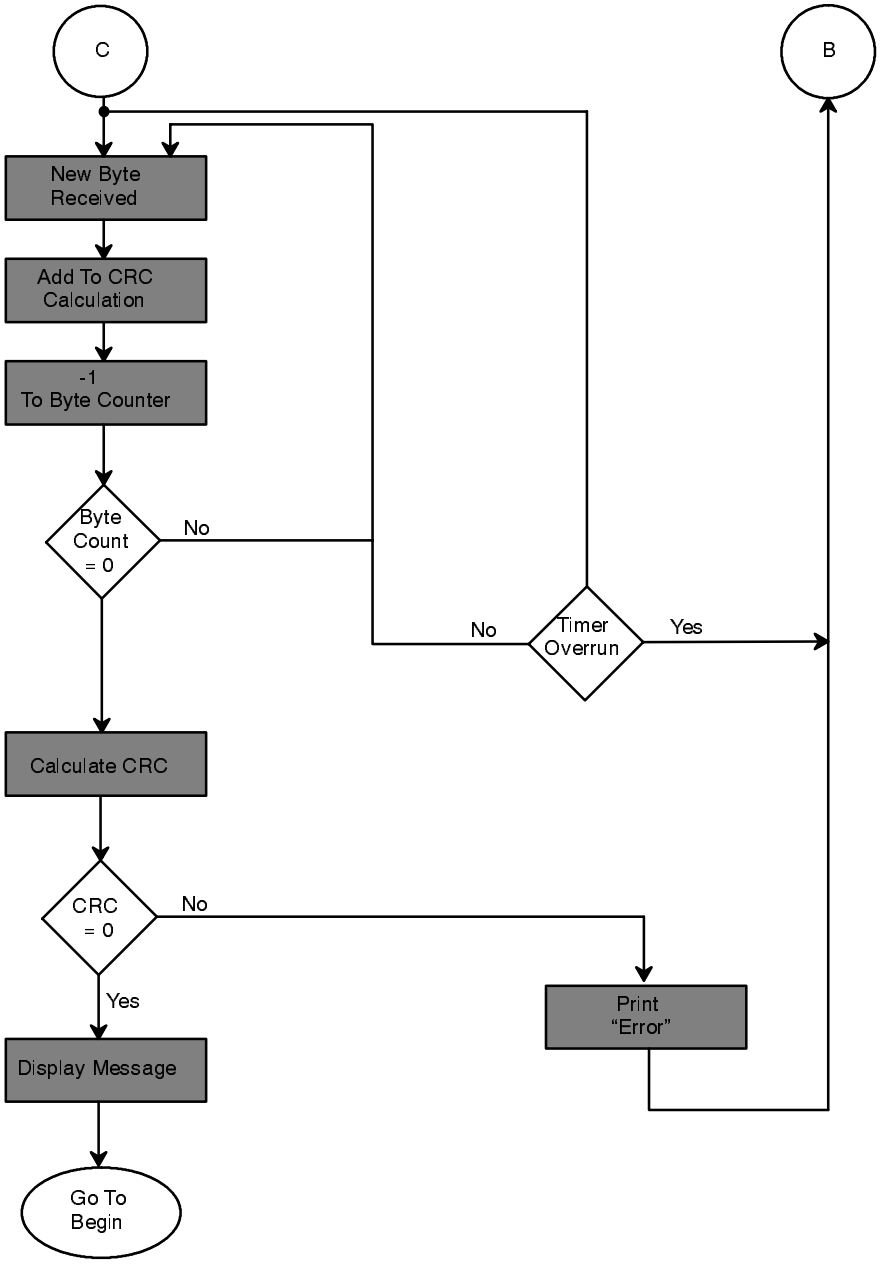


Figure 14. Flow Chart for Caller ID Processing (Cont'd)

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