
# Power Management Solutions for Xilinx® FPGAs/SoCs

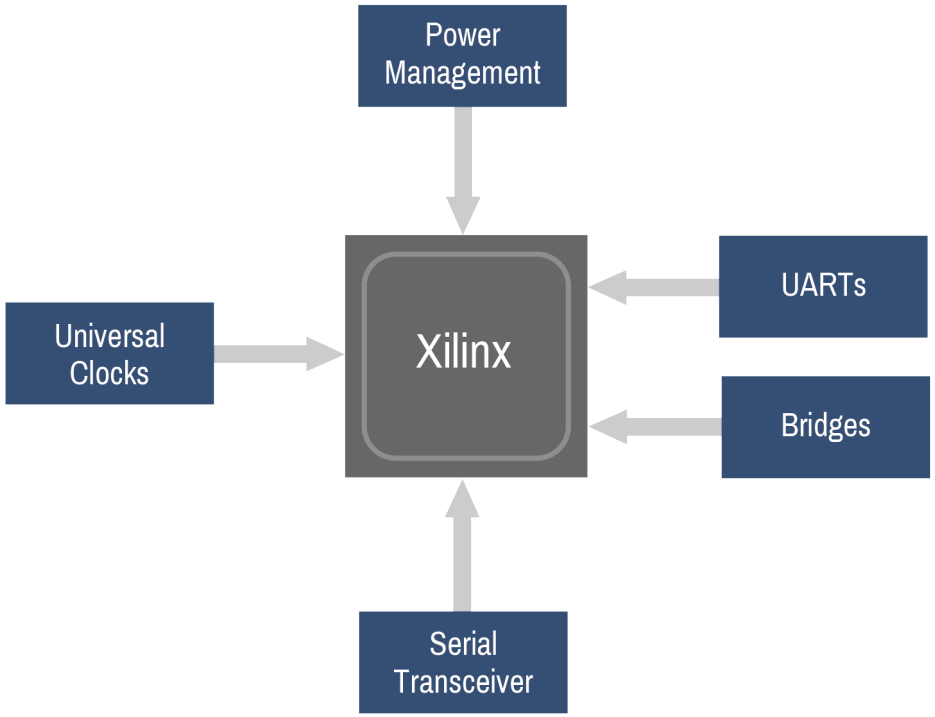
April 2019

UltraSCALE™ Architecture

XILINX ALL PROGRAMMABLE™

ENVISIONING ▪ EMPOWERING ▪ EXCELLING

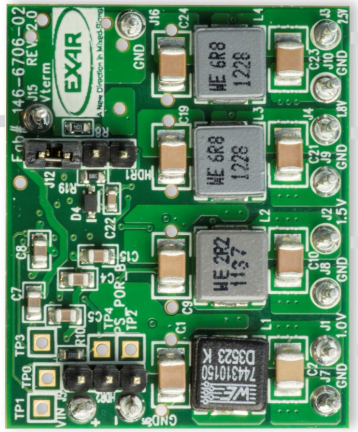
# Power Management & Analog Solutions for Xilinx Zynq® and Zynq® UltraScale+™ FPGAs




- Xilinx reference designs
  - Zynq-7000
  - Zynq-7020
  - Zynq UltraScale+ MPSoCs
    - Zynq UltraScale+
    - Zynq UltraScale+ (No MGTs)
  - Zynq UltraScale+ ZU2, ZU3

# Xilinx Zynq-7000 All Programmable SoC Power System

**XRP7714**
**Reference Design**



**Xilinx® Zynq®-7000 SoC**

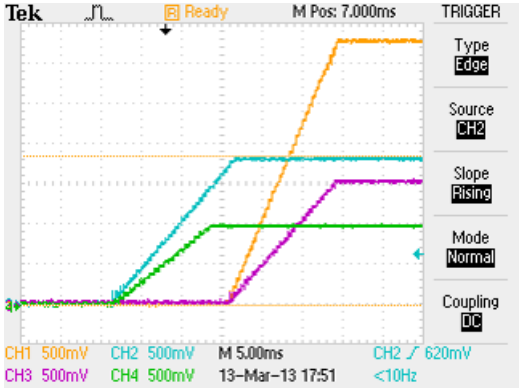
- 2.5V I/O
- 1.8V VCCAUX, VCCPLL
- 1.5V DDR3
- 1.0V VCCINT, VCCBRAM, VCCPINT

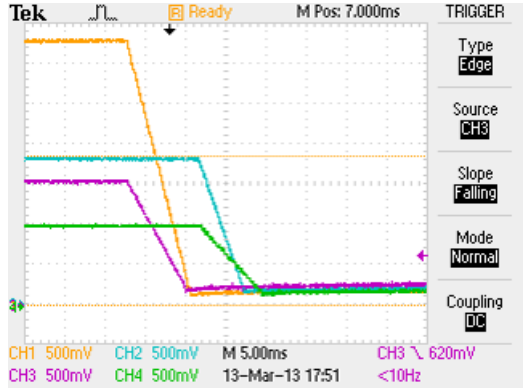
0.75V Vterm for DDR3 SDRAM

4 GPIO signals can be programmed to provide status of PGOOD signals, enables and faults or as I/O expansion

- Powers Zynq 7000 in 1.875 $in^2$
- I2C programmable output voltage, Switching Frequency, Sequencing, and Fault Management
- Dynamic Voltage Scaling

Order and Ramp rates for each supply meet Zynq-7000 requirements



# Zynq 7000 Reference Material

- Application Note ANP-41
- Zynq EVB Configuration File
- OrCAD and PADS Design Files
- and more…

Visit: www.exar.com/products/zyqn-evb

XILINX
ALL PROGRAMMABLE.

Xcell Daily Blog

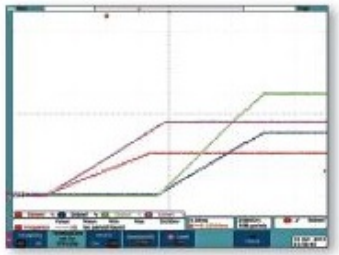
## Reference Design Powers Zynq SoC in 1.875 Square Inches

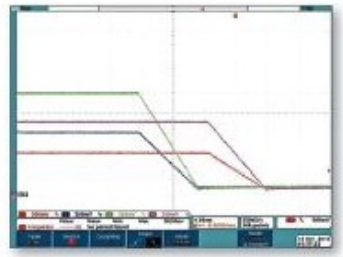
by Steve Leibson
Director of Strategic Marketing and Business Planning at Xilinx

Exar has a slick little quad high-current, programmable, switching power controller IC called the XRP7714 and some recent Googling for "Zynq" uncovered an Exar reference power-supply design that uses the XRP7714 to power a Xilinx Zynq All Programmable SoC. The reference design has a board footprint of 1.875 square inches (1.50 x 1.25 inches) and it looks like (above) on the FET side.

Application note ANP-41 "Powering the Zynq-7000 All Programmable SoC with XRP7714" describes the reference design which uses the XRP7714 to supply 0.75V, 1.0V @ 5A, 1.5V @ 3A, 1.8V @ 1.5A and 2.5V @1.5A to the Zynq SoC. The XRP7714 generates these high current supplies through external switching power FETs. An Exar XRP2997 DDR-2/3 SDRAM bus termination regulator provides a 0.75V termination voltage for the SDRAM.

What makes this design somewhat unusual is the XRP7714 digital power controller's programmability. That programmability—which resides in the power controller's on-chip, non-volatile configuration memory—includes the ability to set supply voltages and to dial in independent power supply sequencing and supply-rail ramp-up and ramp-down slew rates to meet the requirements of the attached circuitry. In this case, that's the Zynq SoC. On the left below is a graphical illustration of the power-on supply voltage ramps for the Zynq SoC reference design. And on the right is the ramp-down profile for the Zynq SoC.





In addition, the XRP7714 has an I²C interface port so the host Zynq SoC can talk to the power supply, if needed, through a couple of spare I/O pins.

https://forums.xilinx.com/t5/Xcell-Daily-Blog/Reference-design-powers-Zynq-SoC-In-1-875-square-inches/ba-p/409547

# Xilinx Zynq-7020 All Programmable SoC Power System

## Industrial Ethernet Power Solution using XRP7714

**XRP7714**
**Reference Design**

**Xilinx® Zynq®-7020 SoC**

1.8V to 3.3V VCCO

1.8V VCCAUX, VCCADC

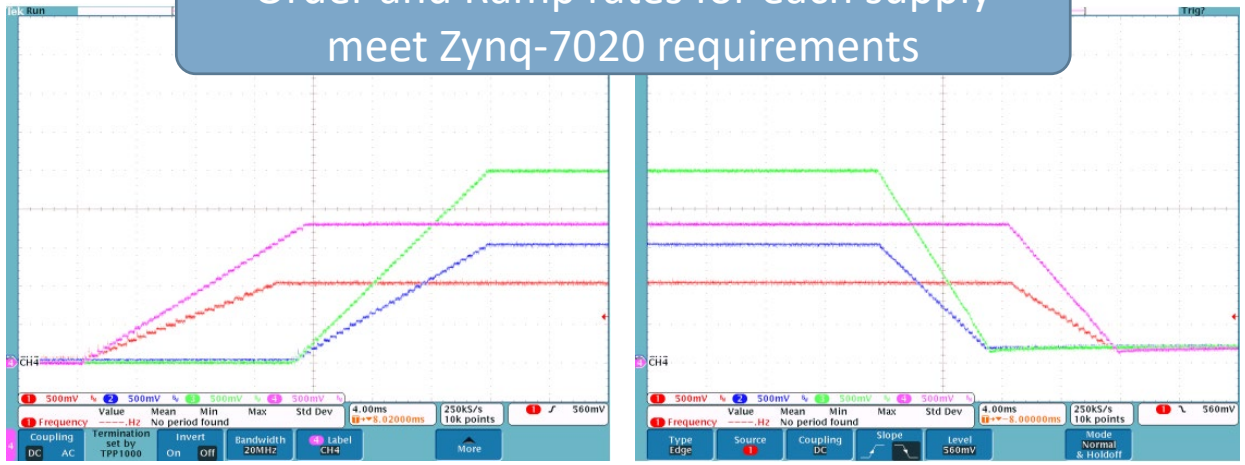
1.2/1.35/1.5V DDR3

1.0V VCCINT, VCCBRAM, VCCPINT

0.60/0.675/0.75V VTT

- Powers Zynq 7000 in 1.875 $in^2$
- I2C programmable output voltage, Switching Frequency, Sequencing, and Fault Management
- Dynamic Voltage Scaling

Order and Ramp rates for each supply meet Zynq-7020 requirements



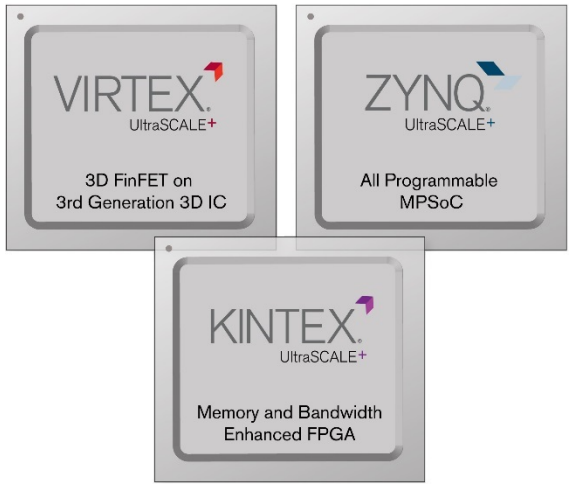
3 GPIO signals can be programmed to provide status of PGOOD signals, enables and faults

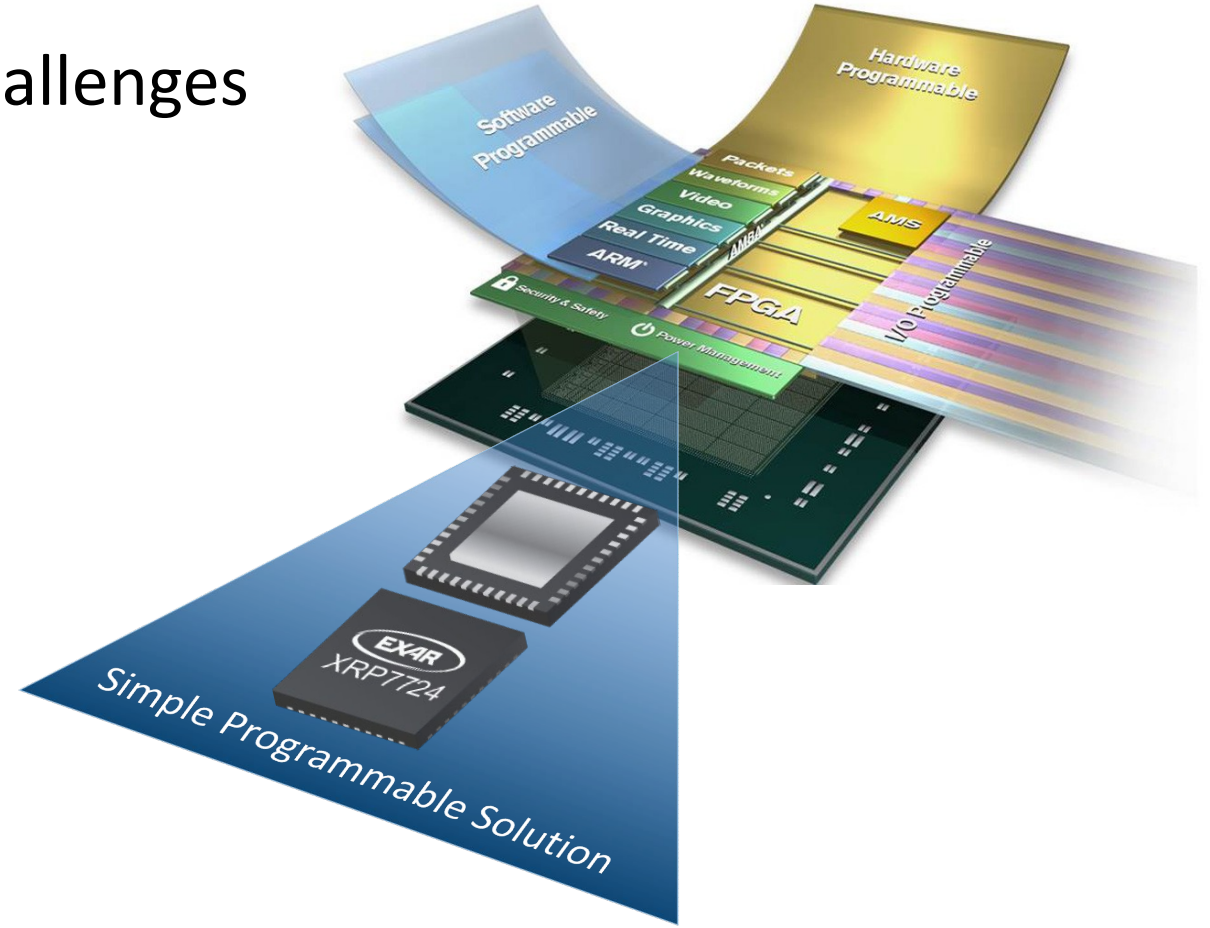
Visit: www.maxlinear.com/products/zyqn-7020

# Power Management Solutions for Xilinx UltraScale+

## Featuring the XRP7724

- Intelligent solution manages design challenges
- Easy-to-use
- Flexible solution works with whole UltraScale+ family



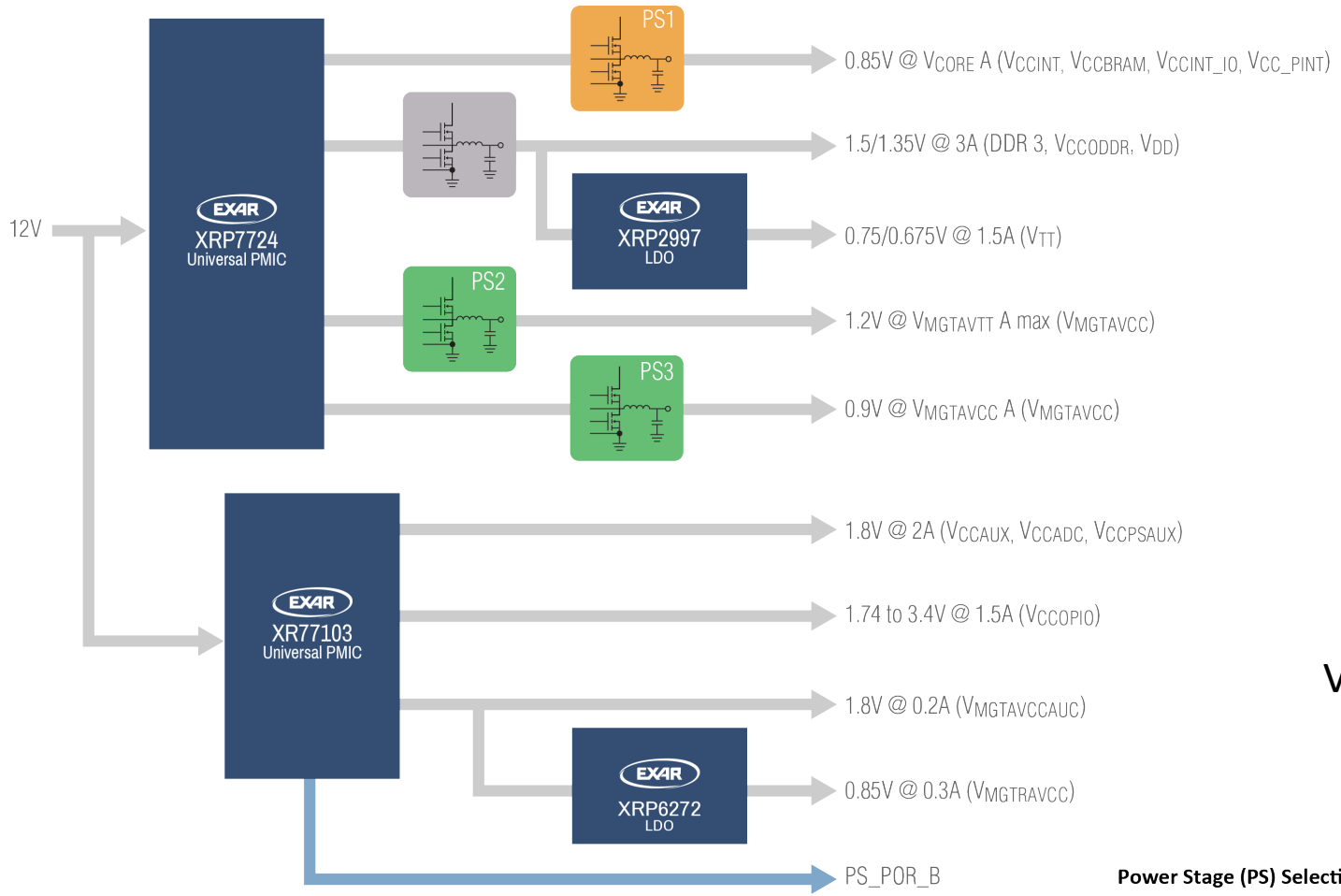








MAXLINEAR

# Scalable Zynq US + Always on Solution (UC1)



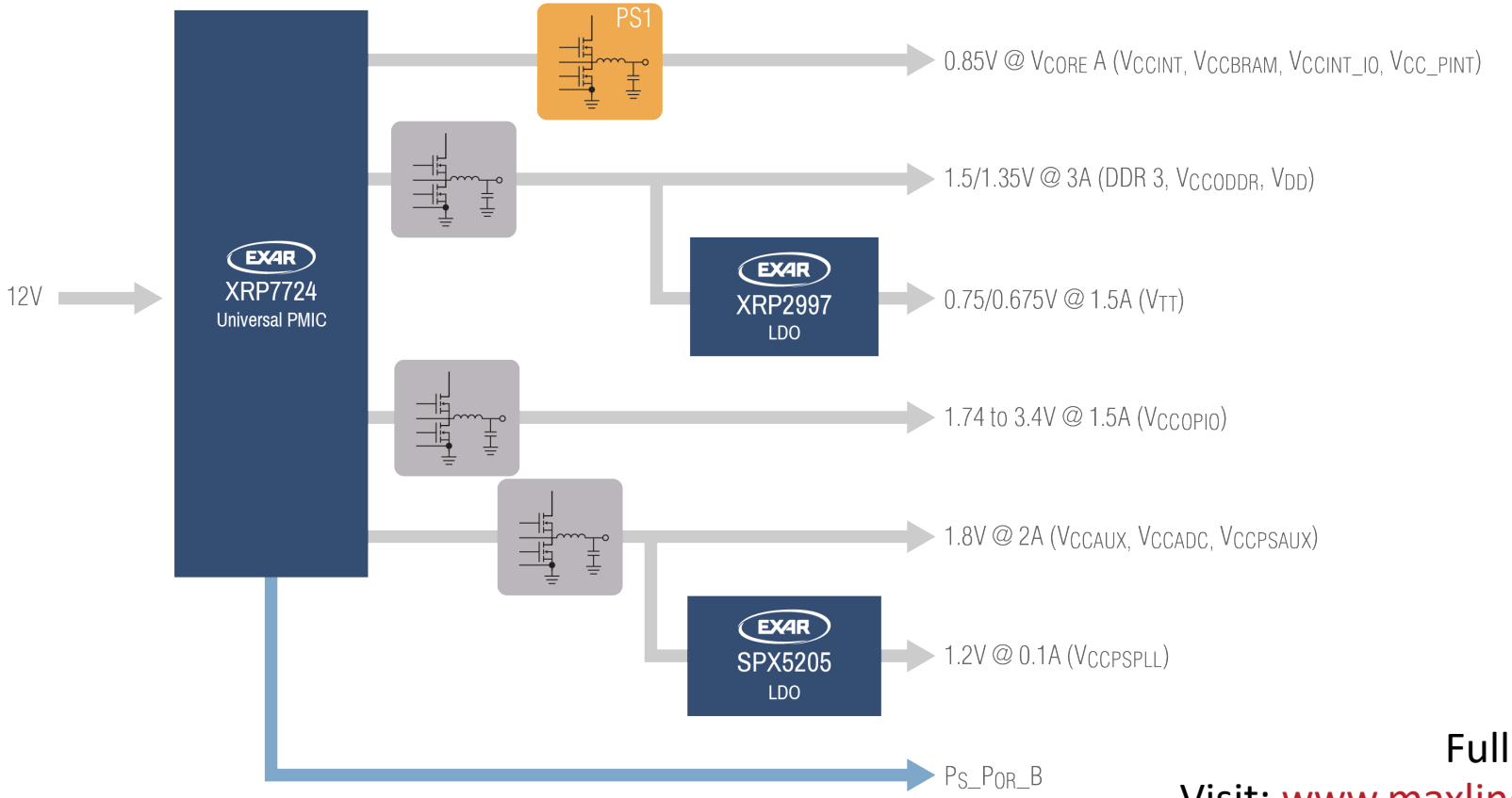

Notes:
1) XRP7724 manages sequence and dependency
2) XRP7724 provides correctly timed Ps_Por_B
3) PSU Telemetry
4) Scalable to meet full Zynq US+ Family
5) Optimized for maximum concatenation of rails

Full Schematic and BOM available
Visit: www.maxlinear.com/xilinx/zynq-ultrascale-plus

**Power Stage (PS) Selection Table**

| | | | | PS1 | | | | PS2 / PS3 | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Device | Icore (max) | Imgtavtt | Imgtavcc | Qh | Ql | L | C | Qh / Ql | L | C22, C28 |
| Zu2, Zu3 | 8A | 3A | 3A | FDPC8014S (dual) | | 0.56µH 18A | 600µF 3mΩ esr | FDMC8200S (dual) | 2µH 7A | 100µF 4mΩ esr |
| Zu4, Zu5 | 16A | 3A | 3A | FDMS3620S (dual) | | 0.22µH 33A | 1200µF 1.6mΩ esr | FDMC8200S (dual) | 2µH 7A | 100µF 4mΩ esr |
| Zu6, Zu7, Zu9 | 25A | 3A | 3A | CSD17304Q3 | BSC009NE2LS | 0.18µH 50A | 1850µF 1.2mΩ esr | FDMC8200S (dual) | 2µH 7A | 100µF 4mΩ esr |
| Zu11, Zu15, Zu17, Zu19 | 35A | 10A | 10A | CSD17304Q4 | BSC009NE2LS | 0.15µH 80A | 2600µF 0.9mΩ esr | FDPC8014S (dual) | 0.47µH 21A | 600µF 3mΩ esr |

# Scalable Zynq US + Always on Solution – No MGTs (UC1)




Notes:
1) XRP7724 manages sequence and dependency
2) XRP7724 provides correctly timed Ps_Por_B
3) PSU Telemetry
4) Scalable to meet full Zynq US+ Family
5) Optimized for maximum concatenation of rails

Full Schematic and BOM available
Visit: www.maxlinear.com/xilinx/zynq-ultrascale-plus_nomgts

**Power Stage (PS) Selection Table**

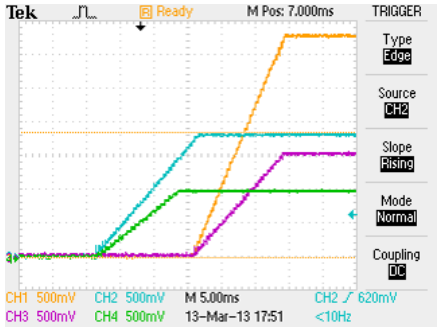
| | | | | PS1 | | | |
|---|---|---|---|---|---|---|---|
| Device | Icore (max) | Imgtavtt | Imgtavcc | Qh | Ql | L | C |
| Zu2, Zu3 | 8A | 3A | 3A | FDPC8014S (dual) | | 0.56µH 18A | 600µF 3mΩ esr |
| Zu4, Zu5 | 16A | 3A | 3A | FDMS3620S (dual) | | 0.22µH 33A | 1200µF 1.6mΩ esr |
| Zu6, Zu7, Zu9 | 25A | 3A | 3A | CSD17304Q3 | BSC009NE2LS | 0.18µH 50A | 1850µF 1.2mΩ esr |
| Zu11, Zu15, Zu17, Zu19 | 35A | 10A | 10A | CSD17304Q4 | BSC009NE2LS | 0.15µH 80A | 2600µF 0.9mΩ esr |

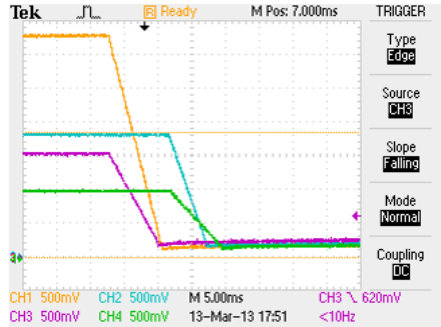
# Challenges & Resolutions

- Power Rail Concatenation
  - › Challenges
    - – UltraScale+ data sheet specifies >30 power rails for a full system including multi-gigabit transceivers (MGTs)
      - For majority of applications this is not required
    - – Group common rails to obtain a more manageable number and still be compliant with spec
  - › Resolution
    - – 2 solutions (one with MGTs & one without MGTs)
    - – Both solutions reduce rails to as few as possible and still meet UltraScale+ spec (UG538)

# Challenges & Resolutions *continued*

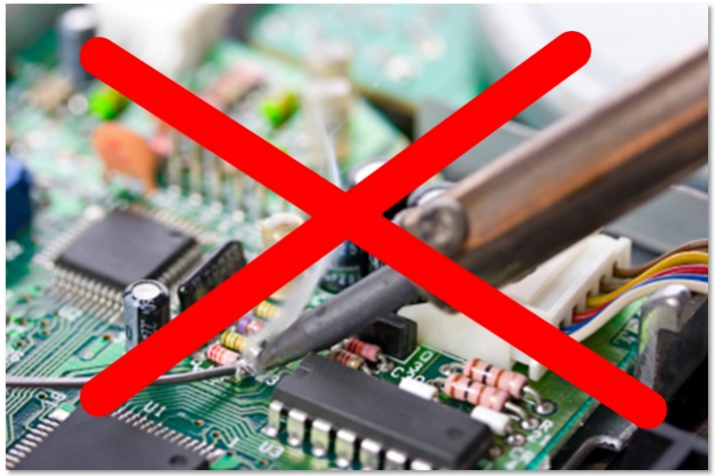
- Power Rail Sequencing
  - › Challenges
    - – Strict power up and power down sequencing requirements
    - – Power up sequencing requirements different than power down
    - – Power rail grouping based on $V_{OUT}$ but must also permit sequencing to be realized
  - › Resolution
    - – Uses internal digital control to easily manage sequencing requirements
    - – Programmable sequencing meets UltraScale+ spec for both power up and power down
    - – Keeps number of separate rails to minimum required to comply with UltraScale+ sequencing requirements



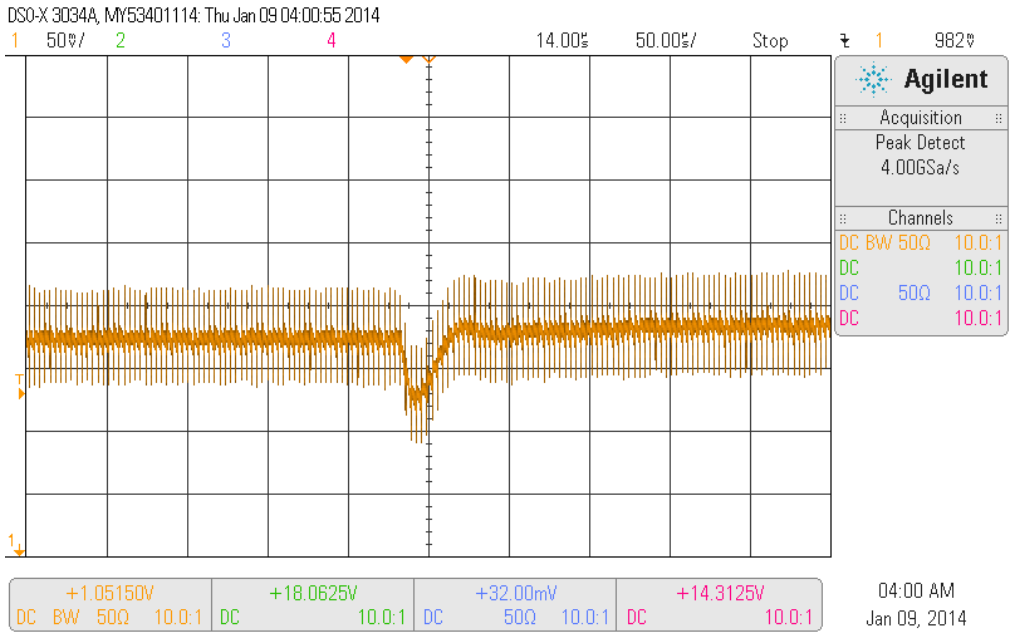
# Challenges & Resolutions *continued*

- Core Load
  - › Challenge
    - – The core load is difficult to determine with absolute certainty
  - › Resolution
    - – Flexible solution allows max current to be adjusted without complete redesign
- Performance
  - › Challenge
    - – UltraScale+ has tight constraints on $V_{OUT}$ for some rails
    - – Actual measured results rather than simulation much preferred
  - › Resolution
    - – See Slide # 12



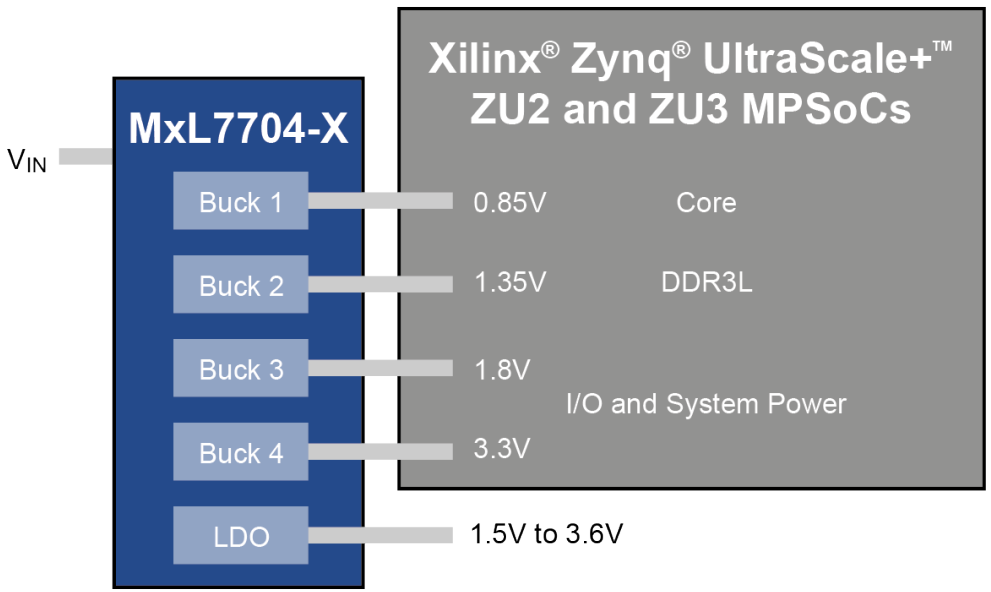
# Performance

- Actual Measurements
  - › Simulation does not take into account board parasitics
    - – When output cap is <1mR plane Z is significant
    - – Most simulations do not model esl of caps
    - – Efficiency measured in range of 83-95% depending on Fsw and load

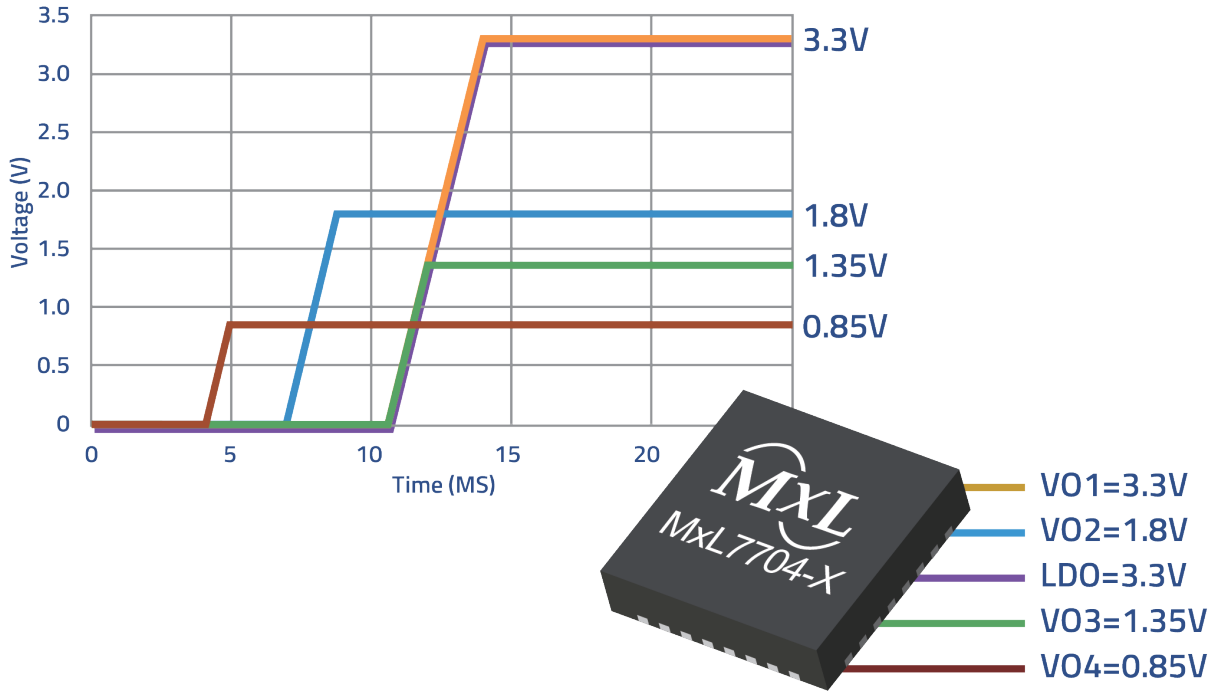



0.9V 5-25A step

# Optimized Power Management IC Provides Highly Efficient Rails for Xilinx Zynq UltraScale+ ZU2 and ZU3 MPSoCs




**Pre-Programmed Bucks Provide System, Memory, I/O and Core Power**




**Sequencing is Tailored to the Unique Needs of the ZU2 and ZU3 MPSoCs**



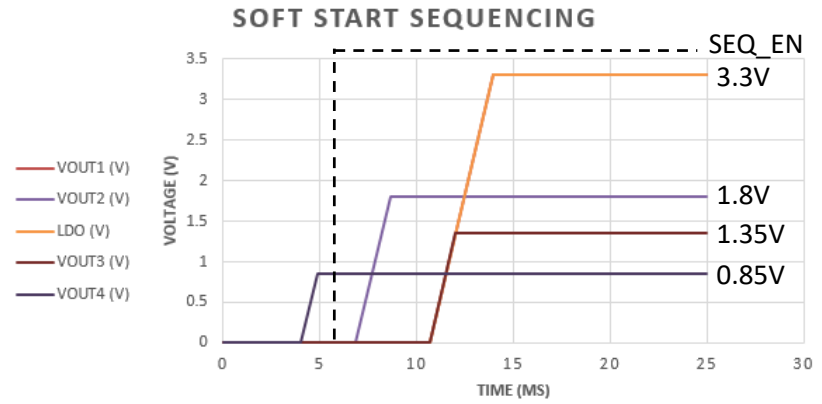


MAXLINEAR

# MxL7704-X : Xilinx® Zynq ® Ultrascale+™ ZU2, ZU3

- Output Voltages
  - 3.3V LDO
  - 3.3V Analog and IO
  - 1.8V IO
  - 1.35V DDR3
  - 0.85V Core
- Sequencing
  - 0.85V → SEQ_EN → 1.8V → 3.3V+1.35V
- PGOOD Assigned
  - PGOOD1 – unused
  - PGOOD2 – logical AND of all bucks
- 1.0MHz switching frequency
- Chip Fault
- 78ohm and soft off on

| | Sequencing Group | | Channel Enable | |
|---|---|---|---|---|
| | Buck 1 | 3 | ON | Buck 1 |
| | Buck 2 | 2 | ON | Buck 2 |
| | Buck 3 | 3 | ON | Buck 3 |
| | Buck 4 | 0 | ON | Buck 4 |
| | LDO | 3 | ON | LDO |
| SEQ_EN Group Assign | | 1 | | |



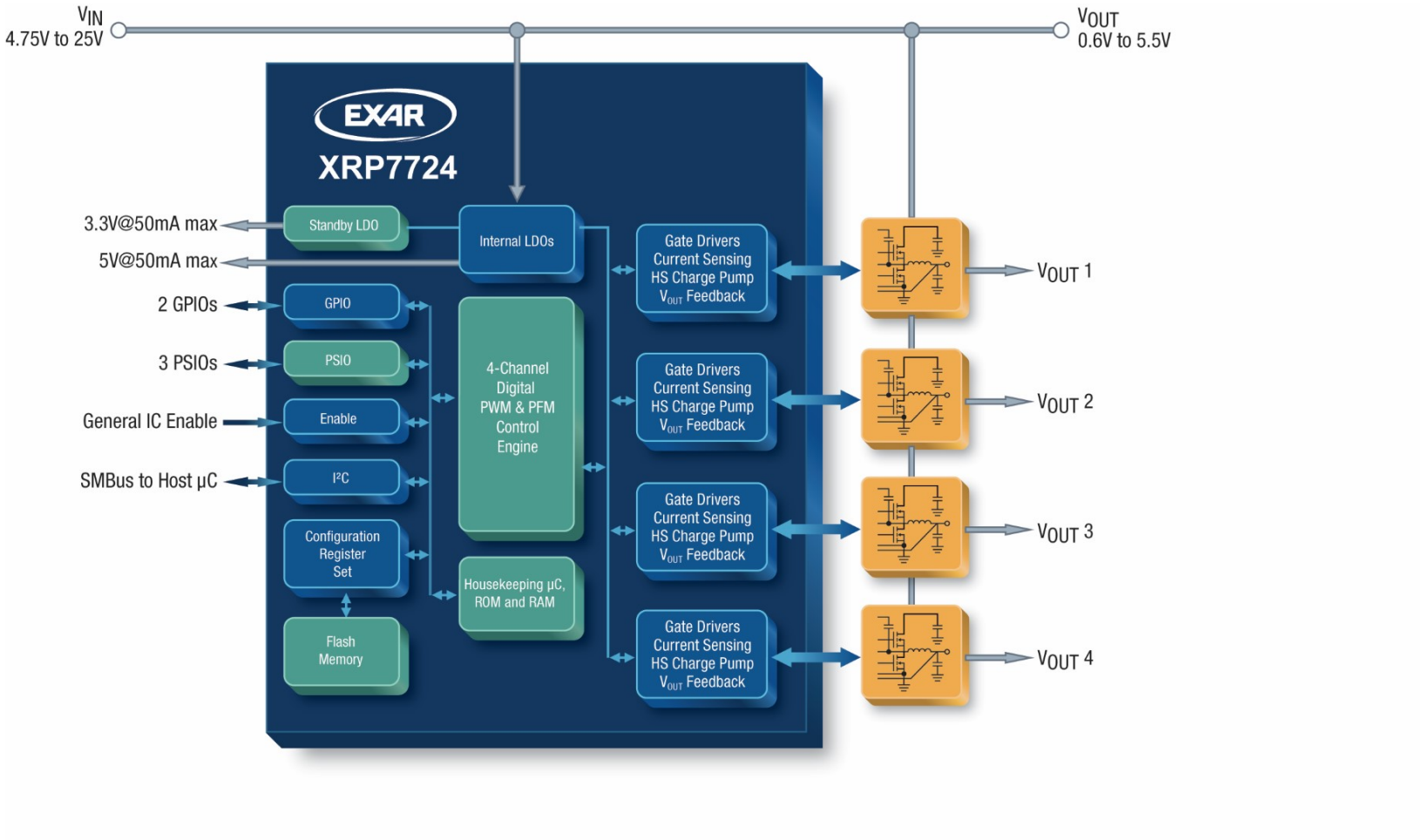

| | PG1 Routing | | PG2 Routing | |
|---|---|---|---|---|
| | Buck 1 | OFF | ON | Buck 1 |
| | Buck 2 | OFF | ON | Buck 2 |
| | Buck 3 | OFF | ON | Buck 3 |
| | Buck 4 | OFF | ON | Buck 4 |
| | LDO | OFF | OFF | LDO |


# Appendix

# Universal PMIC Selector Guide

| | MxL7704 | XR77103 | XRP7740 | XRP7713 | XRP7714 | XRP7724 | XRP7725 | XR77128 | XR77129 |
|---|---|---|---|---|---|---|---|---|---|
| **Channels** | 4 | 3 | 4 | 3 | 4 | 4 | | | |
| **Input Voltage** | 4.5-5.5 | 4.5-14 | 6.5V-20V | 4.75V-25V | | 4.75V-25V | | | 6V – 40V |
| **Output Voltage** | 3.0; 1.3; 0.8; 0.6 | 0.8-6 | 0.9V-5.1V | | | 0.6V-5.5V 2% -40°C→125°C | | 0.6V-5.5V* 1.25% -40°C→125°C | |
| **Gate Drive Ω** | 1.5A; 1.5A; 2.5A; 4A | Integrated MOSFETS | 3Ω/1.8Ω | 6Ω/3Ω | | 4Ω/2Ω | | | |
| **Vo Resolution** | 20mv; 20mV; 6.25mV; 6.25mV | 50mV | 50mV / 100mV | | | 2.5mV/5mV/10mV | | | |
| **Frequency (MHz)** | 1 to 2.1 | 0.3 to 2.2 | | Up to 1.5 | | Up to 1.2 | | | |
| **Monitoring Res** | 8bit | N/A | 8bit | 7bit | | 7bit | 7bit+ | 7bit | |
| **IQuiescent** | 8 | 1.5mA | 9mA | | | 4mA | | | |
| **Controller/Regulator** | Regulator | | Controller | | | | | | |
| **Control Scheme** | Current Mode PWM | Analog current mode | DPWM (11bit fixed, 0.5T Conversion) 300kHz-1.5MHz | | | DPFM/DPWM (17bit, 607ps fixed, 200ns conversion) 106kHz-1.2MHz – 1x; 2x; 4x Selectable | | | |
| **Phasing** | | Selectable 0°/180° | Selectable 90°/120° | Fixed 90° | | Variable with 22.5° resolution | | | |
| **Comm.** | $I^2C$ | $I^2C$ | $I^2C$ | $I^2C$ with PEC | | SMBus/$I^2C$ | | | |
| **GPIOs** | N/A | PGOOD | 4+2 | | | 2+3 PSIO | | 2+3 PSIO w/add'l options | |
| **LDOs** | 100mA | N/A | Single 3.3V or 5V – 110mA | | | Dual 3.3V & 5V / 110mA | | | |
| **Memory Type** | Factory Only | Flash | OTP | | | Flash | | | |
| **Light Load** | | ✓ | ✓ | × | | ✓ | | | |
| **Package** | 5x5 QFN32 | 4x4 TQFN32 | 6x6 TQFN40 | 5x5 TQFN32 | 6x6 TQFN40 | 7x7 TQFN44 pin compatible family | | | |
| **Other** | 2 configurable PGOOD outputs; LDO & 2-Input 8-bit ADC, Temp Monitoring MxL7704-A (Sequencing I/O first core last), MxL7704-X (Sequencing for Xilinx® Zynq® Ultrascale+™ ZU2 and ZU3) | Lower Cost | High Current | Best Value | | | Intel Node Manager Compatible | DrMOS Output | Higher outputs w/ ext. resistors |

# XRP7724 Functional Block Diagram



# MxL7704

## Universal PMIC with 4 Buck Regulators, one LDO, and 2 input 8bit ADC

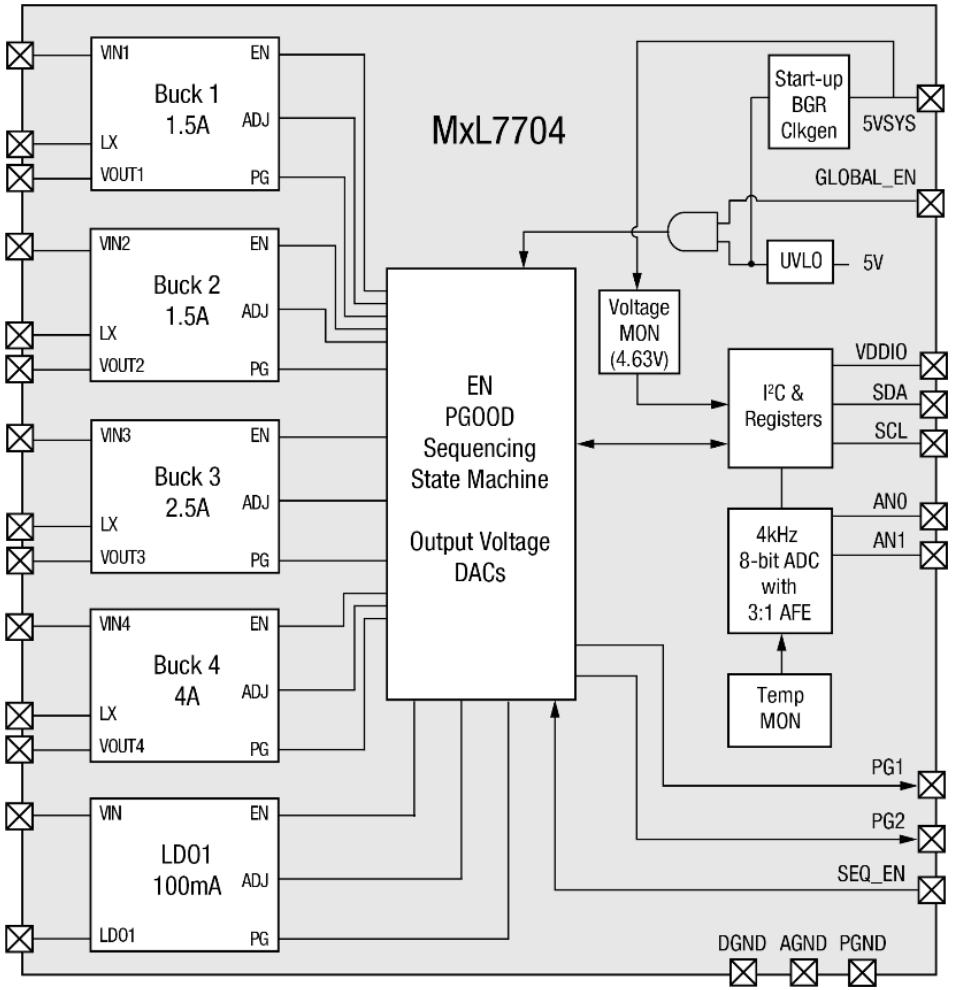
### Key Features

- 4.0V to 5.5V input supply voltage range
- Monolithic synchronous MOSFETs
  - Current-mode control internally compensated
  - 4A/2.5A/1.5A/1.5A Buck Regulator Outputs
- 100mA LDO
- I²C provides dynamic control
  - Dynamic voltage control on all outputs
  - 2 Configurable Power Good Output
  - Conditional Power up and down sequencing with external input for chip to chip sequencing
  - Switching frequency (1MHz to 2.1MHz)
  - Supported by Excel configuration tool
- 8 Bit ADC read through I2C
  - 2 external inputs with 2.55V range,10mV resolution
  - Temperature monitoring -40°C to 150°C
- 32-pin TQFN package, 5mm x 5mm

### Applications

- Low power FPGAs such as Xilinx® Zynq® Ultrascale+™
- ARM based processors
- Embedded low power processors
- Industrial control
- POS terminals

### Functional Block Diagram




### Benefits

- Programmable Power Technology
- Capable of supporting a wide range of processors
- Fast TTM
- Dynamic control
- Easy system integration
- High level integration

### Key Competitive Advantages

- I²C interface tailor to processor requirements
- Flexible Sequencing
- ADC provides telemetry flexibility

### Availability & Tools

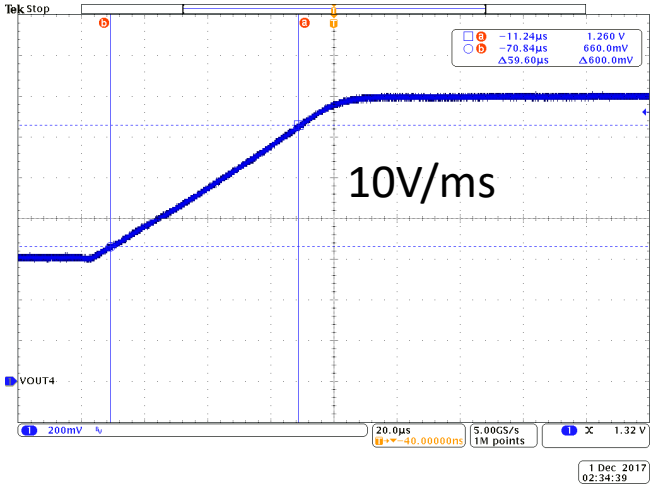
**Production**

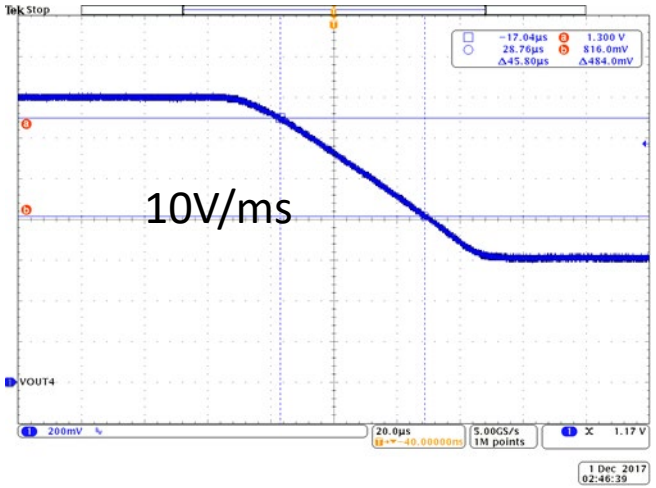
- MxL7704-A
  - ARM® Cortex® A53 and A7/9
- MxL7704-X
  - Xilinx® Zynq® Ultrascale+™ ZU2/3
- Excel configuration tool
- Evaluation Boards

MAXLINEAR

# Dynamically Controllable Outputs

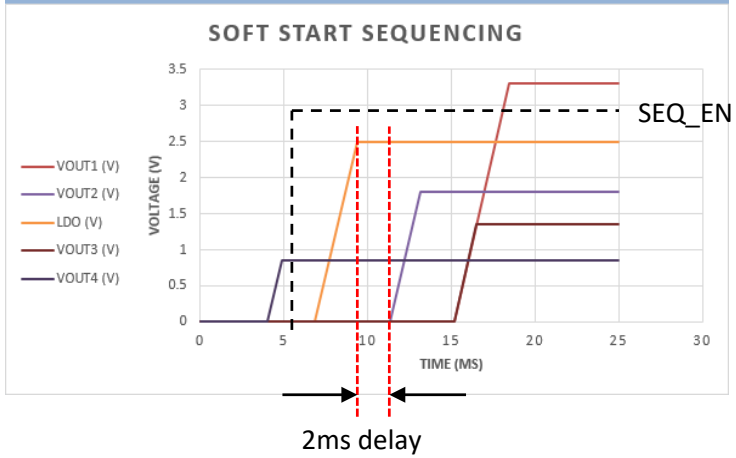
- Buck 1 1.5A 3.0V to 3.6V 20mV resolution
- Buck 2 1.5A 1.3V to 1.92V 20mV resolution
- Buck 3 2.5A 0.8V to 1.6V 6.25mV resolution
- Buck 4 4.0A 0.6V to 1.4V 6.25mV resolution
- LDO 0.1A 1.5V to 3.6V 20mV resolution
- DVS (Dynamic Voltage Scaling) at 10V/ms slew rate meets the latency demands of most processors.



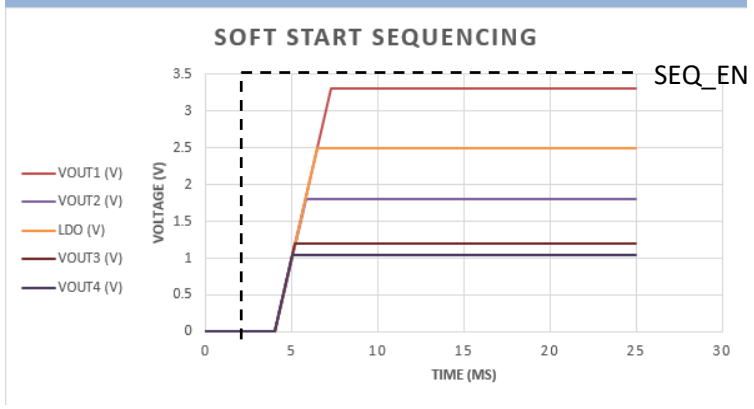



# Flexible Conditional Sequencing Engine

| Sequencing Group | | Channel Enable | |
|---|---|---|---|
| Buck 1 | 3 | ON | Buck 1 |
| Buck 2 | 2 | ON | Buck 2 |
| Buck 3 | 3 | ON | Buck 3 |
| Buck 4 | 0 | ON | Buck 4 |
| LDO | 1 | ON | LDO |
| SEQ_EN Group Assign | 1 | | |

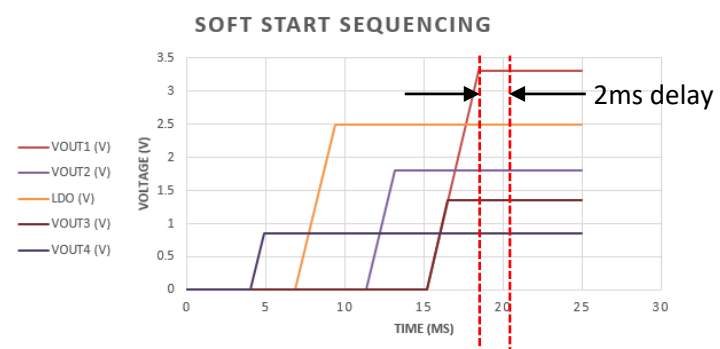



| Sequencing Group | | Channel Enable | |
|---|---|---|---|
| Buck 1 | 1 | ON | Buck 1 |
| Buck 2 | 1 | ON | Buck 2 |
| Buck 3 | 1 | ON | Buck 3 |
| Buck 4 | 1 | ON | Buck 4 |
| LDO | 1 | ON | LDO |
| SEQ_EN Group Assign | 0 | | |

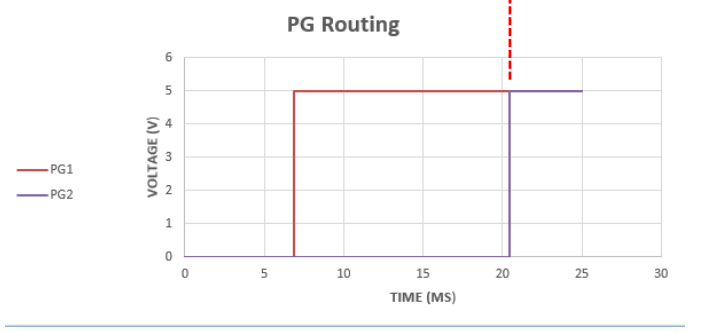


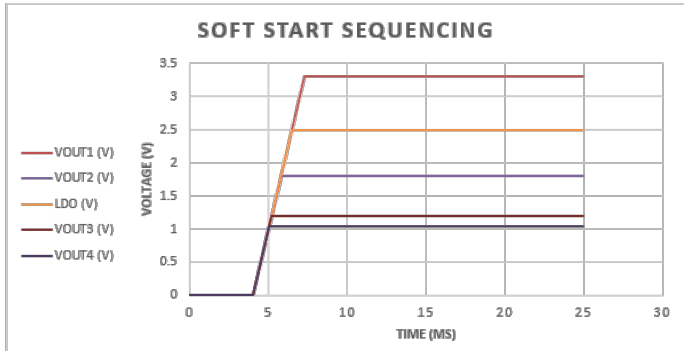

- 4 Sequencing Groups 0 → 3
- All outputs may be assigned to any sequencing group
- Sequencing of the next group is conditional on PGOOD of the first with a 2ms delay
- SEQ_EN input pin gates the sequencing at the group it is assigned.
- Down sequencing is the reverse order of power up.

# PGOOD Routing Flexibility

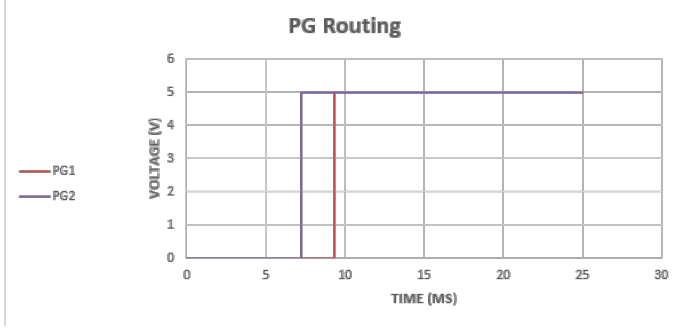



| PG1 Routing | | PG2 Routing | |
|---|---|---|---|
| Buck 1 | OFF | ON | Buck 1 |
| Buck 2 | OFF | ON | Buck 2 |
| Buck 3 | OFF | ON | Buck 3 |
| Buck 4 | ON | OFF | Buck 4 |
| LDO | OFF | ON | LDO |



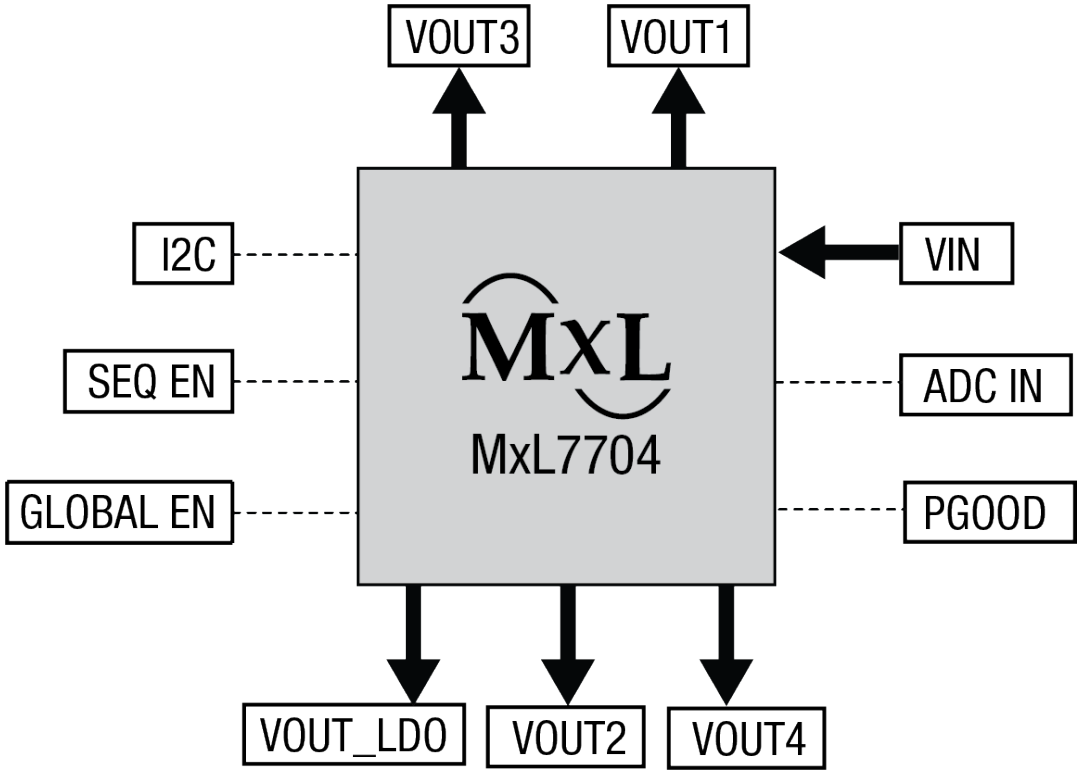



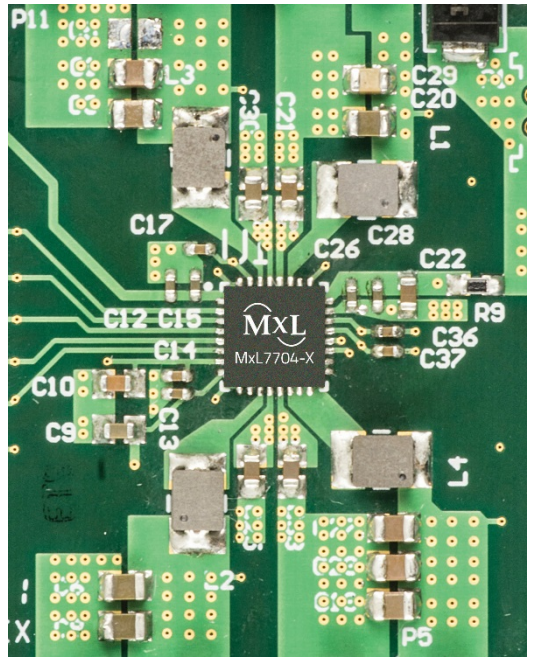

| PG1 Routing | | PG2 Routing | |
|---|---|---|---|
| Buck 1 | ON | OFF | Buck 1 |
| Buck 2 | ON | OFF | Buck 2 |
| Buck 3 | OFF | ON | Buck 3 |
| Buck 4 | OFF | ON | Buck 4 |
| LDO | OFF | OFF | LDO |




- PGOOD Outputs are a logical AND of all the channels assigned to it
- Any channel may be assigned to any PGOOD
- PGOOD goes high when the output is >90% of the final value and soft-start is complete with a 2ms delay
- PGOOD de-asserts when <85% of target or when channel is shut down

# MxL7704 Evaluation Board Block Diagram



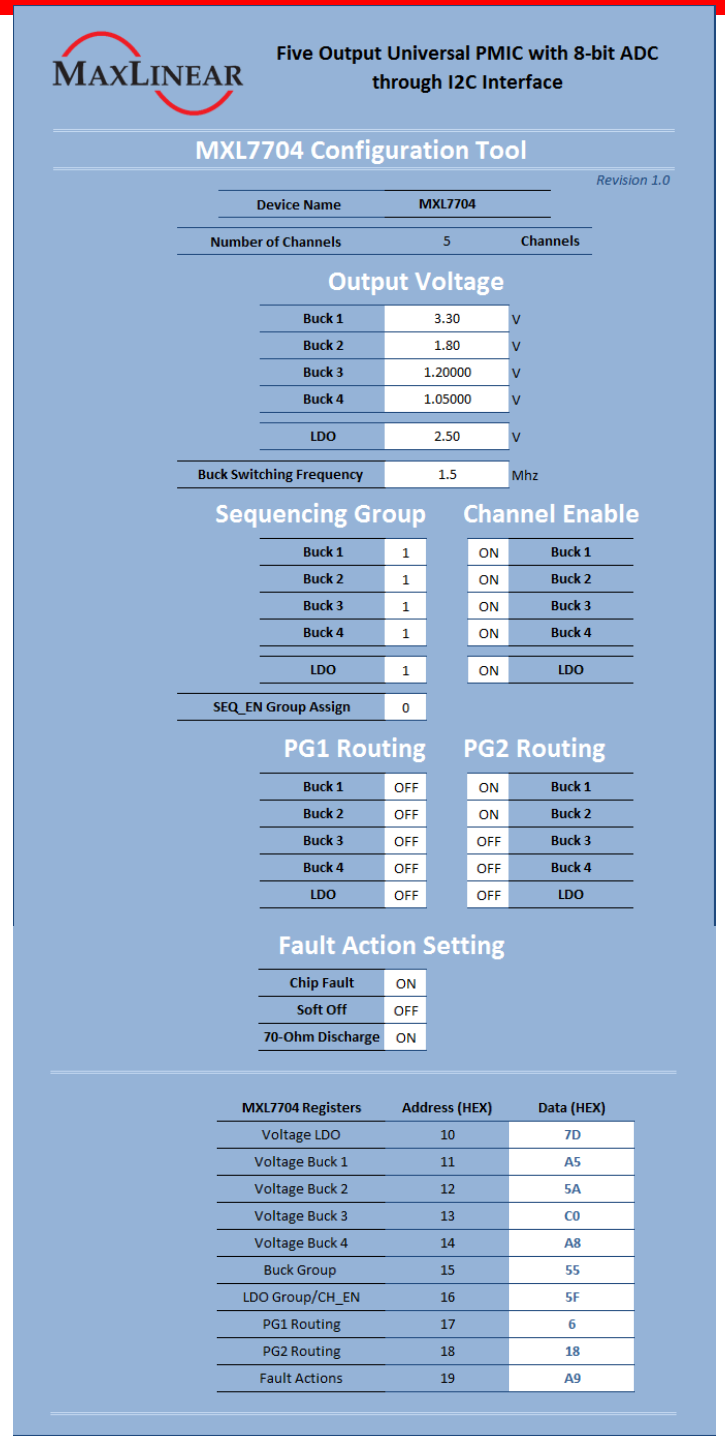

Top View MxL7704 EVB

- Board layout maintains flexibility for the engineer to easily modify components to exercise MxL7704 capabilities

# Software Support

- Simple tool providing the customer a fast and easy way to generate register bits to meet their system requirement

| Address | Register | R/W | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x10 | Vout LDO1 | R/W | VLDO1[7:0] | | | | | | | |
| 0x11 | Vout Buck1 | R/W | VBuck1[7:0] | | | | | | | |
| 0x12 | Vout Buck2 | R/W | VBuck2[7:0] | | | | | | | |
| 0x13 | Vout Buck3 | R/W | VBuck3[7:0] | | | | | | | |
| 0x14 | Vout Buck4 | R/W | VBuck4[7:0] | | | | | | | |
| 0x15 | Buck Sequence Group Assignment | R/W | Buck 4[1:0] | | Buck 3[1:0] | | Buck 2[1:0] | | Buck 1[1:0] | |
| 0x16 | LDO1 Sequence Group Assignment and Channel Enables | R/W | LDO1[1:0] | | | EN4 | EN3 | EN2 | EN1 | ENL |
| 0x17 | SEQ_EN Assign and PG1 Routing | R/W | EN Assign | | | Buck4 | Buck3 | Buck2 | Buck1 | LDO |
| 0x18 | PG2 Routing | R/W | | | | Buck4 | Buck3 | Buck2 | Buck1 | LDO |
| 0x19 | Fault Actions, Down Sequencing, Frequency | R/W | Chip/ Channel | Soft Off | 78ohm discharge | | FREQ[3:0]* | | | |



# XR77129

## 40V Quad Output Digital PWM/PFM Universal PMIC

### Key Features

- Quad Channel Step-down Controller
  - › Digital PWM 105kHz-1.23MHz operation
  - › Individual channel frequency selection
  - › Patented digital PFM with ultrasonic mode
  - › Integrated MOSFET drivers
- 6V to 40V Input Voltage
- 0.6V to 5.5V output voltage (higher w/external resistors)
- SMBus Compliant I2C Interface
- Full Power Monitoring and Reporting
- 3 x 15V Capable PSIO + 2 x GPIOs
- Full Start/Stop Sequencing Support
- Built-in thermal, over-current, UVLO & output
- Over-voltage protection
- On-board 5V and LDOOUT Standby LDOs
- On-board non-volatile memory

### Applications

- Industrial Equipment
- Test Equipment
- Automotive
- Base Stations

### Key Competitive Advantages

**Lower power/channel**

- <1.5mA vs industry at 30mA
- State machine based

**Lower cost and component count**

- Saves as many as 50 components

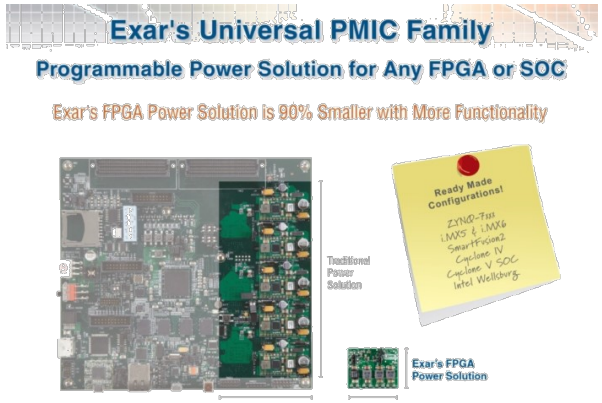
**Easy to use**

- Easy to use tools
- Intuitive register map

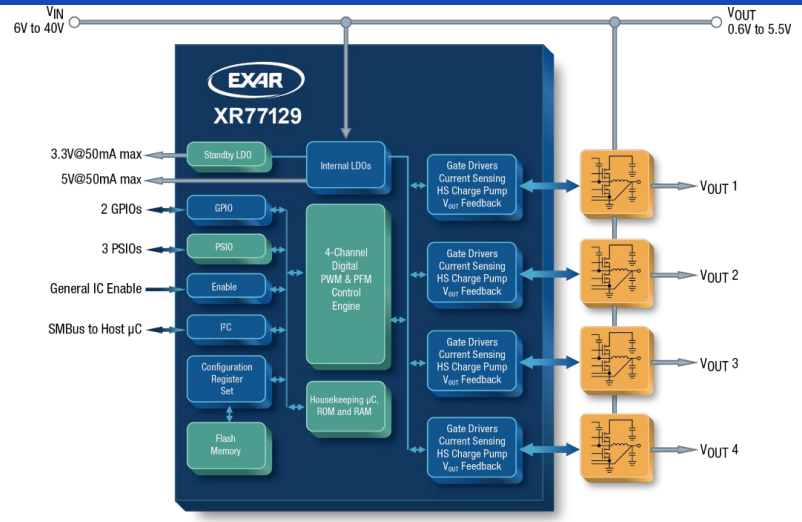
MaxLinear PMIC Advantages

### Benefits

- Only 40V digital controller
- Flexible, adaptive & economical
  - › Quickly adaptable design
  - › Reduced time to market
  - › Integrates several functions/ICs
- Reliable
  - › Eliminates passive components temperature drifts and aging
  - › Remote monitoring/configuration
- High Performance
- Optimized power conversion / output




### Functional Block Diagram




### Availability & Tools

**In Production**

- XR77129
  - › TQFN44
- Supported by PowerArchitect™ 5.2 or later
- Evaluation Board
- Demo Kit with PowerArchitect

**Full line of Universal PMICS**

- XRP7704-40, XRP7713-14, XRP7724, XRP7725 & XR77129, XR77103





MAXLINEAR


# Thank You