ST16C552
ST16C552A

DUAL UART WITH 16-BYTE FIFO AND PARALLEL PRINTER PORT

December 2003

DESCRIPTION

The ST16C552/ST16C552A (552/552A) is a dual universal asynchronous receiver and transmitter (UART) with an added bi-directional parallel port that is directly compatible with a CENTRONICS type printer. The parallel port is designed such that the user can configure it as general purpose I/O interface, or for connection to other printer devices. The 552/552A provides enhanced UART functions with 16 byte FIFO's, a modem control interface, and data rates up to 1.5Mbps. Onboard status registers provide the user with error indications and operational status. The system interrupts and control may be tailored to meet user requirements. An internal loop-back capability allows onboard diagnostics. A programmable baud rate generator is provided to select transmit and receive clock rates from 50 bps to 1.5 Mbps. The 552/552A is available in a 68 pin PLCC package. The 552/552A is compatible with the 16C450 and 16C550. The difference between the ST16C552 and ST16C552A is the logic state of the printer port, INTP interrupt. The INTP interrupt is active high (logic 1) on the ST16C552 whereas INTP is active low (logic 0) on the ST16C552A part when the interrupt latch mode is selected. The 552/552A is fabricated in an advanced CMOS process with power down mode to reduce the power consumption. The 552A does not support the power down mode.

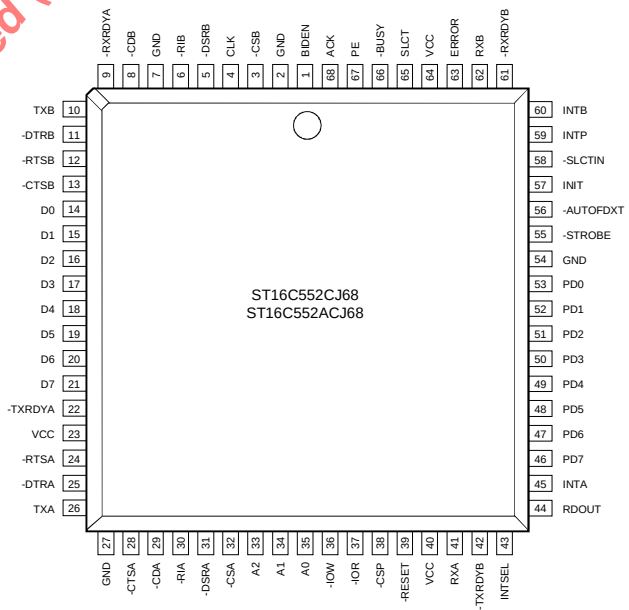
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FEATURES

Added features in device revision "F" and newer:

- 5V Tolerant Inputs
- Pin to pin and functional compatible to ST16C452/ 452PS, TL16C552
- 2.97 to 5.5 volt operation
- Software compatible with INS8250, NS16C550
- 1.5 Mbps transmit/receive operation (24MHz)
- 16 byte transmit FIFO
- 16 byte receive FIFO with error flags
- Independent transmit and receive control
- Modem and printer status registers
- UART port and printer port Bi-directional
- Printer port direction set by single control bit or 8 bit pattern (AA/55)
- Modem control signals (-CTS, -RTS, -DSR, -DTR, -RI, -CD)
- Programmable character lengths (5, 6, 7, 8)
- Even, odd, or no parity bit generation and detection
- TTL compatible inputs, outputs
- Power down mode

PLCC Package

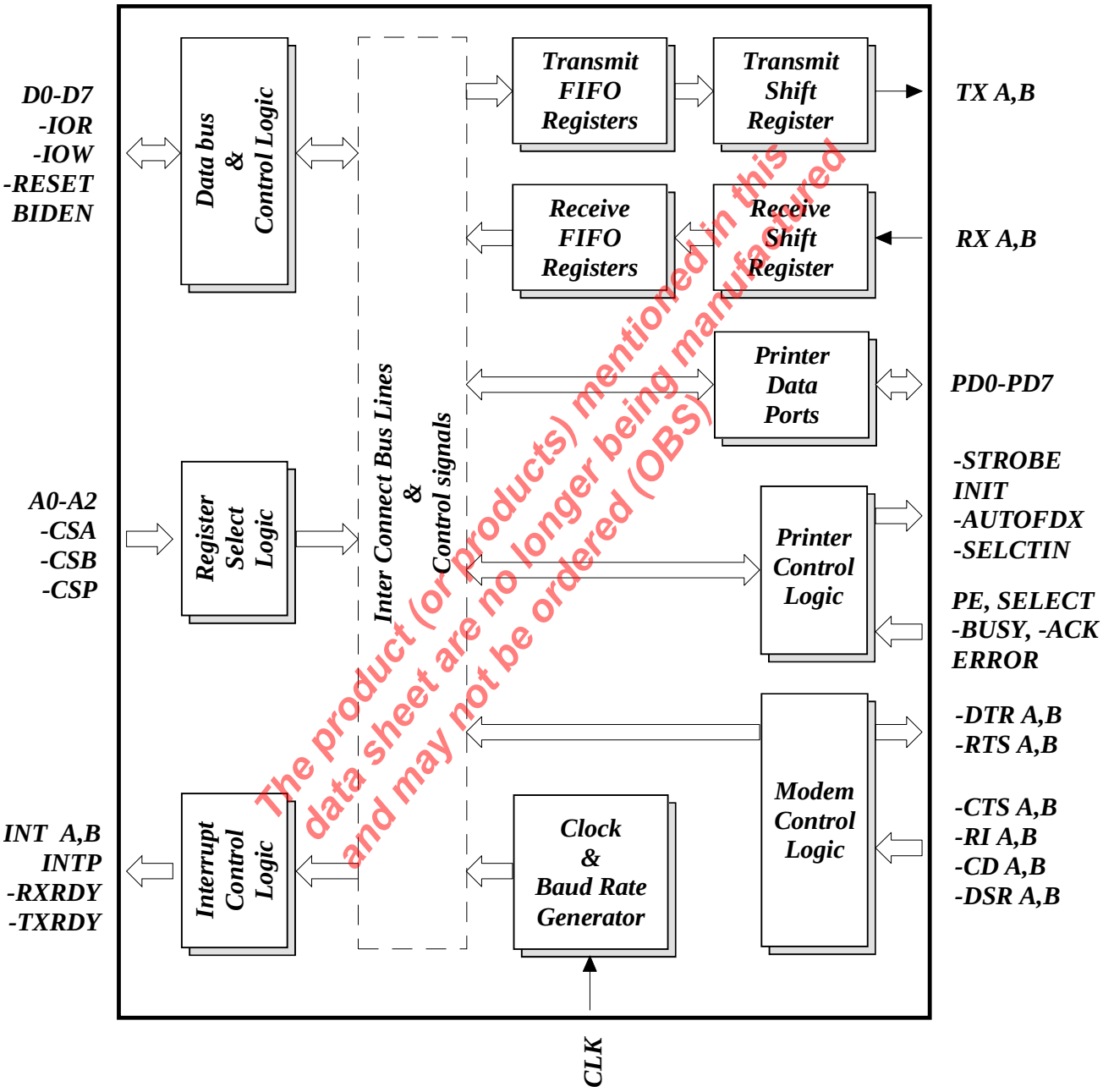


ORDERING INFORMATION

Part number	Pins	Package	Operating temperature	Device Status
ST16C552CJ68	68	PLCC	0° C to + 70° C	Active
ST16C552ACJ68	68	PLCC	0° C to + 70° C	Active
ST16C552IJ68	68	PLCC	-40° C to + 85° C	Active
ST16C552AIJ68	68	PLCC	-40° C to + 85° C	Active

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Figure 1, Block Diagram



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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
A0	35	I	Address-0 Select Bit - Internal registers address selection.
A1	34	I	Address-1 Select Bit - Internal registers address selection.
A2	33	I	Address-2 Select Bit - Internal registers address selection.
-ACK	68	I	Acknowledge (with internal pull-up) - General purpose input or line printer acknowledge (active low). a logic 0 from the printer, indicates successful data transfer to the print buffer.
-AutoFDXT	56	I/O	General purpose I/O (open drain, with internal pull-up) or automatic line feed (open drain input with internal pull-up). When this signal is low the printer should automatically line feed after each line is printed.
BIDEN	1	I	Bi-Direction Enable - PD7-PD0 direction select. A logic 0 sets the parallel port for I/O Select Register Control. A logic 1 sets the parallel port for Control Register Bit-5 Control.
BUSY	66	I	Busy (with internal pull-up) - General purpose input or line printer busy (active high). can be used as an output from the printer to indicate printer is not ready to accept data.
CLK	4	I	Clock Input. - An external clock must be connected to this pin to clock the baud rate generator and internal circuitry (see Programmable Baud Rate Generator). This input is not 5V tolerant.
-CSA	32	I	Chip Select A - A logic 0 at this pin enables the serial channel-A UART registers for CPU data transfers.
-CSB	3	I	Chip Select B - A logic 0 at this pin enables the serial channel-B UART registers for CPU data transfers.
-CSP	38	I	Printer Port Chip Select - (active low). A logic 0 at this pin enables the parallel printer port registers and/or PD7-PD0 for external CPU data transfers.
D0-D7	14-21	I/O	Data Bus (Bi-directional) - These pins are the eight bit, three state data bus for transferring information to or from the controlling CPU. D0 is the least significant bit and the first data bit in a transmit or receive serial data stream.

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
-ERROR	63	I	Error, Printer (with internal pull-up) - General purpose input or line printer error. This pin may be connected to the active low (logic 0) output of a printer to indicate an error condition.
GND	2,7,54 27	Pwr	Signal and Power Ground.
INIT	57	I/O	Initialize (open drain, with internal pull-up) - General purpose I/O signal. This pin may be connected for initialization service of a connected line printer. Generally when this signal is a logic 0, any connected printer will be initialized.
INT A/B	45,60	O	Interrupt output A/B (three state active high) - These pins provide individual channel interrupts, INT A-B. INT A-B are enabled when MCR bit-3 is set to a logic 1, interrupts are enabled in the interrupt enable register (IER), and when an interrupt condition exists. Interrupt conditions include: receiver errors, available receiver buffer data, transmit buffer empty, or when a modem status flag is detected.
-INTP	59	O	Printer Interrupt, - This pin can be used to signal the interrupt status of a connected printer. This pin basically tracks the -ACK input pin, When INTSEL is a logic 0 and interrupts are enabled by bit-4 in the control register. A latched mode can be selected by setting INTSEL to a logic 1. In this case the interrupt -INTP is generated normally but does not return to the inactive state until the trailing edge of the read cycle (-IOR pin). -INTP is three stated until CON bit-4 is set to a logic 1. The difference between the ST16C552 and ST16C552A is the output state of INTP. INTP is active high (logic 1) on the ST16C552 whereas INTP is active low (logic 0) on the ST16C552A part when the interrupt latch mode is selected.
INTSEL	43	I	Interrupt Select mode - This pin selects the interrupt type for the printer port (-INTP). When this pin is a logic 0, the external -ACK signal state is generally followed, minus some minor propagation delay. Making this pin a logic 1 or connecting it to VCC will set the interrupt latched mode. In this case the printer interrupt (-INTP) will not return to a logic 0 on the 552 or a logic 1 on the 552A (552A is inverted), until the

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			trailing edge of -IOR (end of the external CPU read cycle).
-IOR	37	I	Read strobe.- A logic 0 transition on this pin will place the contents of an Internal register defined by address bits A0-A2 for either UART channels A/B or A0-A1 for the printer port, onto D0-D7 data bus for a read cycle by an external CPU.
-IOW	36	I	Write strobe.- A logic 0 transition on this pin will transfer the data on the internal data bus (D0-D7), as defined by either address bits A0-A2 for UART channels A/B or A0-A1 for the printer port, into an internal register during a write cycle from an external CPU.
PD7-PD0	46-53	I/O	Printer Data port (Bi-directional three state) - These pins are the eight bit, three state data bus for transferring information to or from an external device (usually a printer). D0 is the least significant bit. PD7-PD0 are latched during a write cycle (output mode).
PE	67	I	Paper Empty - General purpose input or line printer paper empty (Internal pull-up). This pin can be connected to provide a printer out of paper indication.
RDOUT	44	O	Read Out (active high) - This pin goes to a logic 1 when the external CPU is reading data from the 552/552A. This signal can be used to enable/disable external transceivers or other logic functions.
-RESET	39	I	Master Reset (active low) - a logic 0 on this pin will reset the internal registers and all the outputs. The UART transmitter output and the receiver input will be disabled during reset time. (See ST16C552/552A External Reset Conditions for initialization details.)
-RXRDY A/B	9,61	O	Receive Ready A/B (active low). This function is associated with the dual channel UARTs and provide the RX FIFO/RHR status for individual receive channels (A-B). A logic 0 indicates there is receive data to read/unload, i.e., receive ready status with one or more RX characters available in the FIFO/RHR. This pin is a logic 1 when the FIFO/RHR is empty or when the programmed trigger level has not been

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			reached.
SLCT	65	I	Select (with internal pull-up) - General purpose input or line printer select status. Normally this pin is connected to a printer output (active low) that indicates the ready status of a printer, i.e., on-line and/or on-line and ready.
-SLCTIN	58	I/O	Select In (open drain, with internal pull-up) - General purpose I/O or line printer select. This pin can be read via Bit-3 in the printer command register, or written via bit-3 in the printer control register. As this pin is open-drain, it can be wire-or'd with other outputs. Normally this signal is connected with a printer to select the printer with an active low.
-STROBE	55	I/O	Strobe (open drain, with internal pull-up) - General purpose I/O or data strobe output. Normally this output is connected to a printer and indicates that valid data is available at the printer port (PD0-PD7).
-TXRDY A/B	22,42	O	Transmit Ready A/B (active low). These outputs provide the TX FIFO/THR status for individual transmit channels (A-B). As such, an individual channel's -TXRDY A-B buffer ready status is indicated by logic 0, i.e., at least one location is empty and available in the FIFO or THR. This pin goes to a logic 1 when there are no more empty locations in the FIFO or THR.
VCC	23,40,64	Pwr	2.97 to 5.5V power supply input. All inputs are 5V tolerant except for XTAL1 and all printer port inputs for devices with revision "F" and newer.
-CD A/B	29,8	I	Carrier Detect (active low) - These inputs are associated with individual UART channels A through B. A logic 0 on this pin indicates that a carrier has been detected by the modem for that channel.
-CTS A/B	28,13	I	Clear to Send (active low) - These inputs are associated with individual UART channels, A through B. A logic 0 on this pin(s) indicates the modem or data set is ready to accept transmit data from the 552/552A for the given channel. Status can be tested by reading MSR bit-4 for that channel(s). -CTS has no

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SYMBOL DESCRIPTION

Symbol	Pin	Signal Type	Pin Description
			effect on the transmit or receive operation.
-DSR A/B	31,5	I	Data Set Ready (active low) - These inputs are associated with individual UART channels, A through B. A logic 0 on this pin(s) indicates the modem or data set is powered-on and is ready for data exchange with the UART. This pin has no effect on the UART's transmit or receive operation.
-DTR A/B	25,11	O	Data Terminal Ready (active low) - These outputs are associated with individual UART channels, A through B. A logic 0 on this pin(s) indicates that the 552/552A is powered-on and ready. This pin can be controlled via the modem control register for channel(s) A-B. Writing a logic 1 to MCR bit-0 will set the -DTR output to logic 0, enabling the modem. This pin will be a logic 1 after writing a logic 0 to MCR bit-0, or after a reset. This pin has no effect on the UART's transmit or receive operation.
-RI A/B	30,6	I	Ring Indicator (active low) - These inputs are associated with individual UART channels, A through B. A logic 0 on this pin(s) indicates the modem has received a ringing signal from the telephone line(s). A logic 1 transition on this input pin will generate an interrupt for the ringing channel(s). This pin does not have any effect on the transmit or receive operation.
-RTS A/B	24,12	O	Request to Send (active low) - These outputs are associated with individual UART channels, A through B. A logic 0 on the -RTS pin(s) indicates the transmitter has data ready and waiting to send for the given channel(s). Writing a logic 1 in the modem control register (MCR bit-1) will set this pin to a logic 0 indicating data is available. After a reset this pin will be set to a logic 1. This pin does not have any effect on the transmit or receive operation.
RX A/B	41,62	I	Receive Data Input, RX A-B. - These inputs are associated with individual serial channel(s) to the 552. The RX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local loop-back mode, the RX input pins are disabled and TX data is internally connected to the

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Symbol	Pin	Signal Type	Pin Description
TX A/B	26,10	O	UART RX Inputs, internally. Transmit Data, TX A-B - These outputs are associated with individual serial transmit channel(s) from the 552/552A. The TX signal will be a logic 1 during reset, idle (no data), or when the transmitter is disabled. During the local loop-back mode, the TX output pins are disabled and TX data is internally connected to the UART RX Inputs.

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GENERAL DESCRIPTION

The 552/552A provides serial asynchronous receive data synchronization, parallel-to-serial and serial-to-parallel data conversions for both the transmitter and receiver sections. These functions are necessary for converting the serial data stream into parallel data that is required with digital data systems. Synchronization for the serial data stream is accomplished by adding start and stops bits to the transmit data to form a data character (character orientated protocol). Data integrity is insured by attaching a parity bit to the data character. The parity bit is checked by the receiver for any transmission bit errors. The electronic circuitry to provide all these functions is fairly complex especially when manufactured on a single integrated silicon chip. The 552/552A represents such an integration with greatly enhanced features. The 552/552A is fabricated with an advanced CMOS process.

The 552/552A is an upward solution that provides 16 bytes of transmit and receive FIFO memory, instead of none in the 16C452. The 552/552A is designed to work with high speed modems and shared network environments, that require fast data processing time. Increased performance is realized in the 552/552A by the transmit and receive FIFO's. This allows the external processor to handle more networking tasks within a given time. For example, the ST16C452 without a receive FIFO, will require unloading of the RHR in 95.5 microseconds (This example uses a character length of 11 bits, including start/stop bits at 115.2Kbps). This means the external CPU will have to service the receive FIFO every 100 microseconds. However with the 16 byte FIFO in the 552/552A, the data buffer will not require unloading/loading for 1.53 ms. This increases the service interval giving the external CPU additional time for other applications and reducing the overall UART interrupt servicing time. In addition, the 4 selectable levels of FIFO trigger interrupt is uniquely provided for maximum data throughput performance especially when operating in a multi-channel environment. The FIFO memory greatly reduces the bandwidth requirement of the external controlling CPU, increases performance, and reduces power consumption.

The 552/552A combines the package functions of a dual UART and a printer interface on a single integrated chip. The 552/552A UART is indented to be software compatible with the INS8250/NS16C550 while the bi-directional printer interface mode is intended to operate with a CENTRONICS type parallel printer. However, the printer interface is designed such that it may be configured to operate with other parallel printer interfaces or used as a general purpose parallel interface. The 552/552A is available in two versions, the ST16C552 and the ST16C552A. The 552A provides a active low (logic 0) interrupt for the printer port (INTP) while the 552 provides an active high (logic 1) INTP interrupt. Additionally, the 552A does not support the power down feature.

The 552/552A is capable of operation to 1.5Mbps with a 24 MHz external clock input. With an external clock input of 1.8432 MHz the user can select data rates up to 115.2 Kbps.

The rich feature set of the 552/552A is available through internal registers. Selectable receive FIFO trigger levels, selectable TX and RX baud rates, modem interface controls, and a power-down mode are all standard features. Following a power on reset or an external reset, the 552/552A is software compatible with the previous generation, 16C452.

FUNCTIONAL DESCRIPTIONS

Functional Modes

Two functional user modes are selectable for the 552/552A package. The first of these provides the dual UART functions, while the other provides the functions of a parallel printer interface. These features are available through selection at the package interface select pins.

UART A-B Functions

The UART mode provides the user with the capability to transfer information between an external CPU and the 552/552A package. A logic 0 on chip select pins -CSA or -CSB allows the user to configure, send data, and/or receive data via the UART channels A-B.

Printer Port Functions

The Printer mode provides the user with the capability to transfer information between an external CPU and the 552/552A parallel printer port. A logic 0 on chip select pin -CSP allows the user to configure, send data, and/or receive data via the bi-directional parallel 8-bit data bus, PD0-PD7.

Internal Registers

The 552/552A provides 12 internal registers for monitoring and control of the UART functions and another 6 registers for monitoring and controlling the printer port. These resisters are shown in Table 4 below. The UART registers function as data holding registers (THR/RHR), interrupt status and control registers (IER/ISR), a FIFO control register (FCR), line status and control registers (LCR/LSR), modem status and control registers (MCR/MSR), programmable data rate (clock) control registers (DLL/DLM), and a user assessable scratchpad register (SPR). The printer port registers functions data holding registers (PR), I/O status register (SR), I/O select register (IOSEL), and a command and control register (COM/CON). Register functions are more fully described in the following paragraphs.

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Table 4, INTERNAL REGISTER DECODE

A2	A1	A0	READ MODE	WRITE MODE
General Register Set (THR/RHR, IER/ISR, MCR/MSR, LCR/LSR, SPR): Note 1*				
0	0	0	Receive Holding Register	Transmit Holding Register
0	0	1		Interrupt Enable Register
0	1	0	Interrupt Status Register	FIFO Control Register
0	1	1		Line Control Register
1	0	0		Modem Control Register
1	0	1	Line Status Register	
1	1	0	Modem Status Register	
1	1	1	Scratchpad Register	Scratchpad Register
Baud Rate Register Set (DLL/DLM): Note *2				
0	0	0	LSB of Divisor Latch	LSB of Divisor Latch
0	0	1	MSB of Divisor Latch	MSB of Divisor Latch
Printer Port Set (PR/SR/IOSEL/COM/CON): Note *3				
X	0	0	PORT REGISTER	PORT REGISTER
X	0	1	STATUS REGISTER	I/O SELECT REGISTER
X	1	0	COMMAND REGISTER	CONTROL REGISTER

Note 1* The General Register set is accessible only when CS A or CS B is a logic 0.
Note 2* The Baud Rate register set is accessible only when CS A or CS B is a logic 0 and LCR bit-7 is a logic 1.
Note 3*: Printer Port Register set is accessible only when -CSP is a logic 0 in conjunction with the states of the interface signal BIDEN and Printer Control Register bit-5 or IOSEL register.

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FIFO Operation

The 16 byte transmit and receive data FIFO's are enabled by the FIFO Control Register (FCR) bit-0. The user can set the receive trigger level via FCR bits 6/7 but not the transmit trigger level. The transmit interrupt trigger level is set to 16 following a reset. The receiver FIFO section includes a time-out function to ensure data is delivered to the external CPU. An interrupt is generated whenever the Receive Holding Register (RHR) has not been read following the loading of a character or the receive trigger level has not been reached.

Hardware/Software and Time-out Interrupts

The interrupts are enabled by IER bits 0-3. Care must be taken when handling these interrupts. Following a reset the transmitter interrupt is enabled, the 552/552A will issue an interrupt to indicate that transmit holding register is empty. This interrupt must be serviced prior to continuing operations. The LSR register provides the current singular highest priority interrupt only. It could be noted that CTS and RTS interrupts have lowest interrupt priority. A condition can exist where a higher priority interrupt may mask the lower priority CTS/RTS interrupt(s). Only after servicing the higher pending interrupt will the lower priority CTS/RTS interrupt(s) be reflected in the status register. Servicing the interrupt without investigating further interrupt conditions can result in data errors.

When two interrupt conditions have the same priority, it is important to service these interrupts correctly. Receive Data Ready and Receive Time Out have the same interrupt priority (when enabled by IER bit-3). The receiver issues an interrupt after the number of characters have reached the programmed trigger level. In this case the 552/552A FIFO may hold more characters than the programmed trigger level. Following the removal of a data byte, the user should recheck LSR bit-0 for additional characters. A Receive Time Out will not occur if the receive FIFO is empty. The time out counter is reset at the center of each stop bit received or each time the receive holding register (RHR) is read (see Figure 4, Receive Time-out Interrupt). The actual time out value is T (**T**ime out length in bits) = 4 X P (**P**rogrammed word length) + 12. To convert the time out value to a character value, the user has to consider the complete word length, including data information length, start bit, parity bit, and the size of stop bit, i.e., 1X, 1.5X, or 2X bit times.

Example -A: If the user programs a word length of 7, with no parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) +12 = 40 bit times. The character time will be equal to 40 / 9 = 4.4 characters, or as shown in the fully worked out example: T = [(programmed word length = 7) + (stop bit = 1) + (start bit = 1) = 9]. 40 (bit times divided by 9) = 4.4 characters.

Example -B: If the user programs the word length = 7, with parity and one stop bit, the time out will be:
T = 4 X 7(programmed word length) + 12 = 40 bit times. Character time = 40 / 10 [(programmed word length = 7) + (parity = 1) + (stop bit = 1) + (start bit = 1) = 4 characters.

Programmable Baud Rate Generator

The 552/552A supports high speed modem technologies that have increased input data rates by employing data compression schemes. For example a 33.6Kbps modem that employs data compression may require a 115.2Kbps input data rate. A 128.0Kbps ISDN modem that supports data compression may need an input data rate of 460.8Kbps. The 552/552A can support a standard data rate of 921.6Kbps.

Single baud rate generator is provided for the transmitter and receiver, allowing independent TX/RX channel control. The programmable Baud Rate Generator is capable of accepting an input clock up to 24 MHz, as required for supporting a 1.5Mbps data rate. The 552/552A requires that an external clock source be connected to the CLK input pin to clock the internal baud rate generator for standard or custom rates. (see Baud Rate Generator Programming below).

The generator divides the input 16X clock by any divisor from 1 to 2^{16} -1. The 552/552A divides the basic external clock by 16. The basic 16X clock provides table rates to support standard and custom applications using the

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same system design. The rate table is configured via the DLL and DLM internal register functions. Customized Baud Rates can be achieved by selecting the proper divisor values for the MSB and LSB sections of baud rate generator.

Programming the Baud Rate Generator Registers DLM (MSB) and DLL (LSB) provides a user capability for selecting the desired final baud rate. The example in Table 5 below, shows the selectable baud rate table available when using a 1.8432 MHz external clock input.

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Table 5, BAUD RATE GENERATOR PROGRAMMING TABLE (1.8432 MHz CLOCK):

Output Baud Rate MCR	Output 16 x Clock Divisor (Decimal)	User 16 x Clock Divisor (HEX)	DLM Program Value (HEX)	DLL Program Value (HEX)
50	2304	900	09	00
110	1047	417	04	17
150	768	300	03	00
300	384	180	01	80
600	192	C0	00	C0
1200	96	60	00	60
2400	48	30	00	30
4800	24	18	00	18
7200	16	10	00	10
9600	12	0C	00	0C
19.2k	6	06	00	06
38.4k	3	03	00	03
57.6k	2	02	00	02
115.2k	1	01	00	01

DMA Operation

The 552/552A FIFO trigger level provides additional flexibility to the user for block mode operation. LSR bits 5-6 provide an indication when the transmitter is empty or has an empty location(s). The user can optionally operate the transmit and receive FIFO's in the DMA mode (FCR bit-3). When the transmit and receive FIFO's are enabled and the DMA mode is deactivated (DMA Mode "0"), the 552/552A activates the interrupt output pin for each data transmit or receive operation. When DMA mode is activated (DMA Mode "1"), the user takes the advantage of block mode operation by loading or unloading the FIFO in a block sequence determined by the receive trigger level and the transmit FIFO. In this mode, the 552/552A sets the interrupt output pin when characters in the transmit FIFO is below 16, or the characters in the receive FIFO's are above the receive trigger level.

Power Down Mode

The 552 is designed to operate with low power consumption. The 552 (only) is designed with a special power down mode to further reduce power consumption when the chip is not being used. When MCR bit-7 and IER bit-5 are enabled (set to a logic 1), the 552 powers down. The use of two power down enable bits helps to prevent accidental software shut-down. The 552 will remain powered down until disabled by setting either IER bit-5 or MCR bit-7 to a logic 0.

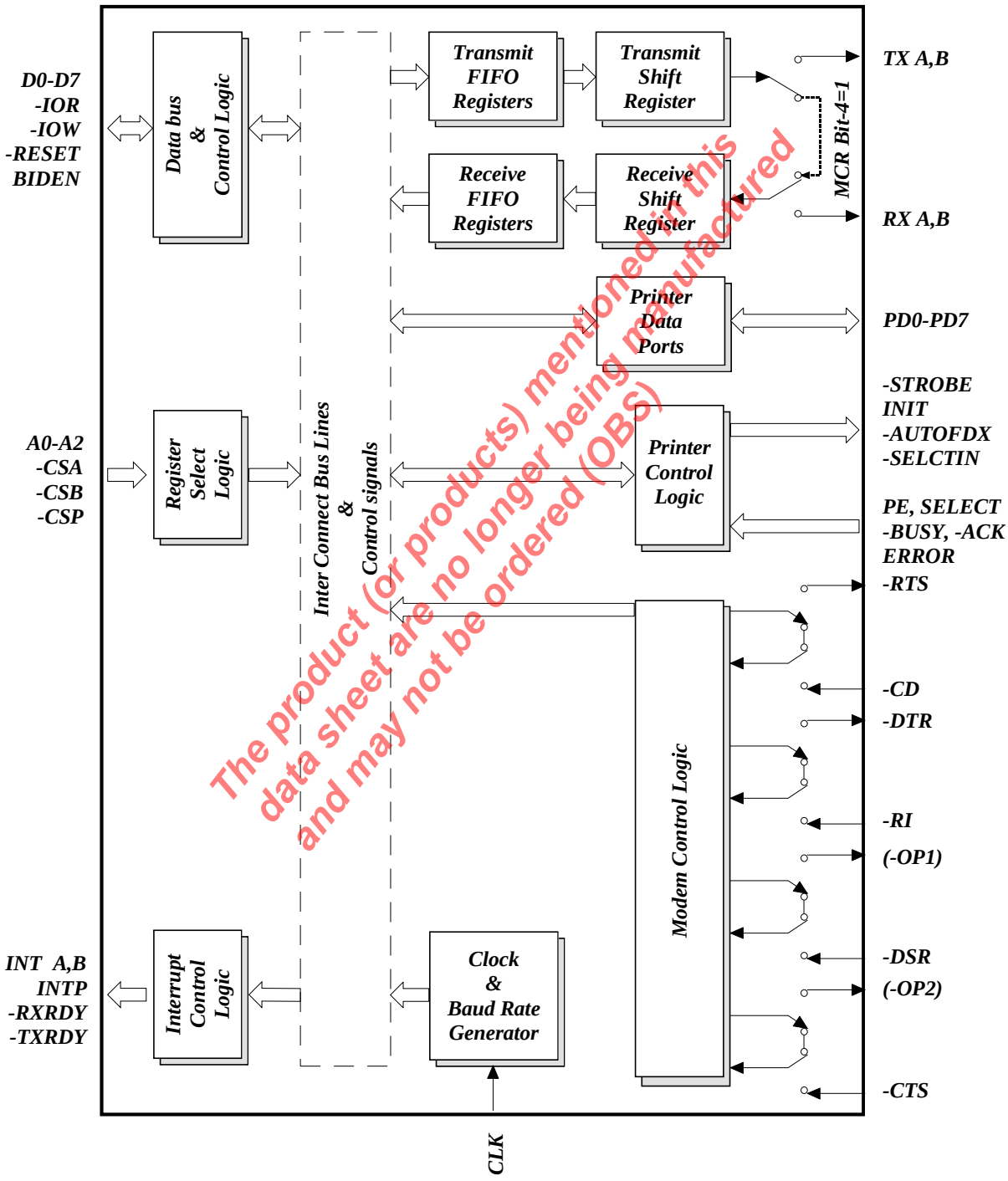
Loop-back Mode

The internal loop-back capability allows onboard diagnostics. In the loop-back mode the normal modem interface pins are disconnected and reconfigured for loop-back internally. MCR register bits 0-3 are used for controlling loop-back diagnostic testing. In the loop-back mode INT enable and MCR bit-2 in the MCR register (bits 2,3) control the modem -RI and -CD inputs respectively. MCR signals -DTR and -RTS (bits 0-1) are used to control the modem -CTS and -DSR inputs respectively. The transmitter output (TX) and the receiver input (RX) are disconnected from their associated interface pins, and instead are connected together internally (See Figure 6). The -CTS, -DSR, -CD, and -RI are disconnected from their normal modem control inputs pins, and instead are connected internally to -DTR, -RTS, INT enable and MCR bit-2. Loop-back test data is entered into the transmit holding register via the user data bus interface, D0-D7. The transmit UART serializes the data and passes the serial data to the receive UART via the internal loop-back connection. The receive UART converts the serial data back into parallel data that is then made available at the user data interface, D0-D7. The user optionally compares the received data to the initial transmitted data for verifying error free operation of the UART TX/RX circuits.

In this mode, the receiver and transmitter interrupts are fully operational. The Modem Control Interrupts are also operational. However, the interrupts can only be read using lower four bits of the Modem Control Register (MCR bits 0-3) instead of the four Modem Status Register bits 4-7. The interrupts are still controlled by the IER.

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Figure 6, INTERNAL LOOP-BACK MODE DIAGRAM



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Printer Port

The 552/552A contains a general purpose 8-bit parallel interface port that is designed to directly interface with a CENTRONICS Printer. A number of the control/ interrupt signals and the 8-bit data bus have been designed as bi-directional data buses. This allows the interface to function with other device parallel data bus applications. Signal -ACK is used to generate an -INTP interface interrupt that would normally be connected to the user CPU. -INTP can be made to follow the -ACK signal, normal mode (see Figure 7) or it can be configured for the latch mode. In the latch mode the interrupt is not cleared until printer status register (SR) is read. Another signal (INIT) can be made to function as an outgoing or incoming interrupt, or combined with other interrupts to provide a common wire-or interrupt output. Interface signals -STROBE, -AutoFDXT, and -SLCTIN are bi-directional and can be used as combinations of input and/or output functions. The signals have internal pull-up resistors and can be wire-or'd. Normally, -STROBE is used to strobe PD0-PD7 bus data into a printer input buffer. -SLCTIN normally selects the printer while AutoFDXT signals the printer to auto-linefeed. Other signals provide similar printer functions but are not bi-directional. The printer functions for these signals are described in table 1, Symbol Description.

The interface provides a mode steering signal called BIDEN. BIDEN controls the bi-directional 8-bit data bus (PD0-PD7) direction, input or output. When BIDEN is a logic 1 a single control bit (D5) in the control register sets the input or output mode. Setting BIDEN to a logic 0 however sets an IBM interface compatible mode. In this mode the bus direction (input/output) is set by eight data bits in the IOSEL register. An AA (Hex) pattern sets the input mode while a 55 (hex) pattern sets the output mode. I/O direction is depicted in Table 6 below.

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Table 6, PD0-PD7 I/O DIRECTION MODE SELECTION

PORT DIRECTION	BIDEN	CONTROL REGISTER (D5)	I/O SELECT REGISTER
Input mode	0	X (Note 4)	AA Hex
Output mode	0	X (Note 4)	55 Hex
Output mode	1	0	X (Note 4)
Input mode	1	1	X (Note 4)

Note: 4 = don't care

REGISTER FUNCTIONAL DESCRIPTIONS

The following table delineates the assigned bit functions for the eighteen 552/552A internal registers. The assigned bit functions are more fully defined in the following paragraphs.

Table 7, ST16C552/552A INTERNAL REGISTERS

A2 A1 A0	Register [Default] Note 5*	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
General Register Set: Note 1*									
0 0 0	RHR [XX]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 0	THR [XX]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	IER [00]	0	0	En Pwr down mode	0	Modem Status Interrupt	Receive Line Status interrupt	Transmit Holding Register interrupt	Receive Holding Register
0 1 0	FCR [00]	RCVR trigger (MSB)	RCVR trigger (LSB)	0	0	DMA mode select	XMIT FIFO reset	RCVR FIFO reset	FIFO enable
0 1 0	ISR [01]	FIFO's enabled	FIFO's enabled	0	0	INT priority bit-2	INT priority bit-1	INT priority bit-0	INT status
0 1 1	LCR [00]	divisor latch enable	set break	set parity	even parity	parity enable	stop bits	word length bit-1	word length bit-0
1 0 0	MCR [00]	Pwr down	0	0	loop back	INT A/B enable	[X]	-RTS	-DTR
1 0 1	LSR [60]	FIFO data error	THR & TSR empty	THR. empty	break interrupt	framing error	parity error	overrun error	receive data ready
1 1 0	MSR [X0]	CD	RI	DSR	CTS	delta -CD	delta -RI	delta -DSR	delta -CTS
1 1 1	SPR [FF]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
Special Register Set: Note *2									
0 0 0	DLL [XX]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
0 0 1	DLM [XX]	bit-15	bit-14	bit-13	bit-12	bit-11	bit-10	bit-9	bit-8

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A2 A1 A0	Register [Default] Note 5*	BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
Printer Port Register Set: Note 3*									
[X] 0 0	PR[00]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
[X] 0 0	PR[00]	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
[X] 0 1	SR[4F]	-Busy	-ACK	PE	SLCT	Error State	-IRQ	logic "1"	logic "1"
[X] 0 1	IOSEL	bit-7	bit-6	bit-5	bit-4	bit-3	bit-2	bit-1	bit-0
[X] 1 0	COM[E0]	logic "1"	logic "1"	logic "1"	-INTP Enable	-SLCTIN	INIT	-Auto FDXT	-STROBE
[X] 1 0	CON[00]	[X]	[X]	PD 0-7 IN/OUT	-INTP Enable	-SLCTIN	INIT	-Auto FDXT	-STROBE

Note 1* The General Register set is accessible only when CS A or CS B is a logic 0.
Note 2* The Baud Rate register set is accessible only when CS A or CS B is a logic 0 and LCR bit-7 is a logic 1.
Note 3*: Printer Port Register set is accessible only when -CSP is a logic 0 in conjunction with the states of the interface signal BIDEN and Printer Control Register bit-5 or IOSEL register.
Note 5* The value between the square brackets represents the register's initialized HEX value, X =N/A.

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MODEM (UART) REGISTER DESCRIPTIONS

Transmit (THR) and Receive (RHR) Holding Registers

The serial transmitter section consists of an 8-bit Transmit Hold Register (THR) and Transmit Shift Register (TSR). The status of the THR is provided in the Line Status Register (LSR). Writing to the THR transfers the contents of the data bus (D7-D0) to the THR, providing that the THR or TSR is empty. The THR empty flag in the LSR register will be set to a logic 1 when the transmitter is empty or when data is transferred to the TSR. Note that a write operation can be performed when the transmit holding register empty flag is set (logic 0 = FIFO full, logic 1= at least one FIFO location available).

The serial receive section also contains an 8-bit Receive Holding Register, RHR. Receive data is removed from the 552/552A and receive FIFO by reading the RHR register. The receive section provides a mechanism to prevent false starts. On the falling edge of a start or false start bit, an internal receiver counter starts counting clocks at the 16x clock rate. After 7 1/2 clocks the start bit time should be shifted to the center of the start bit. At this time the start bit is sampled and if it is still a logic 0 it is validated. Evaluating the start bit in this manner prevents the receiver from assembling a false character. Receiver status codes will be posted in the LSR.

Interrupt Enable Register (IER)

The Interrupt Enable Register (IER) masks the interrupts from receiver ready, transmitter empty, line status and modem status registers. These interrupts would normally be seen on the INT A,B output pins.

IER Vs Receive FIFO Interrupt Mode Operation

When the receive FIFO (FCR BIT-0 = a logic 1) and receive interrupts (IER BIT-0 = logic 1) are enabled, the receive interrupts and register status will reflect the following:

A) The receive data available interrupts are issued to the external CPU when the FIFO has reached the programmed trigger level. It will be cleared when the FIFO drops below the programmed trigger level.

B) FIFO status will also be reflected in the user accessible ISR register when the FIFO trigger level is reached. Both the ISR register status bit and the interrupt will be cleared when the FIFO drops below the trigger level.

C) The data ready bit (LSR BIT-0) is set as soon as a character is transferred from the shift register to the receive FIFO. It is reset when the FIFO is empty.

IER Vs Receive/Transmit FIFO Polled Mode Operation

When FCR BIT-0 equals a logic 1, resetting IER bits 0-3 enables the 552/552A in the FIFO polled mode of operation. Since the receiver and transmitter have separate bits in the LSR either or both can be used in the polled mode by selecting respective transmit or receive control bit(s).

A) LSR BIT-0 will be a logic 1 as long as there is one byte in the receive FIFO.

B) LSR BIT 1-4 will provide the type of errors encountered, if any.

C) LSR BIT-5 will indicate when the transmit FIFO is empty.

D) LSR BIT-6 will indicate when both the transmit FIFO and transmit shift register are empty.

E) LSR BIT-7 will indicate any FIFO data errors.

IER BIT-0:
This interrupt will be issued when the FIFO has reached the programmed trigger level or is cleared when the FIFO drops below the trigger level in the FIFO mode of operation.
Logic 0 = Disable the receiver ready interrupt. (normal default condition)
Logic 1 = Enable the receiver ready interrupt.

IER BIT-1:
This interrupt will be issued whenever the THR is empty and is associated with bit-1 in the LSR register.
Logic 0 = Disable the transmitter empty interrupt. (normal default condition)
Logic 1 = Enable the transmitter empty interrupt.

IER BIT-2:
This interrupt will be issued whenever a fully assembled receive character is transferred from the RSR to the RHR/FIFO, i.e., data ready, LSR bit-0.
Logic 0 = Disable the receiver line status interrupt. (normal default condition)
Logic 1 = Enable the receiver line status interrupt.

IER BIT-3:
Logic 0 = Disable the modem status register interrupt. (normal default condition)
Logic 1 = Enable the modem status register interrupt.

IER BIT -4:
Not Used - initialized to a logic 0.

IER BIT-5: (ST16C552 only)
Logic 0 = Disable the power down mode. (normal default condition). The ST16C552A does not support the power down mode and this bit is set to “0”.
Logic 1 = Enable the power down mode (MCR bit-7 must also be a logic 1 before power down will be activated).

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IER BIT 6-7:
Not Used - initialized to a logic 0.

FIFO Control Register (FCR)

This register is used to enable the FIFO's, clear the FIFO's, set the receive FIFO trigger levels, and select the DMA mode. The DMA, and FIFO modes are defined as follows:

DMA MODE
Mode 0 Set and enable the interrupt for each single transmit or receive operation, and is similar to the ST16C450 mode. Transmit Ready (-TXRDY) will go to a logic 0 when ever an empty transmit space is available in the Transmit Holding Register (THR). Receive Ready (-RXRDY) will go to a logic 0 whenever the Receive Holding Register (RHR) is loaded with a character.
Mode 1 Set and enable the interrupt in a block mode operation. The transmit interrupt is set when the transmit FIFO is below the programmed trigger level. -TXRDY remains a logic 0 as long as one empty FIFO location is available. The receive interrupt is set when the receive FIFO fills to the programmed trigger level. However the FIFO continues to fill regardless of the programmed level until the FIFO is full. -RXRDY remains a logic 0 as long as the FIFO fill level is above the programmed trigger level.

FCR BIT-0:
Logic 0 = Disable the transmit and receive FIFO. (normal default condition)
Logic 1 = Enable the transmit and receive FIFO. This bit must be a "1" when other FCR bits are written to or they will not be programmed.

FCR BIT-1:
Logic 0 = No FIFO receive reset. (normal default condition)
Logic 1 = Clears the contents of the receive FIFO and resets the FIFO counter logic (the receive shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.

FCR BIT-2:
Logic 0 = No FIFO transmit reset. (normal default condition)
Logic 1 = Clears the contents of the transmit FIFO and resets the FIFO counter logic (the transmit shift register is not cleared or altered). This bit will return to a logic 0 after clearing the FIFO.

FCR BIT-3:
Logic 0 = Set DMA mode "0". (normal default condition)
Logic 1 = Set DMA mode "1."

Transmit operation in mode "0":
When the 552/552A is in the ST16C450 mode (FIFO's disabled, FCR bit-0 = logic 0) or in the FIFO mode (FIFO's enabled, FCR bit-0 = logic 1, FCR bit-3 = logic 0) and when there are no characters in the transmit FIFO or transmit holding register, the -TXRDY pin will be a logic 0. Once active the -TXRDY pin will go to a logic 1 after the first character is loaded into the transmit holding register.

Receive operation in mode "0":
When the 552/552A is in mode "0" (FCR bit-0 = logic 0) or in the FIFO mode (FCR bit-0 = logic 1, FCR bit-3 = logic 0) and there is at least one character in the receive FIFO, the -RXRDY pin will be a logic 0. Once active the -RXRDY pin will go to a logic 1 when there are no more characters in the receiver.

Transmit operation in mode "1":
When the 552/552A is in FIFO mode (FCR bit-0 = logic 1, FCR bit-3 = logic 1), the -TXRDY pin will be a logic 1 when the transmit FIFO is completely full. It will be a logic 0 if one or more FIFO locations are empty.

Receive operation in mode "1":
When the 552/552A is in FIFO mode (FCR bit-0 = logic 1, FCR bit-3 = logic 1) and the trigger level has been reached, or a Receive Time Out has occurred, the -RXRDY pin will go to a logic 0. Once activated, it will go to a logic 1 after there are no more characters in the FIFO.

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FCR BIT 4-5:
Not Used - initialized to a logic 0.

FCR BIT 6-7: (logic 0 or cleared is the default condition, RX trigger level = 1)
These bits are used to set the trigger level for the receive FIFO interrupt.

An interrupt is generated when the number of characters in the FIFO equals the programmed trigger level. However the FIFO will continue to be loaded until it is full.

BIT-7	BIT-6	RX FIFO trigger level
0	0	01
0	1	04
1	0	08
1	1	14

Interrupt Status Register (ISR)

The 552/552A provides four levels of prioritized interrupts to minimize external software interaction. The Interrupt Status Register (ISR) provides the user with four interrupt status bits. Performing a read cycle on the ISR will provide the user with the highest pending interrupt level to be serviced. No other interrupts are acknowledged until the pending interrupt is serviced. Whenever the interrupt status register is read, the interrupt status is cleared. However it should be noted that only the current pending interrupt is cleared by the read. A lower level interrupt may be seen after rereading the interrupt status bits. The Interrupt Source Table 8 (below) shows the data values (bits 0-3) for the four prioritized interrupt levels and the interrupt sources associated with each of these interrupt levels:

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Table 8, INTERRUPT SOURCE TABLE

Priority Level	[ISR BITS] Bit-3	Bit-2	Bit-1	Bit-0	Source of the interrupt
1	0	1	1	0	LSR (Receiver Line Status Register)
2	0	1	0	0	RXRDY (Received Data Ready)
2	1	1	0	0	RXRDY (Receive Data time out)
3	0	0	1	0	TXRDY (Transmitter Holding Register Empty)
4	0	0	0	0	MSR (Modem Status Register)

ISR BIT-0:
Logic 0 = An interrupt is pending and the ISR contents may be used as a pointer to the appropriate interrupt service routine.
Logic 1 = No interrupt pending. (normal default condition)

ISR BIT 1-3: (logic 0 or cleared is the default condition)
These bits indicate the source for a pending interrupt at interrupt priority levels 1, 2, and 3 (See Interrupt Source Table).

ISR BIT 4-5: (logic 0 or cleared is the default condition)
Not Used - initialized to a logic 0.

ISR BIT 6-7: (logic 0 or cleared is the default condition)
These bits are set to a logic 0 when the FIFO's are not being used in the 16C450 mode. They are set to a logic 1 when the FIFO's are enabled in the 16C552/552A mode.

Line Control Register (LCR)

The Line Control Register is used to specify the asynchronous data communication format. The word length, the number of stop bits, and the parity are selected by writing the appropriate bits in this register.

LCR BIT 0-1: (logic 0 or cleared is the default condition)
These two bits specify the word length to be transmitted or received.

BIT-1	BIT-0	Word length
0	0	5
0	1	6
1	0	7
1	1	8

LCR BIT-2: (logic 0 or cleared is the default condition)
The length of stop bit is specified by this bit in conjunction with the programmed word length.

BIT-2	Word length	Stop bit length (Bit time(s))
0	5,6,7,8	1
1	5	1-1/2
1	6,7,8	2

LCR BIT-3:
Parity or no parity can be selected via this bit.
Logic 0 = No parity. (normal default condition)
Logic 1 = A parity bit is generated during the transmission, receiver checks the data and parity for transmission errors.

LCR BIT-4:
If the parity bit is enabled with LCR bit-3 set to a logic 1, LCR BIT-4 selects the even or odd parity format.
Logic 0 = ODD Parity is generated by forcing an odd number of logic 1's in the transmitted data. The receiver must be programmed to check the same format. (normal default condition)
Logic 1 = EVEN Parity is generated by forcing an even the number of logic 1's in the transmitted. The receiver must be programmed to check the same format.

LCR BIT-5:
If the parity bit is enabled, LCR BIT-5 selects the forced parity format.
LCR BIT-5 = logic 0, parity is not forced. (normal default condition)
LCR BIT-5 = logic 1 and LCR BIT-4 = logic 0, parity bit is forced to a logical 1 for the transmit and receive data.
LCR BIT-5 = logic 1 and LCR BIT-4 = logic 1, parity bit is forced to a logical 0 for the transmit and receive data.

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LCR Bit-5	LCR Bit-4	LCR Bit-3	Parity selection
X	X	0	No parity
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Force parity odd parity
1	1	1	Forced even parity

LCR BIT-6:
When enabled the Break control bit causes a break condition to be transmitted (the TX output is forced to a logic 0 state). This condition exists until disabled by setting LCR bit-6 to a logic 0.
Logic 0 = No TX break condition. (normal default condition)
Logic 1 = Forces the transmitter output (TX) to a logic 0 for alerting the remote receiver to a line break condition.

LCR BIT-7:
The internal baud rate counter latch and Enhance Feature mode enable.
Logic 0 = Divisor latch disabled. (normal default condition)
Logic 1 = Divisor latch and enhanced feature register enabled.

Modem Control Register (MCR)

This register controls the interface with the modem or a peripheral device.

MCR BIT-0:
Logic 0 = Force -DTR output to a logic 1. (normal default condition)
Logic 1 = Force -DTR output to a logic 0.

MCR BIT-1:
Logic 0 = Force -RTS output to a logic 1. (normal default condition)
Logic 1 = Force -RTS output to a logic 0.

MCR BIT-2:
This bit is used in the Loop-back mode only. In the loop-back mode this bit is use to write the state of the modem -RI interface signal.

*MCR BIT-3: (*Used to control the modem -CD signal in the loop-back mode.)
Logic 0 = Forces INT (A-B) outputs to the three state mode. (normal default condition) In the Loop-back mode, sets -CD internally to a logic 1.
Logic 1 = Forces the INT (A-B) outputs to the active mode. In the Loop-back mode, sets -CD internally to a logic 0.

MCR BIT-4:
Logic 0 = Disable loop-back mode. (normal default condition)
Logic 1 = Enable local loop-back mode (diagnostics).

MCR BIT 5-6:
Not Used - initialized to a logic 0.

MCR BIT-7:
Logic 0 = Disable power down mode. (normal, default condition, 552 only)
Logic 1 = Enable power down mode (IER bit-5 must also be a logic 1 before power down will be activated).

Line Status Register (LSR)

This register provides the status of data transfers between. the 552/552A and the CPU.

LSR BIT-0:
Logic 0 = No data in receive holding register or FIFO. (normal default condition)
Logic 1 = Data has been received and is saved in the receive holding register or FIFO.

LSR BIT-1:
Logic 0 = No overrun error. (normal default condition)
Logic 1 = Overrun error. A data overrun error occurred in the receive shift register. This happens when additional data arrives while the FIFO is full. In this case the previous data in the shift register is overwritten. Note that under this condition the data byte in the receive shift register is not transferred into the FIFO, therefore the data in the FIFO is not corrupted by the error.

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LSR BIT-2:
Logic 0 = No parity error. (normal default condition)
Logic 1 = Parity error. The receive character does not have correct parity information and is suspect. In the FIFO mode, this error is associated with the character at the top of the FIFO.

LSR BIT-3:
Logic 0 = No framing error. (normal default condition)
Logic 1 = Framing error. The receive character did not have a valid stop bit(s). In the FIFO mode this error is associated with the character at the top of the FIFO.

LSR BIT-4:
Logic 0 = No break condition. (normal default condition)
Logic 1 = The receiver received a break signal (RX was a logic 0 for one character frame time). In the FIFO mode, only one break character is loaded into the FIFO.

LSR BIT-5:
This bit is the Transmit Holding Register Empty indicator. This bit indicates that the UART is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to CPU when the THR interrupt enable is set. The THR bit is set to a logic 1 when a character is transferred from the transmit holding register into the transmitter shift register. The bit is reset to logic 0 concurrently with the loading of the transmitter holding register by the CPU. In the FIFO mode this bit is set when the transmit FIFO is empty; it is cleared when at least 1 byte is written to the transmit FIFO.

LSR BIT-6:
This bit is the Transmit Empty indicator. This bit is set to a logic 1 whenever the transmit holding register and the transmit shift register are both empty. It is reset to logic 0 whenever either the THR or TSR contains a data character. In the FIFO mode this bit is set to one whenever the transmit FIFO and transmit shift register are both empty.

LSR BIT-7:
Logic 0 = No Error. (normal default condition)
Logic 1 = At least one parity error, framing error or break indication is in the current FIFO data. This bit is cleared when RHR register is read.

Modem Status Register (MSR)

This register provides the current state of the control interface signals from the modem, or other peripheral device that the 552/552A is connected to. Four bits of this register are used to indicate the changed information. These bits are set to a logic 1 whenever a control input from the modem changes state. These bits are set to a logic 0 whenever the CPU reads this register.

MSR BIT-0:
Logic 0 = No -CTS Change (normal default condition)
Logic 1 = The -CTS input to the 552/552A has changed state since the last time it was read. A modem Status Interrupt will be generated.

MSR BIT-1:
Logic 0 = No -DSR Change. (normal default condition)
Logic 1 = The -DSR input to the 552/552A has changed state since the last time it was read. A modem Status Interrupt will be generated.

MSR BIT-2:
Logic 0 = No -RI Change. (normal default condition)
Logic 1 = The -RI input to the 552/552A has changed from a logic 0 to a logic 1. A modem Status Interrupt will be generated.

MSR BIT-3:
Logic 0 = No -CD Change. (normal default condition)
Logic 1 = Indicates that the -CD input to the has changed state since the last time it was read. A modem Status Interrupt will be generated.

MSR BIT-4:
Normally MSR bit-4 bit is the compliment of the -CTS input. However in the loop-back mode, this bit is equivalent to the RTS bit in the MCR register.

MSR BIT-5:
DSR (active high, logical 1). Normally this bit is the compliment of the -DSR input. In the loop-back mode, this bit is equivalent to the DTR bit in the MCR register.

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MSR BIT-6:
RI (active high, logical 1). Normally this bit is the compliment of the -RI input. In the loop-back mode this bit is equivalent to MCR bit-2 in the MCR register.

MSR BIT-7:
CD (active high, logical 1). Normally this bit is the compliment of the -CD input. In the loop-back mode this bit is equivalent to MCR bit-3 in the MCR register.

Note: Whenever any MSR bit 0-3: is set to logic "1", a MODEM Status Interrupt will be generated.

Scratchpad Register (SPR)

The ST16C552/552A provides a temporary data register to store 8 bits of user information.

PRINTER PORT REGISTER DESCRIPTIONS

Port Register (PR)
PR BIT 0-7:
Printer Data port (Bi-directional) - These pins are the eight bit data bus for transferring information to or from an external device (usually a printer). D0 is the least significant bit. PD7-PD0 are latched during a write cycle (output mode).

I/O Select Register (IOSEL)

This bit is used in conjunction with the state of BIDEN to set the direction (input/output) of the PD7-PD0 data bus. This register is used only when BIDEN is a logic 0.
Logic 55 (Hex) + BIDEN 0 = PD7-PD0 are set for output mode
Logic AA (Hex) + BIDEN 0 = PD7-PD0 are set for input mode

Status Register (SR)
This register provides the printer port input logical states and the status of the interrupt -INTP based on the condition of the -ACK printer port interface signal. The logical state of these pins is dependent on external interface signals.

SR BIT 1-0:
Not Used - initialized to a logic 1.

SR BIT-2:
Logic 0 = an interrupt is pending
When INTSEL is a logic 0, SR bit-2 basically tracks the -ACK input interface pin (returns to a logic 1 when the -ACK input returns to a logic 1). However when INTSEL is a logic 1, the latched mode is selected, SR bit-2 goes to a logic 0 with the -ACK input but does not return to a logic 1 until the end of the read cycle, i.e., reading SR will set this bit to a logic 1.
Logic 1 = no interrupt is pending. (normal inactive state)

SR BIT-3:
Logic 0 = -ERROR input is a logic 0.
Logic 1 = -ERROR input is a logic 1. (normal inactive state)

SR BIT-4:
Logic 0 = SLCT input is a logic 0. (normal inactive state)
Logic 1 = SLCT input is a logic 1.

SR BIT-5:
Logic 0 = PE input is a logic 0. (normal inactive state)
Logic 1 = PE input is a logic 1.

SR BIT-6:
Logic 0 = -ACK input is a logic 0.
Logic 1 = -ACK input is a logic 1. (normal inactive state)

SR BIT-7:
Logic 0 = BUSY input is a logic 0
Logic 1 = BUSY input is a logic 1 (normal inactive state)

Command Register (COM)

This register provides the printer port input logical states and the status of the printer interrupt INIT, which is based on the state of CON bit-1.

COM BIT-0:
-STROBE is a bi-directional signal with an open

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source driver and internal pull-up so that it may be wire-or'd with other outputs. COM bit-1 is used to read status while CON bit 1 is used to set an output state. If it is to function as an input, CON bit-1 shall be set to a logic 1 first.
Logic 0 = -STROBE pin is a logic 1. (normal default condition)
Logic 1 = -STROBE pin is a logic 0.

COM BIT-1:
-AutoFDXT is a bi-directional signal with an open source driver and internal pull-up so that it may be wire-or'd with other outputs. COM bit-1 is used to read status while CON bit 1 is used to set an output state. If it is to function as an input, CON bit-1 shall be set to a logic 1 first.
Logic 0 = -AutoFDXT pin is a logic 1. (normal default condition)
1= -AutoFDXT pin is a logic 0.

COM BIT-2:
INIT is a bi-directional signal with an open source driver and internal pull-up so that it may be wire-or'd with other outputs. COM bit-2 is used to read status while CON bit 2 is used to set an output state. If it is to function as an input, CON bit-1 shall be set to a logic 1 first.
Logic 0 = INIT pin is a logic 0. (normal default condition)
Logic 1 = INIT pin is a logic 1.

COM BIT-3:
-SLCTIN is a bi-directional signal with an open source driver and internal pull-up so that it may be wire-or'd with other outputs. COM bit-1 is used to read status while CON bit 1 is used to set an output state. If it is to function as an input, CON bit-1 shall be set to a logic 1 first.
Logic 0 = -SLCTIN pin is a logic 1 (normal default condition)
Logic 1 = -SLCTIN pin is a logic 0

COM BIT-4:
This bit allows the state of -INTP to be read back by the external CPU.
Logic 0 = Interrupt (-INTP output) is disabled (normal default condition)
Logic 1 = Interrupt (-INTP output) is enabled

COM BIT 5-7:
Not Used - initialized to a logic 1.

Control Register (CON)

This register provides control of the printer port output logical states and controls the printer interrupts INIT and -INTP. With the exception of PD 0-7 IN/OUT, the status of this register may be read by reading the COM register.

CON BIT-0:
The -STROBE output control bit is under software control, i.e., the hardware will not generate a strobe. It is up to software to return the state of -STROBE to the inactive (logic 1) state. The hardware driver is open drain so that -STROBE may be wire-or'd. The state of this bit can be read using COM bit-0.
Logic 0 = -STROBE output is set to a logic 1. (normal default condition)
Logic 1 = -STROBE output is set to a logic 0.

CON BIT-1:
The -AutoFDXT output control bit is set by software using CON bit-1. The hardware driver is open drain so that -AutoFDXT may be wire-or'd. The state of this bit can be read using COM bit-1.
Logic 0 = -AutoFDXT output is set to a logic 1. (normal default condition)
Logic 1 = -AutoFDXT output is set to a logic 0.

CON BIT-2:
The INIT output control bit is set by software using CON bit-2. The hardware driver is open drain so that INIT may be wire-or'd. The state of this bit can be read using COM bit-2.
Logic 0 = INIT output is set to a logic 0. (normal default condition)
Logic 1 = INIT output is set to a logic 1.

CON BIT-3:
The -SLCTIN output control bit is set by software using CON bit-3. The hardware driver is open drain so that -AutoFDXT may be wire-or'd. The state of this bit can be read using COM bit-3.

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Logic 0 = -SLCTIN output is set to a logic 1. (normal default condition)
Logic 1 = -SLCTIN output is set to a logic 0.

CON BIT-4:
This bit enables or masks the printer interrupt output -INTP. The state of this bit can be read using COM bit-4.
Logic 0 = Disable -INTP output. (normal default condition)
Logic 1 = Enable -INTP output.

CON BIT-5:
This bit is used in conjunction with the state of BIDEN to set the direction (input/output) of the PD7-PD0 data bus.
Logic 0 + BIDEN 1 = PD7-PD0 are set for output mode (normal default condition)
Logic 1 + BIDEN 1 = PD7-PD0 are set for input mode

CON BIT 6-7:
Not Used - initialized to a logic 1.

ST16C552/552A EXTERNAL RESET CONDITION

REGISTERS (UART)	RESET STATE
IER	BITS 0-7=0
ISR	ISR BIT-0=1, ISR BITS 1-7=0
LCR	LCR BITS 0-7=0
MCR	MCR BITS 0-7=0
LSR	LSR BITS 0-4=0, LSR BITS 5-6=1 LSR, BIT 7=0
MSR	MSR BITS 0-3=0, MSR BITS 4-7=input signals
FCR	FCR BITS 0-7=0

REGISTERS Printer Port	RESET STATE
IOSEL	IOSEL BITS-0-7=0
SR	SR BITS 0-1=1, BITS 2-7=input signals
COM	COM BITS 0-4=0, BITS 5-7=1
CON	CON BITS 0-5=0, BITS 6-7=1

SIGNALS	RESET STATE
TX A/B	High
-RTS A/B	High
-DTR A/B	High
INT A/B, P	Three state mode
-RXRDY A/B	High
-TXRDY A/B	Low
PD0-PD7	Low, output mode
-STROBE	High, output mode
-AutoFDXT	High, output mode
INIT	Low, output mode
-SLCTIN	High, output mode

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AC ELECTRICAL CHARACTERISTICS

T_A=0° - 70°C (-40° - +85°C for Industrial grade packages), Vcc=3.3 - 5.0 V ± 10% unless otherwise specified.

Symbol	Parameter	Limits 3.3		Limits 5.0		Units	Conditions
		Min	Max	Min	Max		
T_{1w},T_{2w}	Clock pulse duration	17		17		ns	
T_{3w}	Oscillator/Clock frequency		8		24	MHz	
T_{6s}	Address setup time	5		0		ns	
T_{7d}	-IOR delay from chip select	10		10		ns	
T_{7w}	-IOR strobe width	35		25		ns	
T_{7h}	Chip select hold time from -IOR	0		0		ns	
T_{9d}	Read cycle delay	40		30		ns	
T_{12d}	Delay from -IOR to data		35		25	ns	
T_{12h}	Data disable time		25		15	ns	
T_{13d}	-IOW delay from chip select	10		10		ns	
T_{13w}	-IOW strobe width	40		25		ns	
T_{13h}	Chip select hold time from -IOW	0		0		ns	
T_{15d}	Write cycle delay	40		30		ns	
T_{16s}	Data setup time	20		15		ns	
T_{16h}	Data hold time	5		5		ns	
T_{17d}	Delay from -IOW to output		50		40	ns	100 pF load
T_{18d}	Delay to set interrupt from MODEM input		40		35	ns	100 pF load
T_{19d}	Delay to reset interrupt from -IOR		40		35	ns	100 pF load
T_{20d}	Delay from stop to set interrupt		1		1	Rclk	
T_{21d}	Delay from -IOR to reset interrupt		45		40	ns	100 pF load
T_{22d}	Delay from stop to interrupt		45		40	ns	
T_{23d}	Delay from initial INT reset to transmit start	8	24	8	24	Rclk	
T_{24d}	Delay from -IOW to reset interrupt		45		40	ns	
T_{25d}	Delay from stop to set -RxRdy		1		1	Rclk	
T_{26d}	Delay from -IOR to reset -RxRdy		45		40	ns	
T_{27d}	Delay from -IOW to set -TxRdy		45		40	ns	
T_{28d}	Delay from start to reset -TxRdy		8		8	Rclk	
T_{39w}	-ACK pulse width	75		75		ns	
T_{40s}	PD7 - PD0 setup time	15		10		ns	
T_{41h}	PD7 - PD0 hold time	30		25		ns	
T_{42d}	Delay from -ACK low to interrupt low	10		5		ns	
T_{43d}	Delay from -IOR to reset interrupt	10		5		ns	
T_R	Reset pulse width	40		40		ns	
N	Baud rate devisor	1	2^{16}-1	1	2^{16}-1	Rclk	

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ABSOLUTE MAXIMUM RATINGS

Supply range	7 Volts
Voltage at any pin	GND - 0.3 V to VCC +0.3 V
Operating temperature	-40° C to +85° C
Storage temperature	-65° C to 150° C
Package dissipation	500 mW

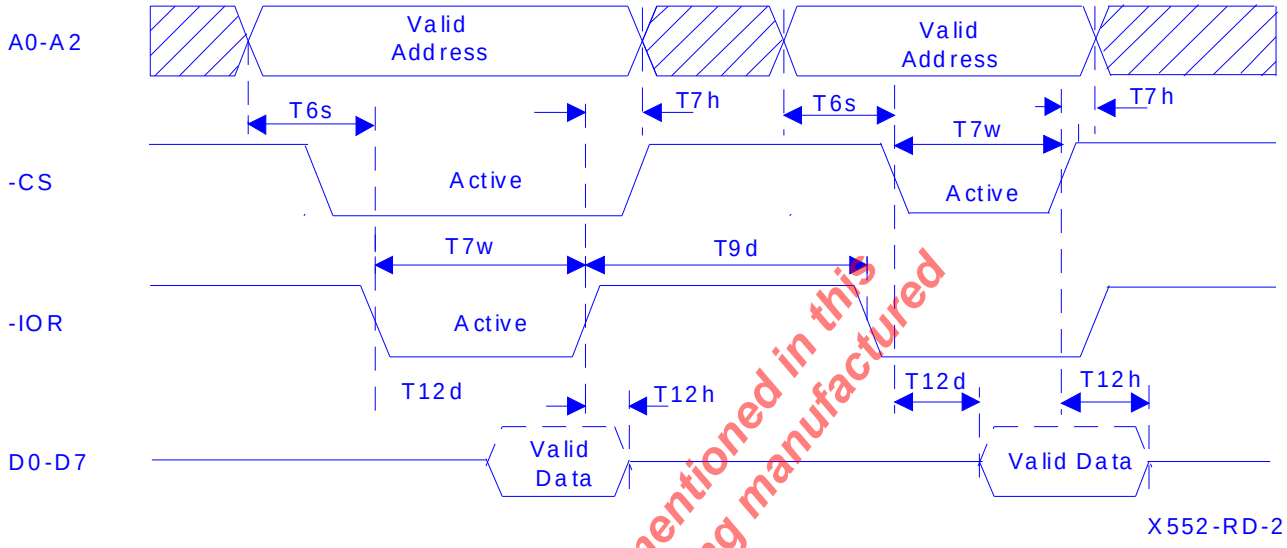
DC ELECTRICAL CHARACTERISTICS

T_A=0° - 70°C (-40° - +85°C for Industrial grade packages), Vcc=2.97 - 5.5V unless otherwise specified.

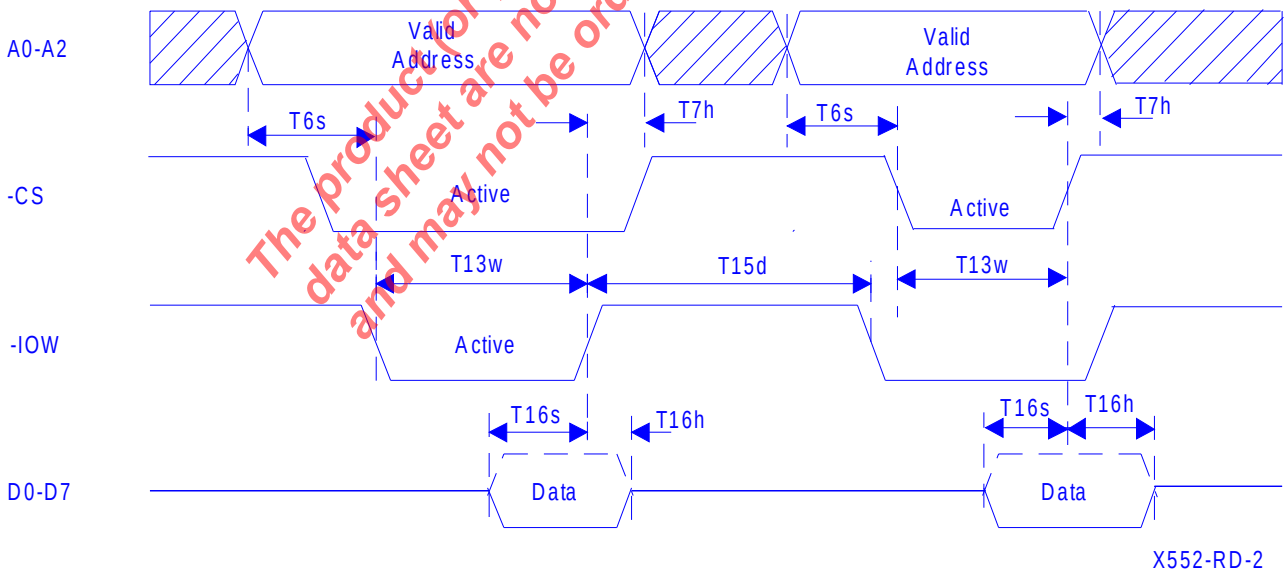
Symbol	Parameter	Limits 3.3		Limits 5.0		Units	Conditions
		Min	Max	Min	Max		
V_{ILCK}	Clock input low level	-0.3	0.6	-0.5	0.6	V	
V_{IHCK}	Clock and printer port input high level	2.4	VCC	3.0	VCC	V	
V_{IL}	Input low level	-0.3	0.8	-0.5	0.8	V	
V_{IH}	Input high level (Rev "E" and older)	2.0	VCC	2.2	VCC	V	
V_{IH}	Input high level (Rev "F" and newer)	2.0	5.5	2.2	5.5	V	
V_{OL}	Output low level on all outputs				0.4	V	I_{OL}= 4 mA
V_{OL}	Output low level on all outputs		0.4			V	I_{OL}= 4 mA
V_{OH}	Output high level			2.4		V	I_{OH}= -4 mA
V_{OH}	Output high level	2.0				V	I_{OH}= -1 mA
I_{IL}	Input leakage		±10		±10	µA	
I_{CL}	Clock leakage		±10		±10	µA	
I_{CC}	Avg power supply current		1.5		3	mA	
C_P	Input capacitance		5		5	pF	
R_{IN}	Internal pull-up resistance	9			22	kΩ	

Note: See the Symbol Description Table, for a listing of pins having internal pull-up resistors.

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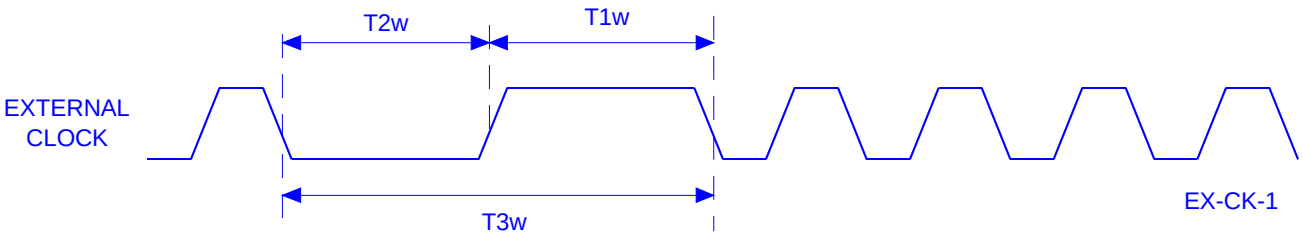


General read timing



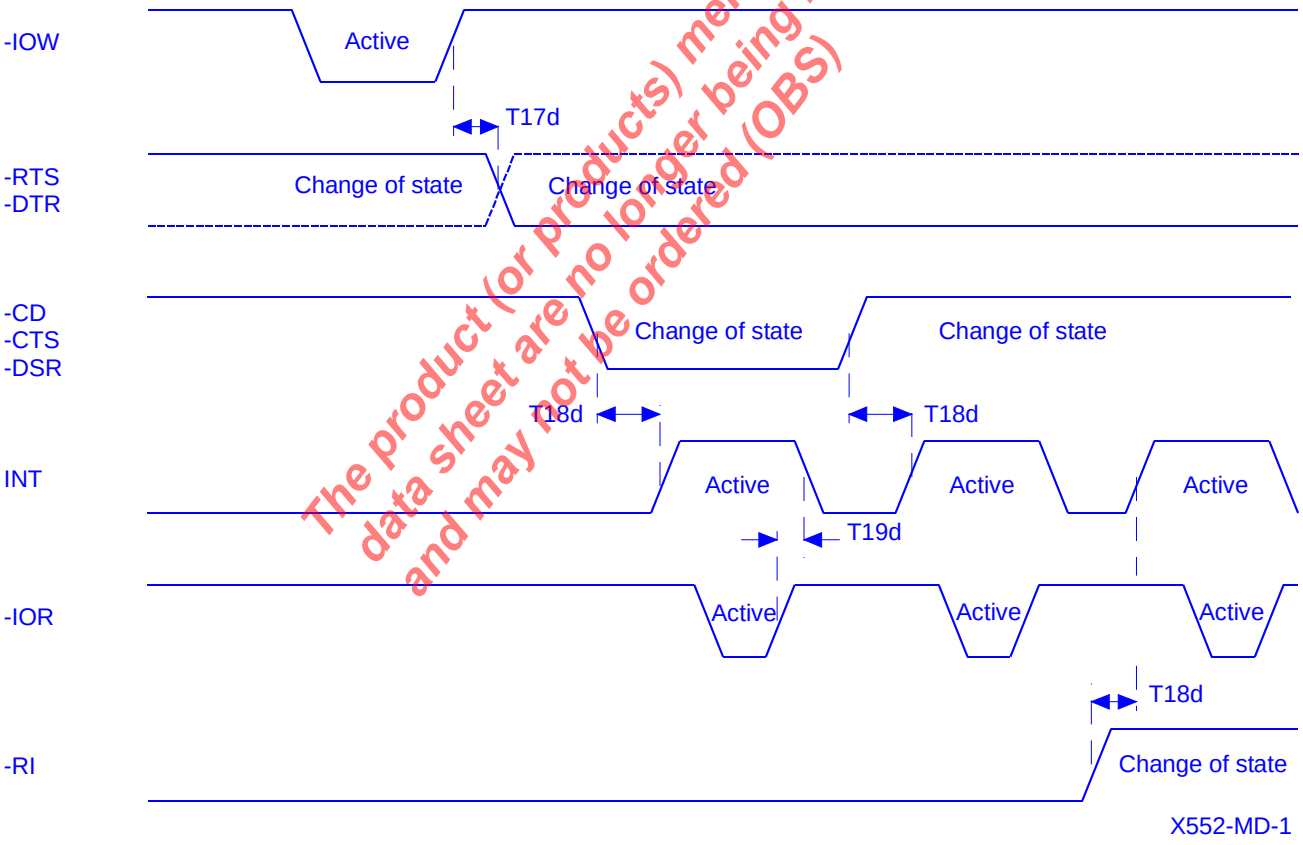
General write timing

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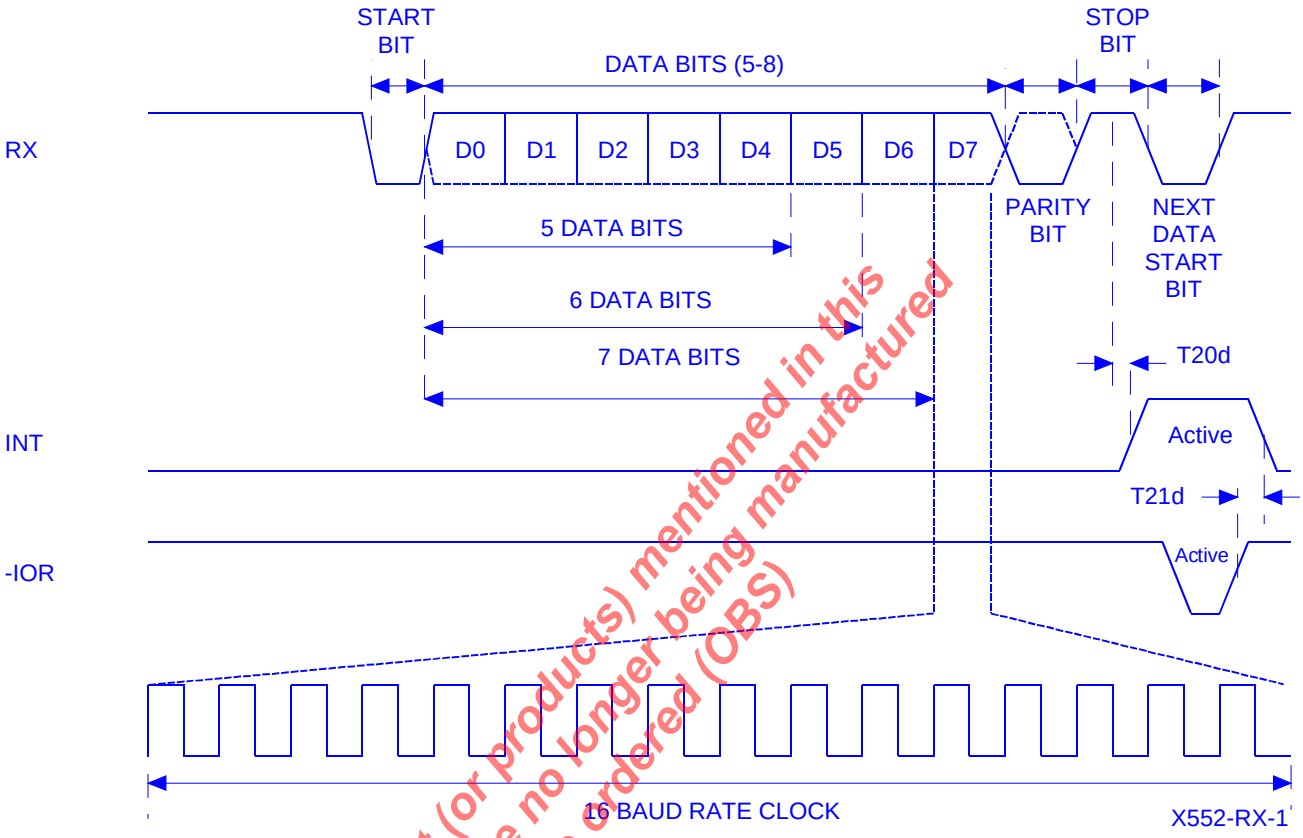


External clock timing

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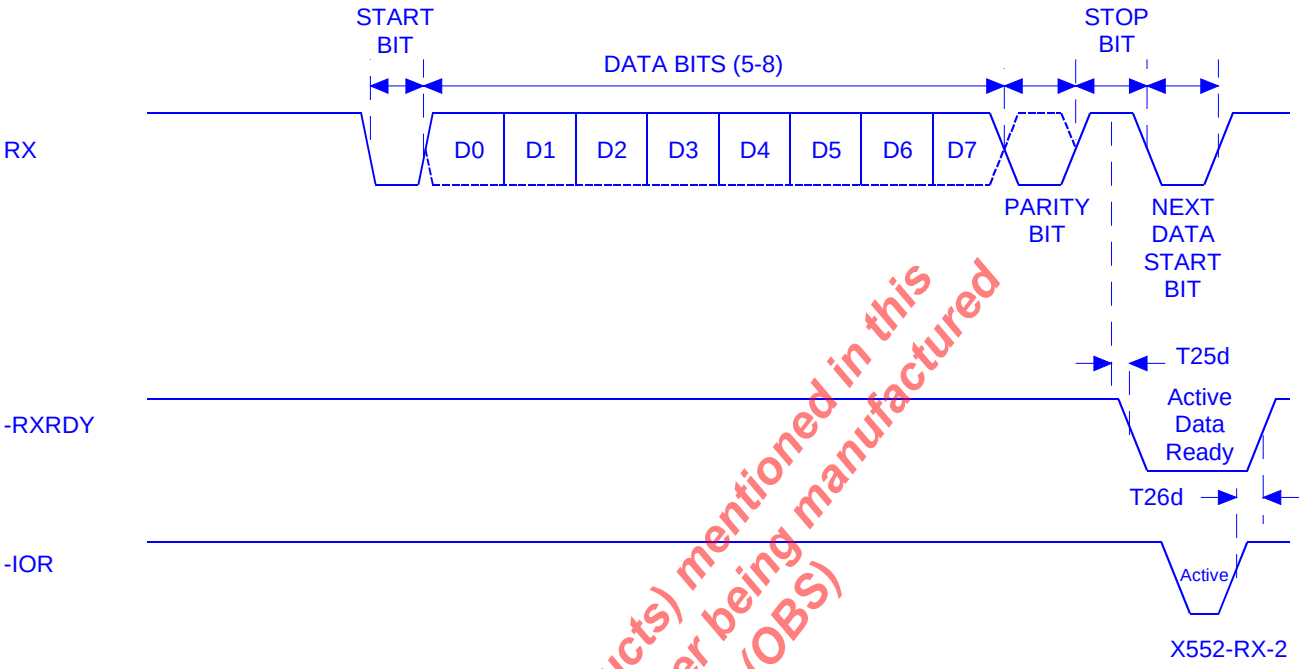


Modem input/output timing



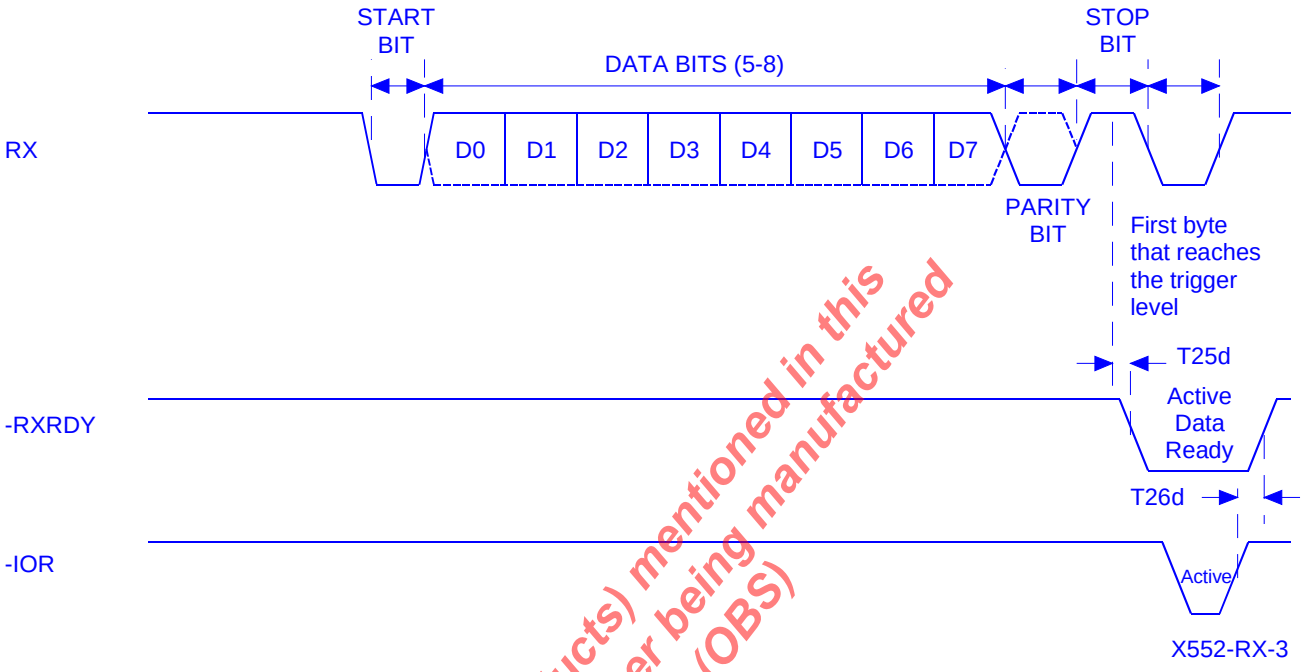
Receive timing

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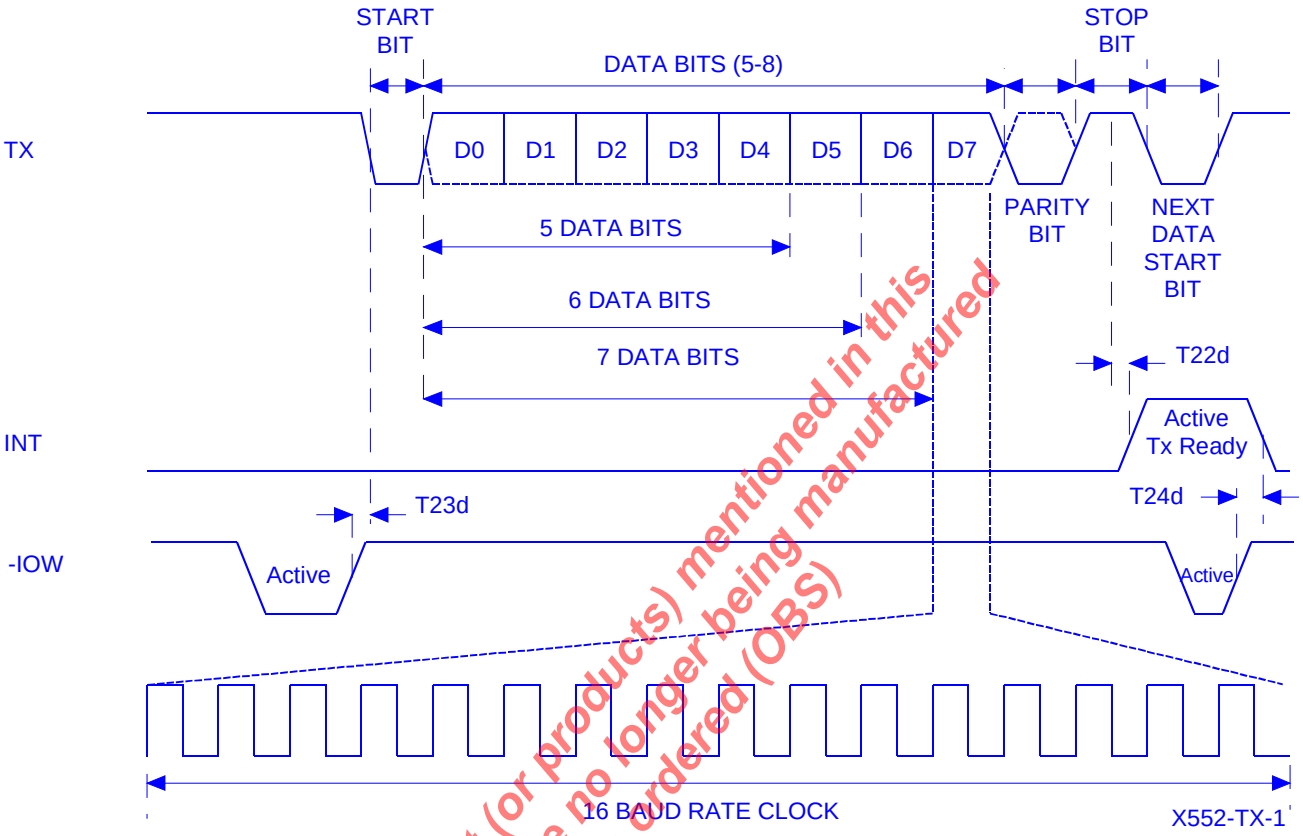
Receive ready timing in none FIFO mode

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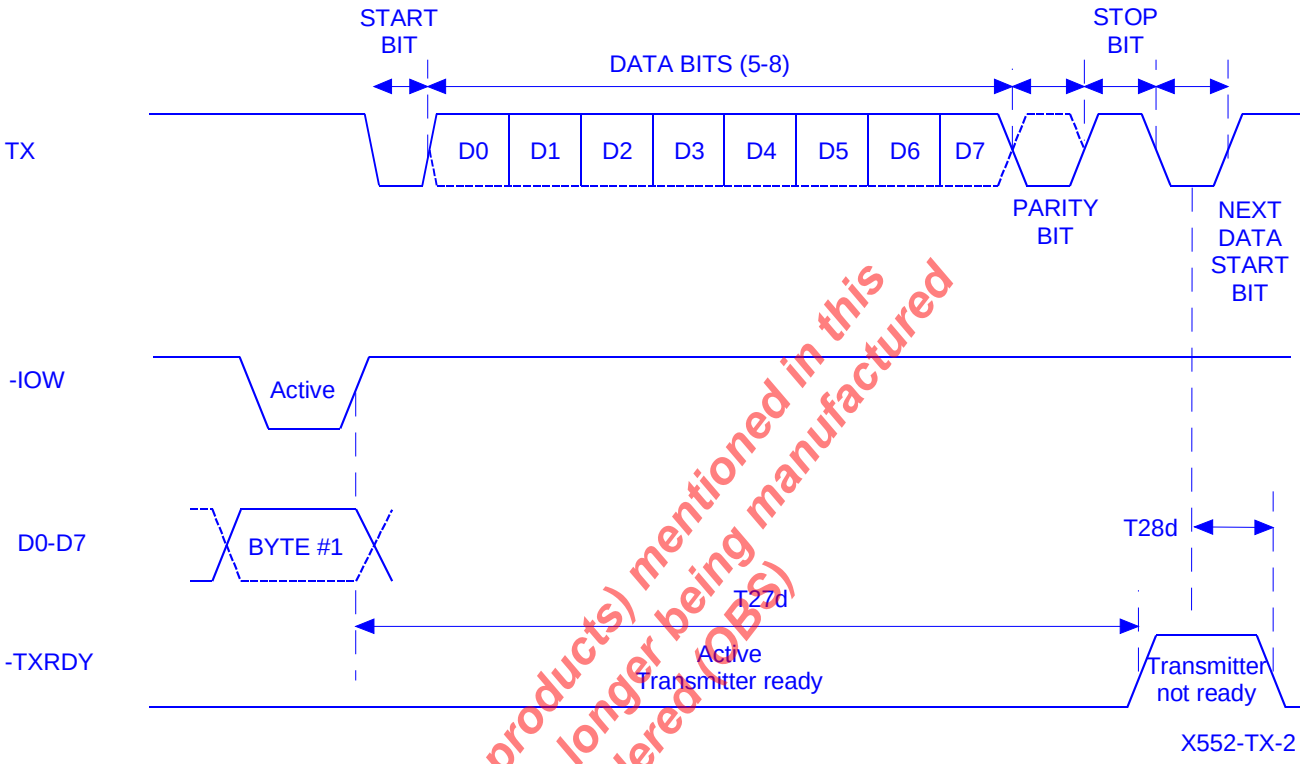
Receive timing in FIFO mode

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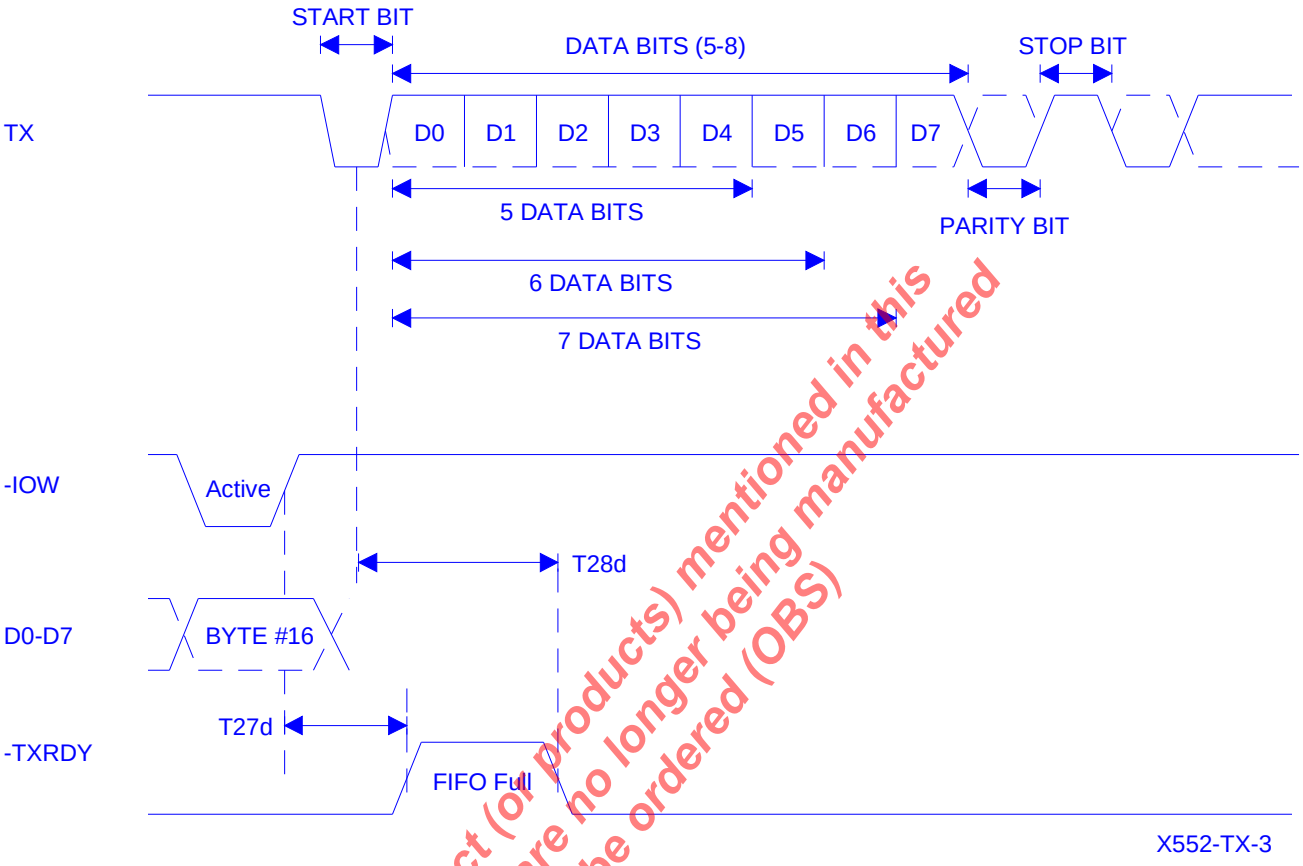
Transmit timing

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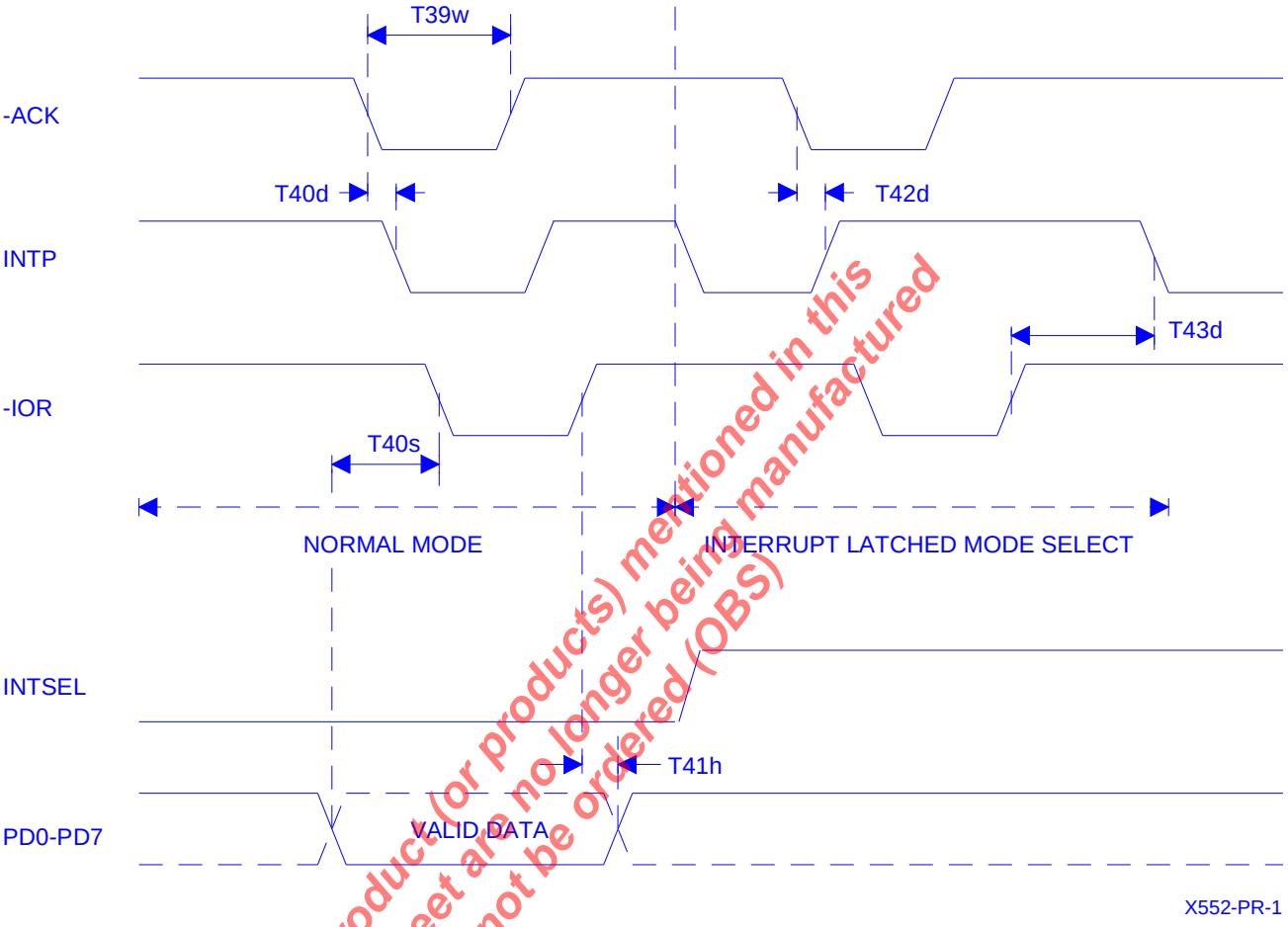
The product (or products) mentioned in this data sheet are no longer being manufactured and may not be ordered (OBS)

Transmit ready timing in none FIFO mode



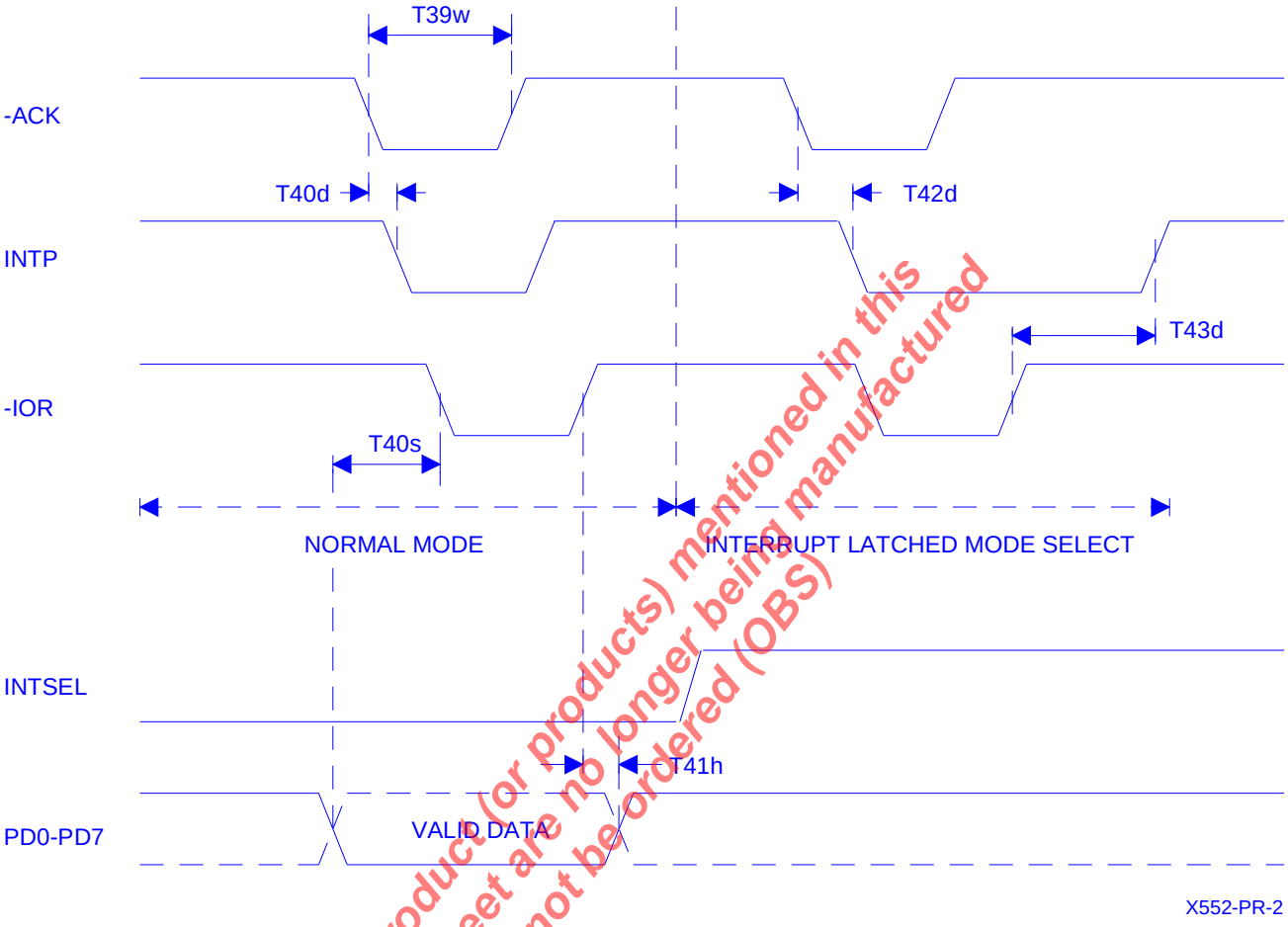
Transmit ready timing in FIFO mode

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Printer port timing (552 only)

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Printer port timing (552A only)

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EXPLANATION OF DATA SHEET REVISIONS:

FROM	TO	CHANGES	DATE
3.30	3.40	Added revision history. Added Device Status in Ordering Information. Device revisions of "F" and newer have 5V tolerant inputs except for XTAL1 and printer port inputs. Device revisions of "E" and older do not have 5V tolerant inputs.	Dec 2003

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