Design Solution # 41

Reducing Parasitic Oscillations at the Switching Node

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Part Numbers: SP6133/6, SP6134, SP6132

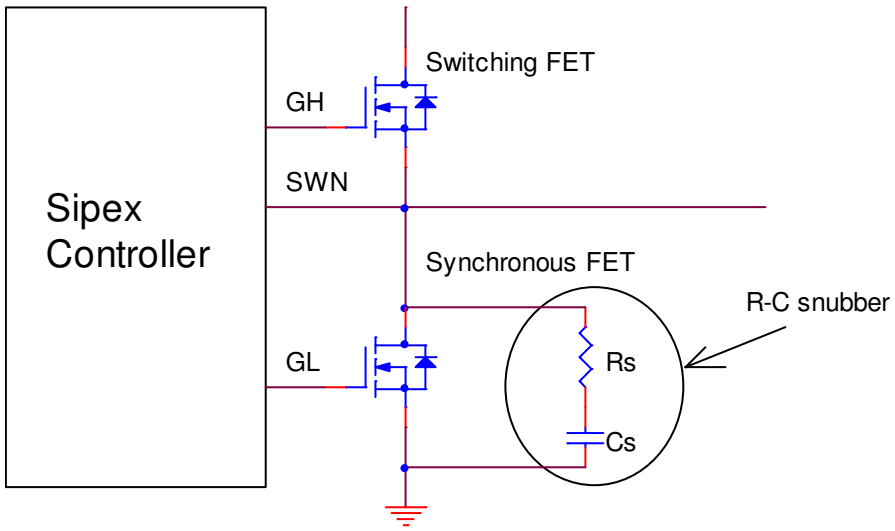
Application Description: Any noise-sensitive application where synchronous buck converters are used.

Electrical Requirements:

Input Voltage	5V – 24V
Output Current	higher than 10A

Circuit Description:
There usually exist high-frequency parasitic oscillations at the node between the switching FET and synchronous FET (SWN). It is not uncommon to see SWN peak voltage as high as 2.5xV_{IN}. The oscillations are a product of parasitic inductance in the DC-Loop of the Printed Circuit Board (PCB) and snappy reverse-recovery of synchronous FET's body diode. A dissipative R-C snubber across the synchronous FET dampens the oscillation quickly and reduces the peak voltage.

This report includes the application schematic and a procedure for determining the R-C snubber components Resistors and Capacitors.



Application Schematic

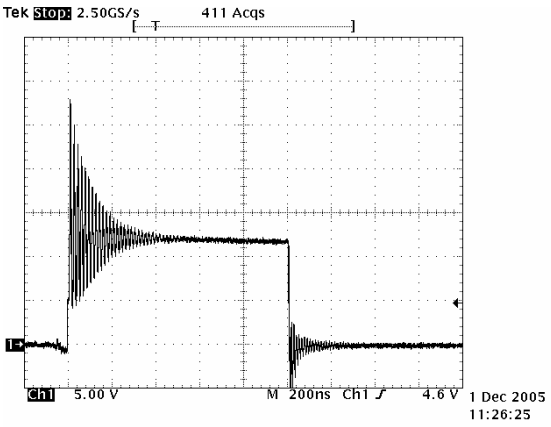


Figure 1: SWN without R-C snubber

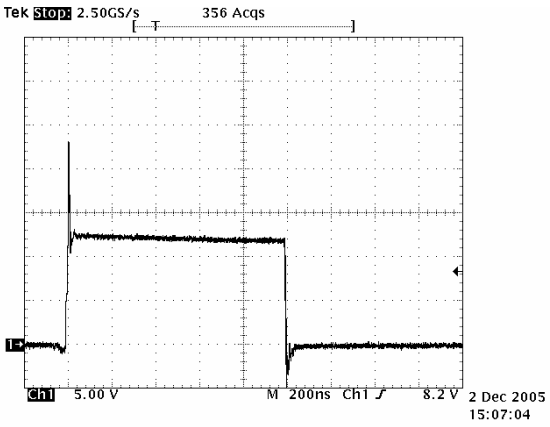


Figure 2: SWN with R-C snubber

Comments:

Oscillations at the switching node (SWN) are a product of parasitic inductance in the PCB's DC-Loop and snappy recovery of Synchronous FET's body diode. The parasitic inductance stores energy when the switching FET conducts. Following the recovery of the synchronous FET's body diode, this energy is transferred back and forth between the parasitic inductance and output capacitance of the synchronous FET (Coss). The oscillations stress the SWN node of the controller plus the synchronous FET and are a potential source of Electro Magnetic Interference.

Procedure for selecting snubber components

Let Cs = 4 x Coss

Where:

Cs is the snubber capacitor
Coss is the output capacitance of the synchronous FET. Determine the value corresponding to V_{IN} of the converter from the Coss graph in the FET datasheet.

As a rule of thumb use a 0.25W Resistor Rs in the 2 to 3Ω range. Place the snubber components as close to the FET as possible.