INTRODUCTION:

PowerArchitect™ is Exar's intuitive and easy-to-use software for developing power supplies with the XRP7724, XRP7720, XRP7725, XRP9711, and XRP9710 family programmable power management system. PowerArchitect™ empowers engineers to create complex sequencing schemes, modify voltage, current and many other parameters in seconds. This guide intends to quickly introduce you to this powerful tool and start designing.

DOWNLOADING & INSTALLATION:

1. PowerArchitect™ is provided on the supplied USB dongle for Power^{XR} kits. If you do not have the USB dongle, you can download the latest version of PowerArchitect™ from: http://powerxr.exar.com. You must provide your name and email address in order to download the software.

2. Once downloaded, double-click **PowerArchitect5.1-rX.exe** (the version as of this writing) to install the software. During the install you may get warning messages as the program installs. This is normal, just ignore the warnings. Please bear in mind that this is the install program and not the runtime program. It will put a link on your desktop that you use to run the software.

3. You should now be able to launch PowerArchitect™ 5.1.

STARTING POWERARCHITECT™

When you start up the program you will be brought to the welcome screen shown in Figure 1. The welcome screen asks you to choose a family, Devices or Modules.

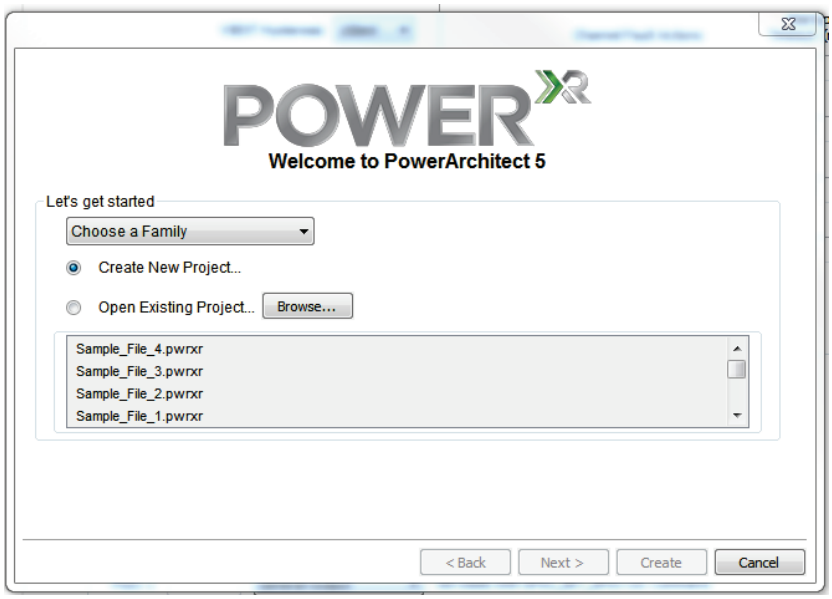


Figure 1: Welcome Screen

2. After you select a family, you are required to select the device that you want to use with PowerArchitect™.

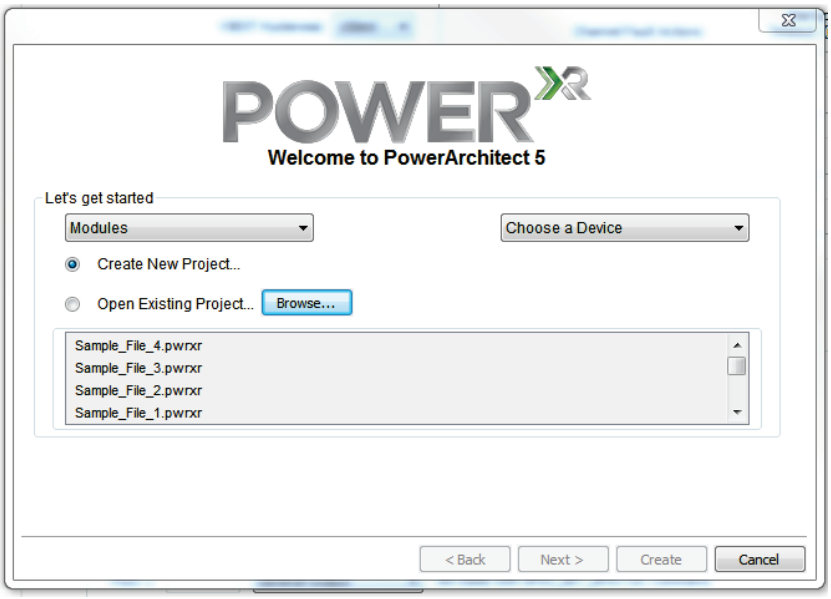


Figure 2: Welcome Screen after Family selection

3. After you select the device, there are three options to start PowerArchitect™.

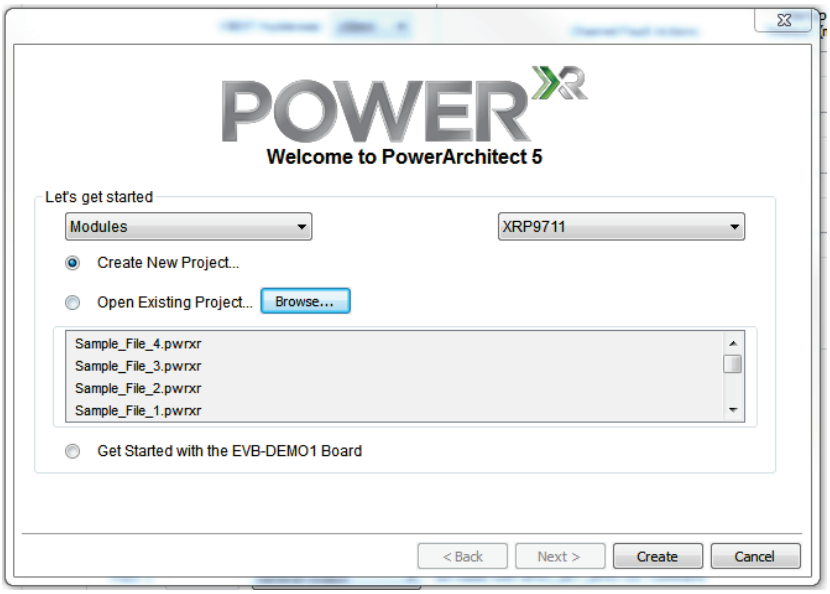


Figure 3: Welcome Screen after Device selection

1. **Create New Project**

   This will start the PowerArchitect™ Wizard walkthrough to configure a new project (Note that the default values used are not the same as the EVB-DEMO-1 Boards.)

2. **Open an Existing Project**

   This will open an already existing project that you can select from the list of recently opened files or browse to a particular file location to open that project.

3. **Get started with the EVB-DEMO1 Board**

   This will start PowerArchitect™ and load its default values based on the components on the demo board and bring you to the main design window.

GET STARTED WITH THE EVB-DEMO1 BOARD

Select the **Get started with the EVB-DEMO1 Board**. This will begin PowerArchitect™, load its default values based on the demo board, and bring you to the main design window shown in Figure 4. At this point you do not need the demo board connected to the computer.

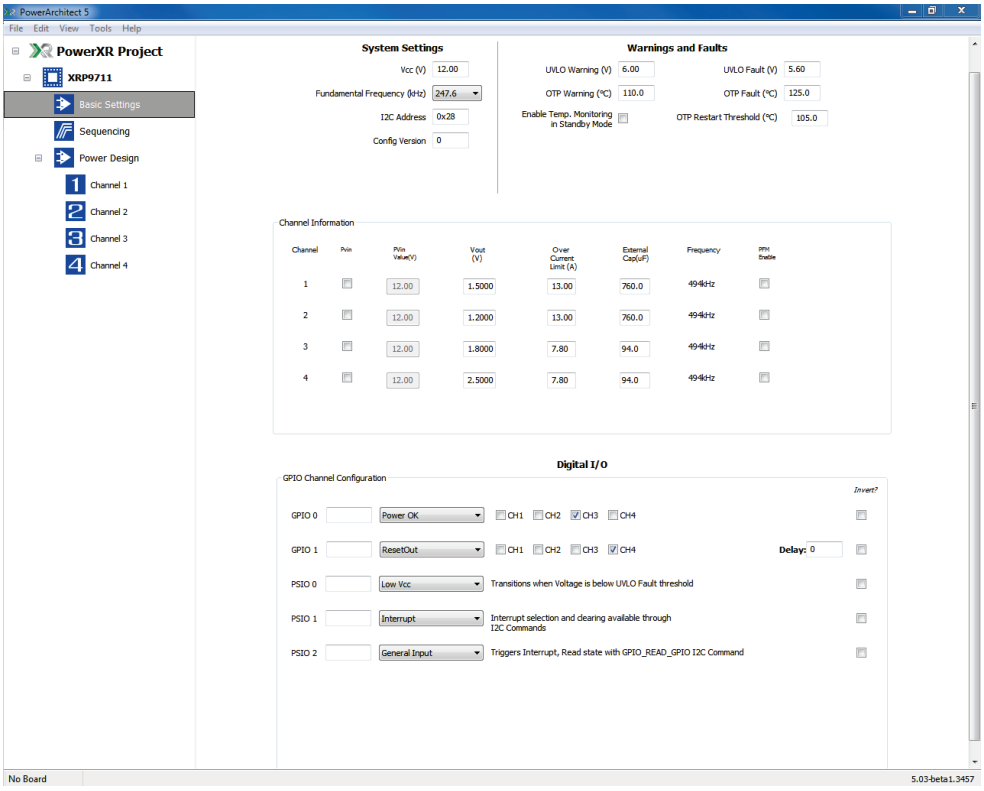


Figure 4: Main Design Screen

The main design window is comprised of two parts. The left side is a menu of the available design windows and the right side is the actual design window selected. There are 9 menu windows that you can select.

Menu Windows

1) PowerXR Project
2) Device Window (XRP9711 in this case)
3) Basic Settings
4) Sequencing
5) Power Design
6) Channel 1
7) Channel 2
8) Channel 3
9) Channel 4

POWERXR PROJECT WINDOW (FIGURE 5)

This contains general logistic information that you can enter about the project.

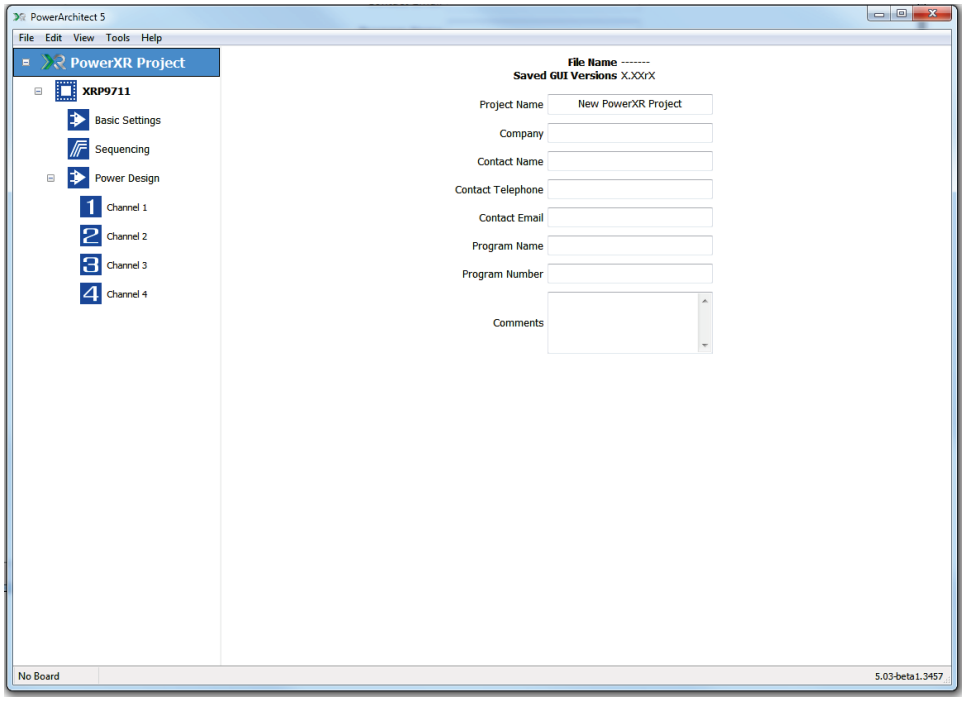


Figure 5: PowerXR Project Window

DEVICE WINDOW (FIGURE 6)

This window contains a summary of the project and design settings. The right side has a scroll bar to allow you to scroll down to see all the data. You can also right click on the right side and select "Print Preview" to see all the data at once and to send it to a printer.

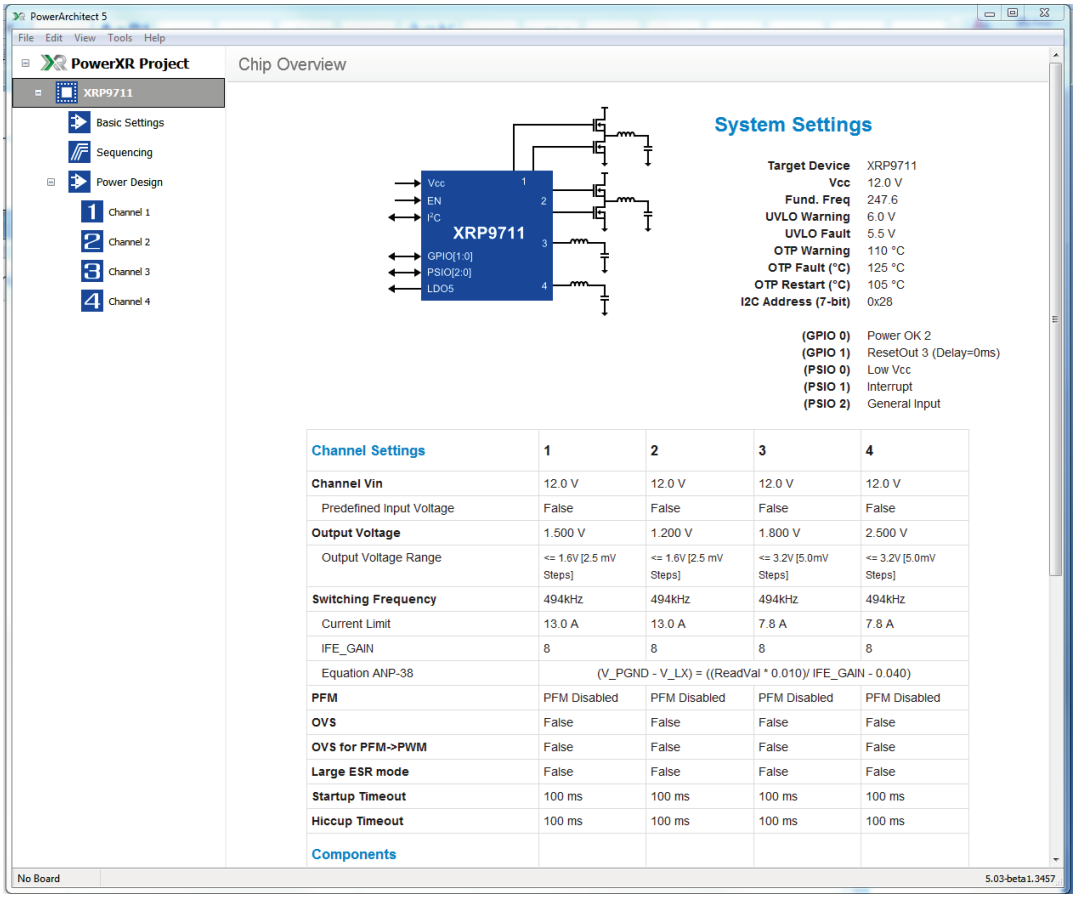


Figure 6: Device Window

BASIC SETTINGS WINDOW (FIGURE 7)

This is the window where you define the common functions of the design.

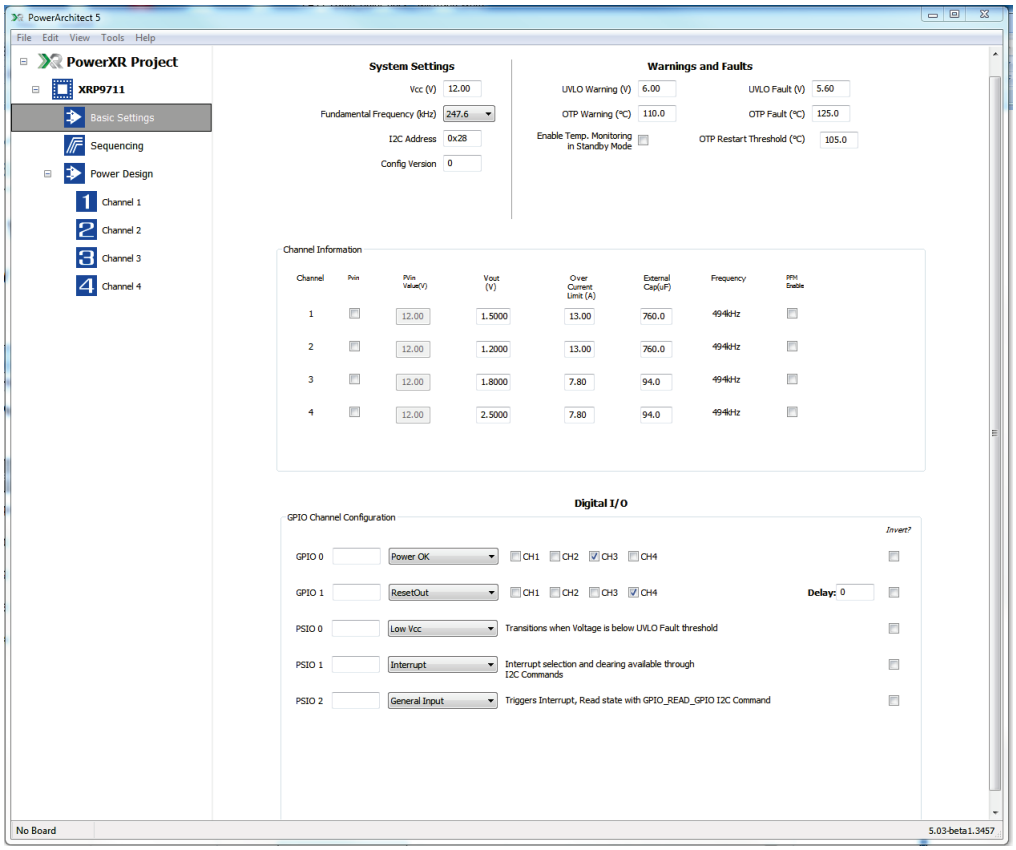
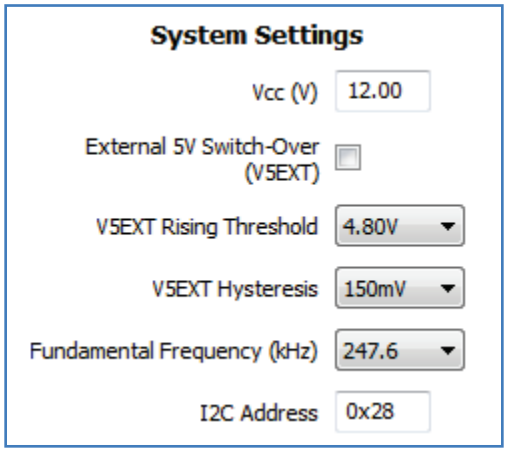


Figure 7: Basic Settings Window

a. System Settings Section:

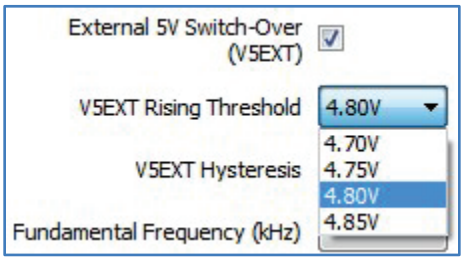


- **Vcc (V)**

  Enter the Vcc voltage that will be supplied to the XRP7724. When you click in the value, up/down arrows will appear to allow you to change the voltage in 0.1V steps.

- **V5EXT switchover control**

  If an external 5V supply will be connected to the V5EXT pin, check this box to enable this function. The switchover thresholds are programmable in 50mV steps from 4.70V to 4.85V. The hysteresis to switch the external power supply in-out is 150mV. The internal LDO5 LDO automatically turns off when the external voltage is switched in and turns on when the external voltage drops below the lower threshold.



  When the controller switches over to the V5EXT rail, the V5EXT_RISE interrupt is generated to inform the host. Similarly, when the controller switches out, the V5EXT_FALL interrupt gets generated.

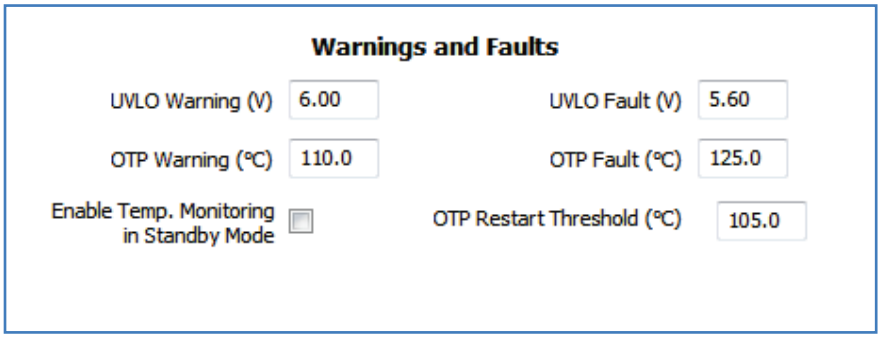
- **Fundamental Frequency (kHz):**

  This is a pull down menu where you select the available fundamental switching frequency for all the output channels.

- **I2C Address:**

  This is the I2C address for the device. When you click the box, up/down arrows will appear to allow you to change it. The default address is 0x28 (seven bit representation).

b. Warnings and Faults Section



UVLO Warning (V):

Select the Vcc level in 200mV increments where you want the device to issue a warning flag. If operating with a Vcc voltage of 5V enter 4.6V or 4.8V. After the UVLO fault, and when Vcc returns to a level above this threshold, the chip will reset.

UVLO Fault (V):

Select the Vcc level in 200mV increments where you want the device to issue a fault flag. If operating with a Vcc voltage of 5V enter 4.4V or 4.6V.

OTP Warning (°C):

Select the over temperature level, in 5°C increments, where you want the device to issue a warning flag.

OTP Fault (°C):

Select the over temperature level in 5°C increments, where you want the device to issue a fault flag.

OTP Restart Threshold (°C):

Enter the temperature that you want the device to restart after an OTP fault.

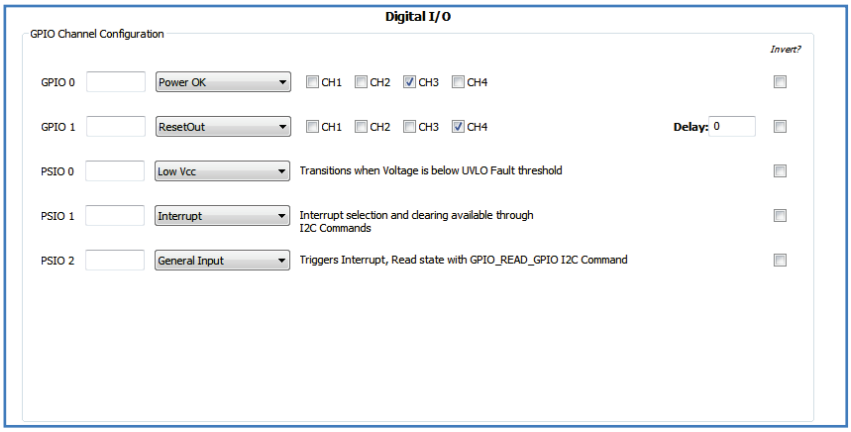
Enable Temp. Monitoring in Standby Mode:

Check this box if you need to monitor the device temperature when the chip is in standby mode. Selecting this option will significantly increase quiescent current.

c. Digital I/O Section

DIGITAL I/O

The chips and modules have two General Purpose Input Output (GPIO) and three Power System Input Output (PSIO) user configurable pins.



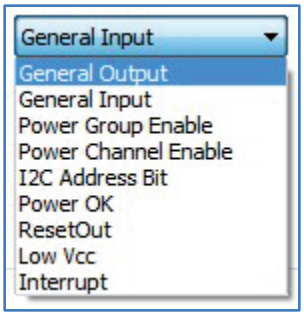
- GPIOs are 3.3V CMOS logic compatible and 5V tolerant.
- PSIOs when configured as outputs are open drain and require external pull-up resistors. These I/Os are 3.3V and 5V CMOS logic compatible, and up to 15V capable.

The polarity of the GPIO/PSIO pins can be set in PowerArchitect™ by clicking the "Invert" box or with an I^2C command.

The white text boxes next to the pin label are used to name the pin. This name is displayed next to the pin description in top right of the overview panel.

Configuring GPIO/PSIOs

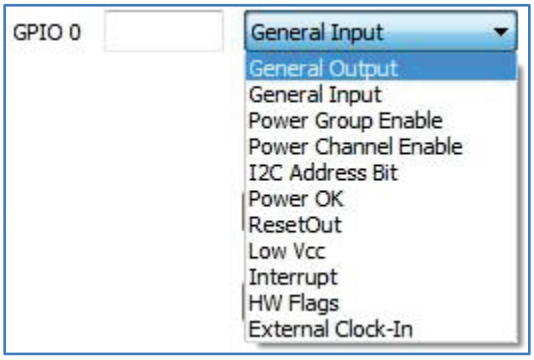
The following functions can be controlled from, or outputted to, any GPIO/PSIO:



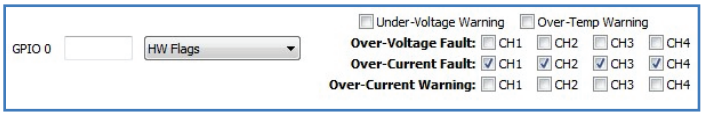
- **General Output** – set with an I^2C command
- **General Input** – triggers an interrupt; state read with an I^2C command
- **Power Group Enable** – controls enabling and disabling of Group 1 and/or Group 2
- **Power Channel Enable** – controls enabling and disabling of a individual channel or LDO3_3
- **I^2C Address Bit** – controls an I^2C address bit
- **Power OK** – indicates that selected channels have reached their target levels and have not faulted. Multiple channel selection is available in which case the resulting signal is the AND logic function of all channels selected
- **ResetOut** – is delayed Power OK. Delay is programmable in 1msec increments with the range of 0 to 255 milliseconds
- **Low Vcc** – indicates when Vcc has fallen below the UVLO fault threshold and when the UVLO condition clears (Vcc voltage rises above the UVLO warning level)
- **Interrupt** – the controller generated interrupt; masking and clearing is done through I^2C commands

Interrupt, Low Vcc, Power OK and ResetOut signals can only be forwarded to a single GPIO/PSIO.

Functions Unique to GPIO0.

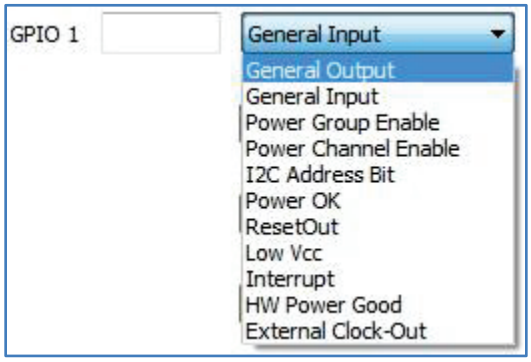


HW Flags – these are hardware monitoring functions forwarded to GPIO0 only. The functions include Under-Voltage Warning, Over-Temperature Warning, Over-Voltage Fault, Over-Current Fault and Over-Current Warning for every channel. Multiple selection is available in which case the resulting signal is the OR logic function



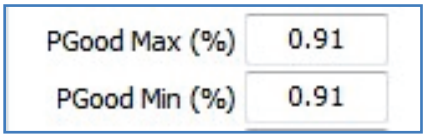
External Clock-in – enables the controller to lock to an external clock that is applied to the GPIO0 pin, including one from another XRP7724. There are two ranges of clock frequencies that the controller will accept; these are selectable by the user

Functions Unique to GPIO1.



HW Power Good – the Power Good hardware monitoring function. It can only be forwarded to GPIO1. It is an output voltage monitoring function that is a hardware comparison of channel output voltage against its user defined Power Good threshold limits (Power Good minimum and maximum levels). . It has no hysteresis. Multiple channel selection is available in which case the resulting signal is the AND logic function of all channels selected.

The Power Good minimum and maximum levels are expressed as percentages of the target voltage.



"PGood Max" is the upper window and "PGood Min" is the lower window. The minimum and maximum for each of these values can be calculated by the following equation:

$$PGOOD(\%) = \frac{N * LSB(mV) * 10^5}{Vtarget\ (V)}$$

Where N =1 to 63 for the PGOOD Max value and N=1 to 62 for the PGOOD Min value. For example, with the target voltage of 1.5V and set point resolution of 2.5mV (LSB), the Power Good min and max values can range from 0.17% to 10.3% and 0.17% to 10.5% respectively. A user can effectively double the values by changing to the next higher output voltage range setting, but at the expense of reduced set point resolution.

External Clock-out – clock sent out through GPIO1 for synchronizing with another XRP7724 (see the clock out section of the datasheet for more information).

Sequencing Window (Figure 8)

This is where you define the turn-on, turn-off and channel to channel relationships.

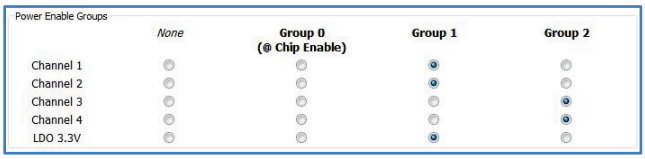
Figure 8: Sequencing Window

POWER SEQUENCING

All four channels and LDO3.3 can be grouped together and start-up and shut-down in a user defined sequence.

Selecting none means channel(s) will not be assigned to any group and will be controlled independently.

Group Selection



There are three groups:

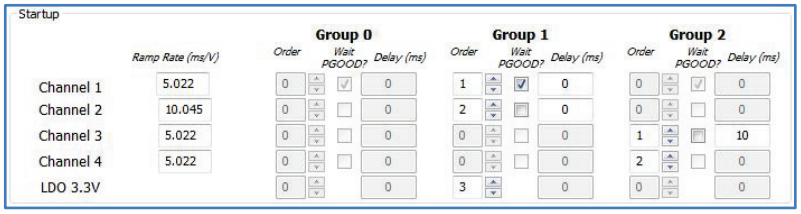
Group 0 – is controlled by the chip ENABLE or I^2C command. Channels assigned to this group will come up with the ENABLE signal being high (plus some additional delay needed to transfer configuration from flash to run time registers), and will go down with the ENABLE signal being low. The control can be overridden with an I^2C command.

Since it is recommended to leave the ENABLE pin floating in the applications when Vcc = LDO5 = 4.75V to 5.5V, please contact Exar for how to configure the channels to start up during power up in this scenario.

Group 1 – can be controlled by any GPIO/PSIO or I^2C command. Channels assigned to this group will start-up or shut-down following transitions of a signal applied to the GPIO/PSIO set to control the group. The control can always be overridden with an I^2C command.

Group 2 – can be controlled by any GPIO/PSIO or I^2C command. Channels assigned to this group will start-up or shut-down following transitions of a signal applied to the GPIO/PSIO set to control the group. The control can always be overridden with an I^2C command.

Start-up



For each channel within a group a user can specify the following start-up characteristics:

Ramp Rate – expressed in milliseconds per Volt. It does not apply to LDO3.3.

Order – order position of a channel to come-up within the group

Wait PGOOD? – selecting this option for a channel means the next channel in the order cannot start ramping-up until this channel reaches the target level and its Power Good flag gets asserted.

Delay – an additional time delay a user can specify to postpone a channel start-up with respect to the previous channel in the order. The delay is expressed in milliseconds with a range of 0ms to 255ms.

Shut-down

For each channel within a group a user can specify the following shut-down characteristics:

Ramp Rate – expressed in milliseconds per Volt. It does not apply to LDO3.3.

Order – order position of a channel to come-down within the group

Wait Stop Thresh? – selecting this option for a channel means the next channel in the order cannot start ramping-down until this channel reaches the Stop Threshold level. The stop threshold level is fixed at 600mV.

Delay – additional time delay a user can specify to postpone a channel shut-down with respect to the previous channel in the order. The delay is expressed in milliseconds with a range of 0msec to 255msec.

Power Design Window (Figure 9)

This is the window where the fault conditions are specified and the sample de-rating curves are shown.

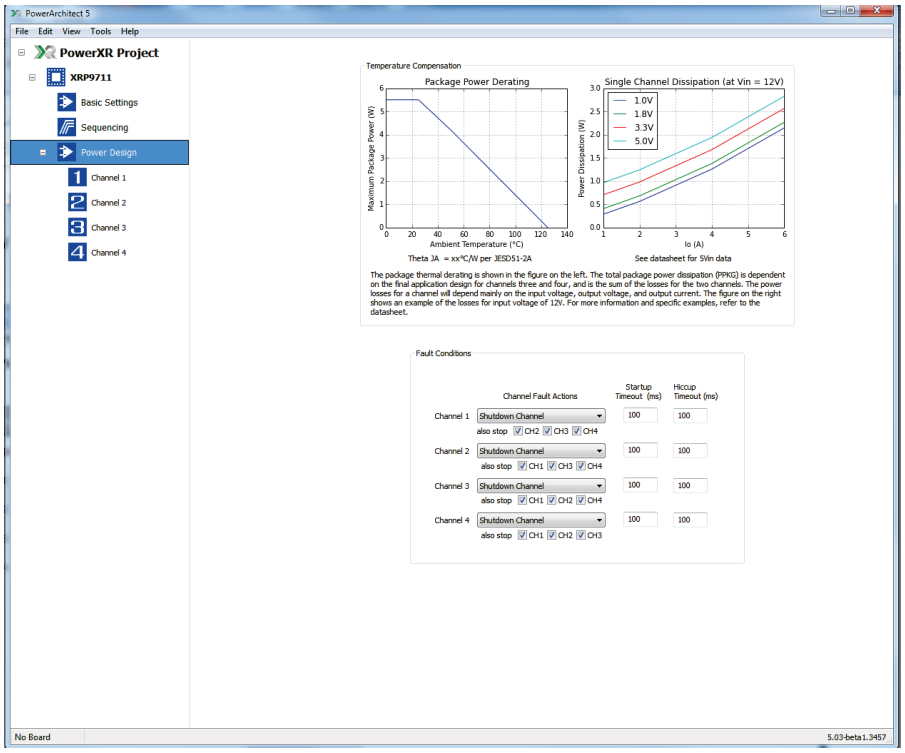
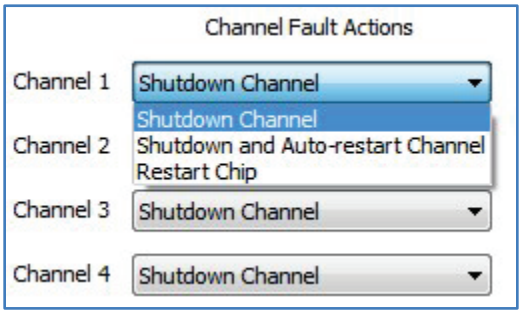


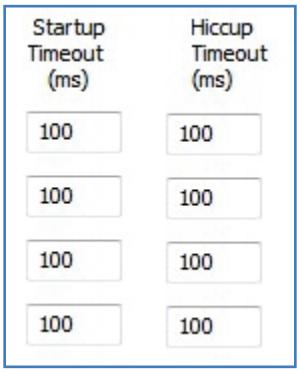
Figure 9: Power Design Window

Channel Fault Actions:

A user can choose one of three options on how to react to an OVP, OCP, or startup fault event: to shutdown the faulting channel, to shut down faulting channel and to perform auto-restart of the channel, or to restart the chip.



In the case of shutting down the faulting channel and auto-restarting, the user has an option to specify startup timeout (the time in which the fault is validated) and hiccup timeout (the period after which the controller will try to restart the channel) periods in 1 millisecond increments with a maximum value of 255 msec.



Channel 1 Design Window (Figure 10)

This is the window where the power supply output design is done for a channel.

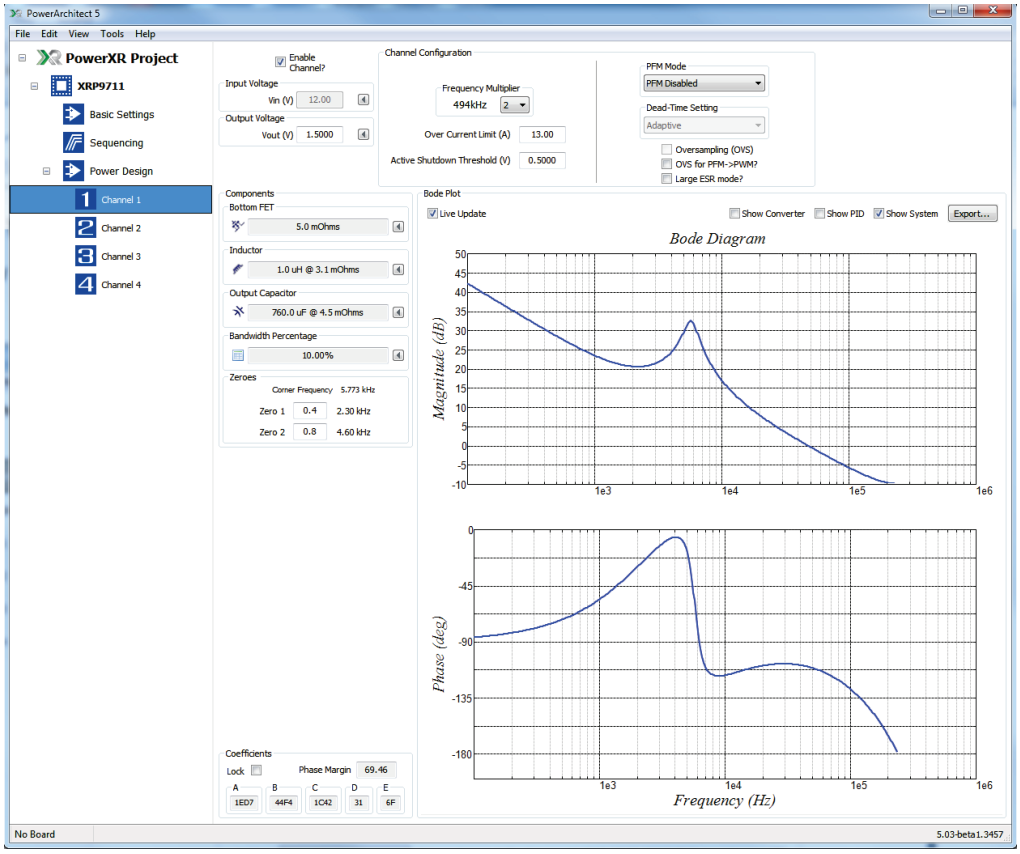


Figure 10: Channel 1 Window

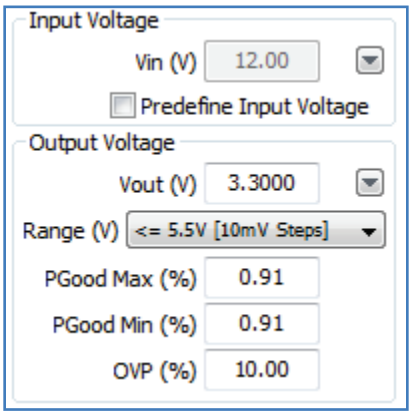
The top area of the window is where you specify the operating conditions for the channel and the bottom area is where you specify the output filter.

TOP SECTION:

The top section has Input and Output Voltage on the left and Channel Configuration on the right.

Input and Output Voltage

The input and output inputs have submenus as shown below.

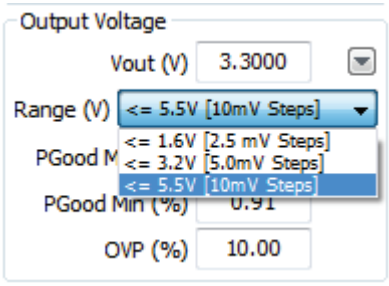


Input Voltage:

If the input voltage (Vin) for the channel is the same as the Vcc input check the "Predefine Input Voltage" box. This will enable the Vcc feed forward function. If the voltage for the channel is different than Vcc enter the channel voltage value.

Output Voltage:

The chips and modules have three selectable output voltage ranges with the lower ranges having better resolution. Select the correct range from the pull down menu for the required output voltage. Then enter the required output voltage in the Vout (V) box. PowerArchitect™ will then display the closest available voltage available based on the resolution of the selected range.



After the output voltage setting is complete enter the values for PGood Min(%) and Max(%) and OVP(%).

Channel Configuration Section:

Frequency Multiplier

Select the Frequency Multiplier for the channel from the pull down menu. This can be 1x, 2x, 4x the fundamental switching frequency that was entered in the General Design window.

Over Current Limit (A)

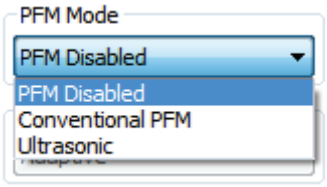
Enter the over current limit for the channel.

Active Shutdown Threshold (V)

This is the voltage that the output will be actively ramped down to based on the options chosen in the Power Sequence section.

PFM Mode

Select the PFM operating mode from the pull down menu.



Dead-Time Setting

This is where the options for the driver dead timings can be selected. In this release only Adaptive dead time operation is supported.

Oversampling (OVS)

Check this box to enable the oversampling feature. Oversampling is only available if the channel is operating in 1x frequency mode.

OVS for PFM->PWM

Check this box to enable the oversampling feature for PFM to PWM transitions. Again, oversampling is only available if the channel is operating in 1x frequency mode.

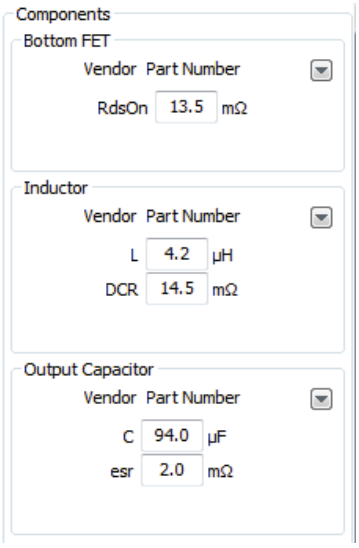
Large ESR Mode

The ESR of the output capacitors can effect certain PID calculations. If the output capacitors have higher ESR (typically non ceramic types) then this box should be checked.

BOTTOM SECTION:

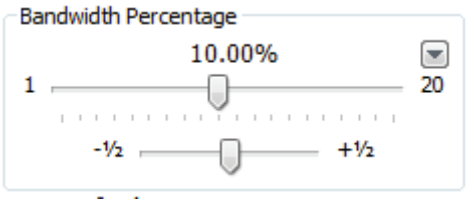
The Bottom section is broken down into two parts. The left side is where the design of the output filter is done and the right side shows the Bode plot for the design. **Left Side:**

Component Values:



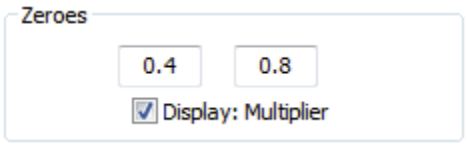
The bottom FET, inductor, and output capacitor design values for are entered here. For convenience a part number for the component can also be entered.

Bandwidth Percentage:



The loop crossover frequency, as a percentage of the switching frequency, is displayed. It has a course (1% steps) and a fine selector. Slide the bars to the crossover that you want.

Zeros (kHz)

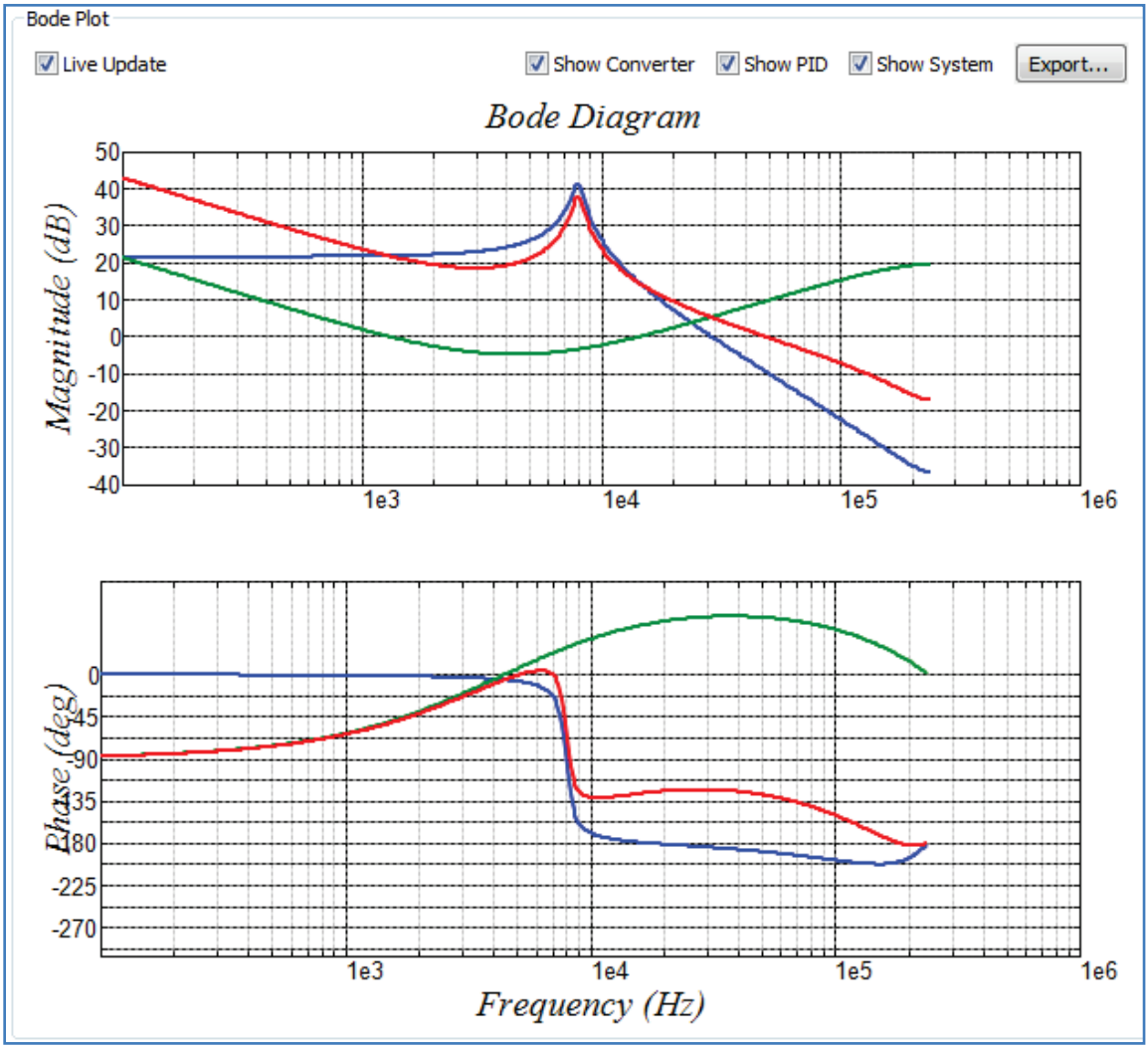


This displays the zero frequencies that the design tool calculates for the design. You can change the display from frequency to a multiplier of the double pole frequency by checking the "Display" box. You can override the calculated zero values by entering new values in the boxes.

Coefficients:

This area shows the calculated coefficients for the PID and the resultant loop phase margin. Checking the "Lock" box will lock the coefficients at the values shown. This allows you to vary various design parameters to evaluate the design under different operating conditions.

Right Side- Bode Diagram:



The Bode diagram on the right allows you to evaluate the design. In addition to the System plots you can also display the plots of the PID and Converter by checking the appropriate boxes. The export button allows you to export the plot data to a CSV file. Be aware that this can be a slow process and take a lot of time.

Channels 2 through 4 Windows

The design windows for all the output channels are structured the same. Although only Channel 1 is discussed in detail in this document, the information is applicable to all the other channels.

SETTING UP THE DEMO BOARD

The XRP7724 Evaluation Board is shown below. Refer to the board's Quick Start Guide document (XRPAQSG-XRP7724_0212) included in the kit and the XRP77XX Configuration Module document (XRP77XXEVB-XCM) for more detailed information on the board.

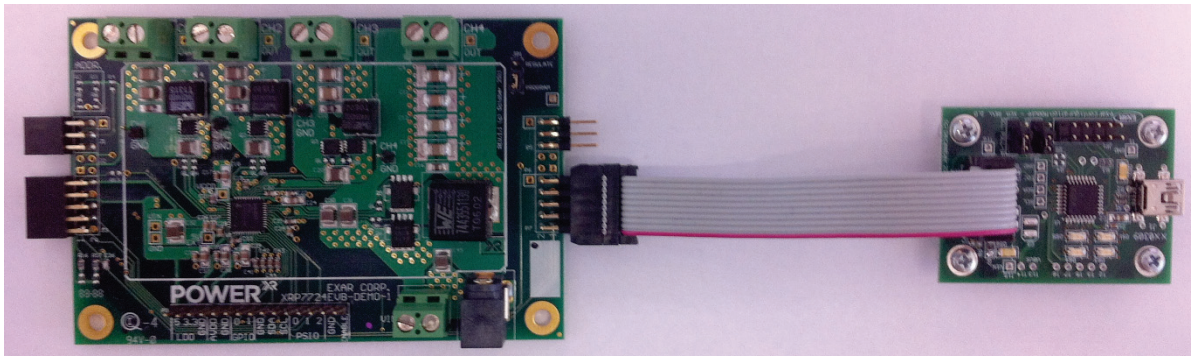
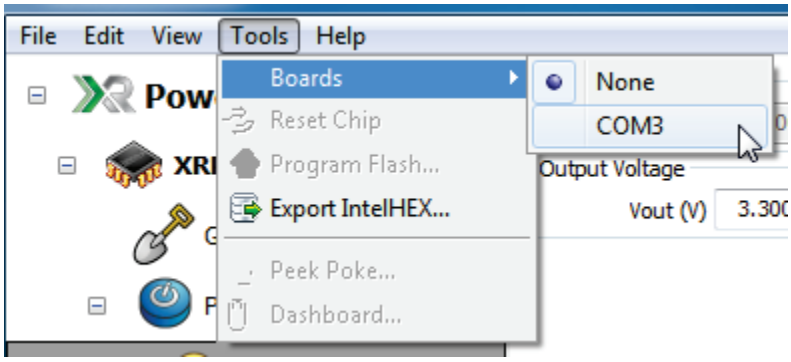


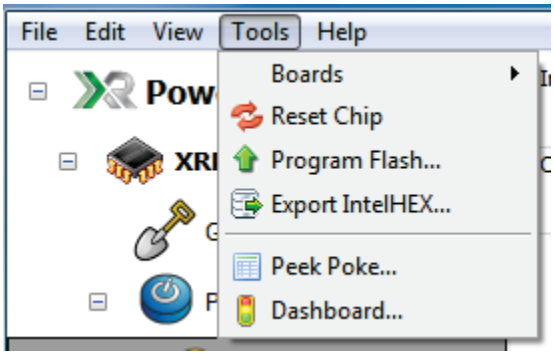
Figure 11: XRP7724EVB-DEMO-1 Evaluation Board

Connect a USB cable from your computer to the small board on the right and apply power to the board. In the upper left of the PowerArchitect™ window select the "Tools" button then "Boards" from the pull down menu and click on "COM3" (COM ports will vary).

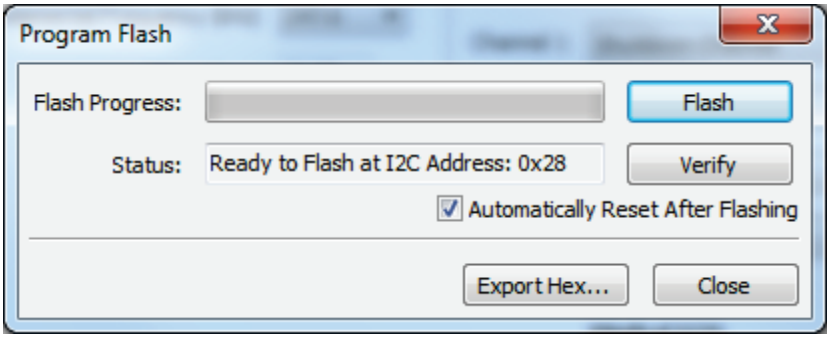


In the bottom left corner of the window the message will change from "No Board" to "XCM on COM3". You are now communicating with the demo board.

Reselect the Tools button and you will see a number of new options listed.



Select "Program Flash" option to open the program flash window.



Click on the "Flash" button and the Power Architect design will be written into the non volatile memory of the chip or the module on the demo board. Once the flash process is completed click on the close button. The board is now ready to run.

Please remember that whenever you change anything in the project you need to reflash the chip or the module for the changes to take effect.

RUNNING THE BOARD

To operate the board, select the "Dashboard" option from the tools menu which will open the Dashboard menu shown in figure 12.

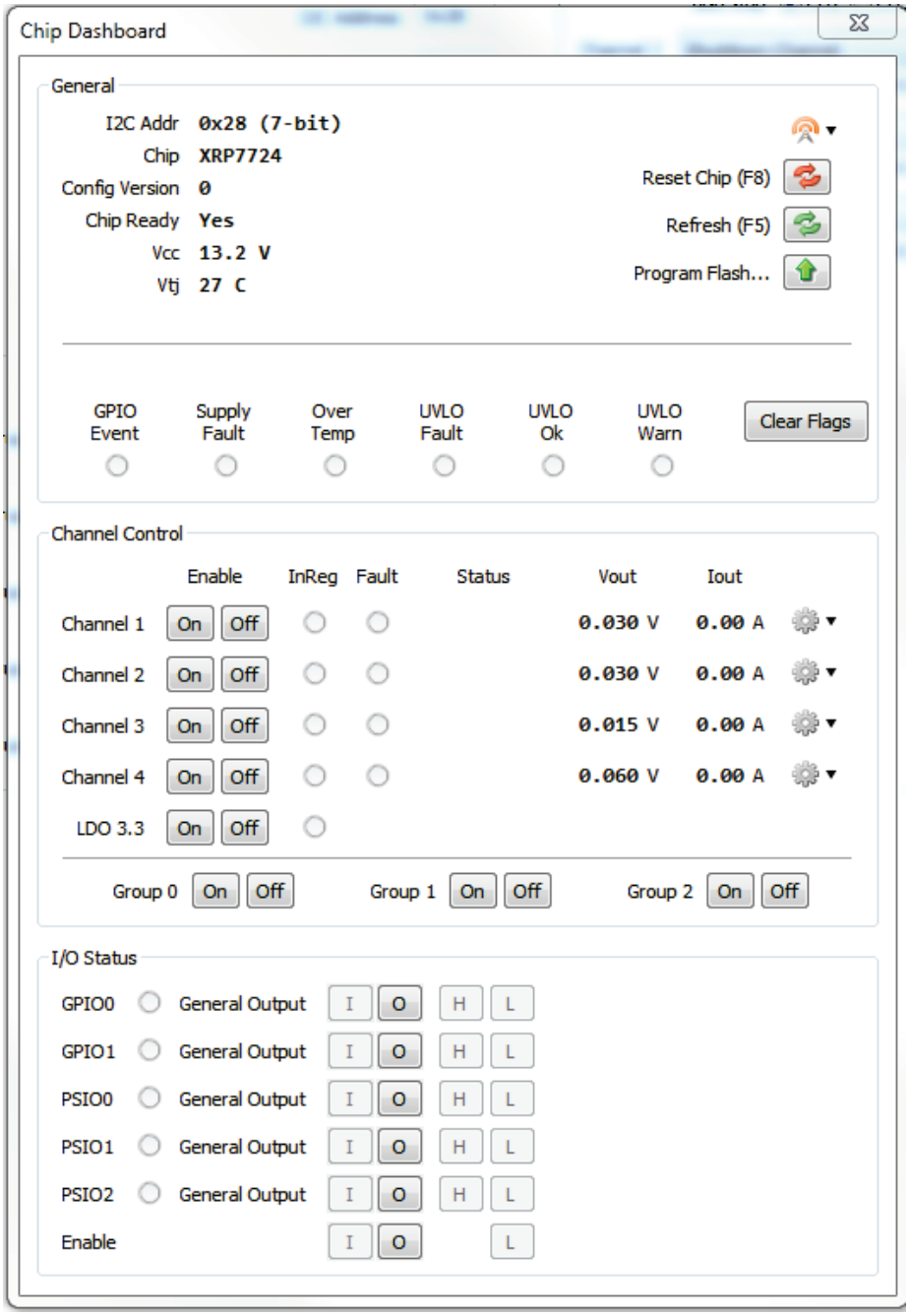
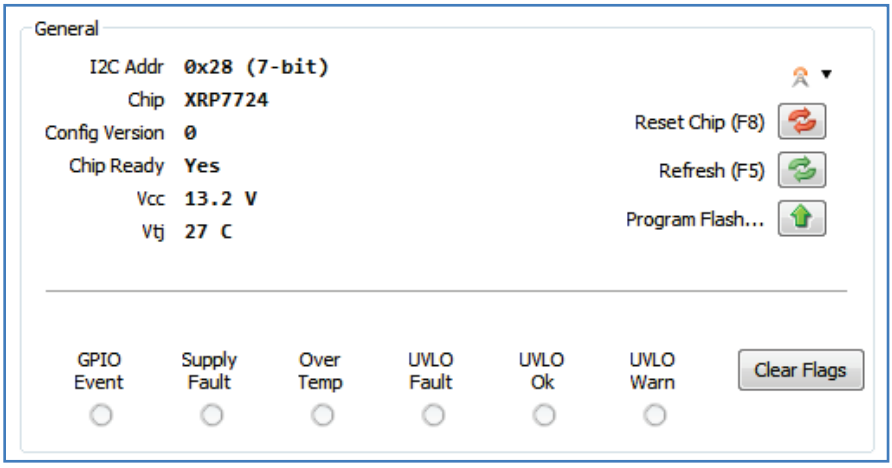


Figure 12: Dashboard Screen

The dashboard gives you real time control of the device on the demo board. Please note that any changes made through the dashboard are not programmed into flash memory and will not be saved as part of the as part of the project.

General Section:

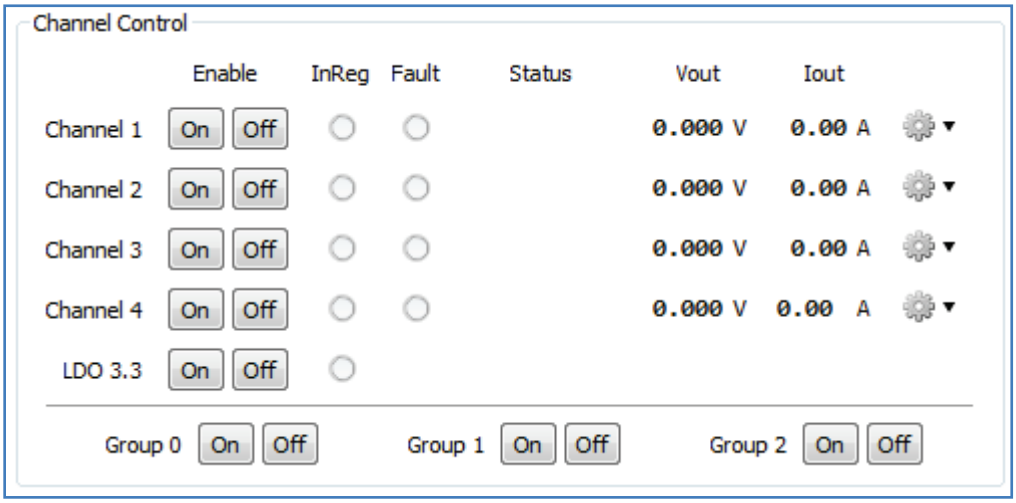


This section gives you general information about the device. The top left side shows the I^2C Address, Chip part number, Chip Ready status, Vcc input voltage and the die temperature.

The top right side gives you a pull down menu to set the chip communication options. The Reset Chip (F8) button resets the chip. Clicking on the Refresh (F5) button will immediately refresh the Dashboard information.

The bottom part of the general section contains indicators that show the condition of various system fault and warning flags.

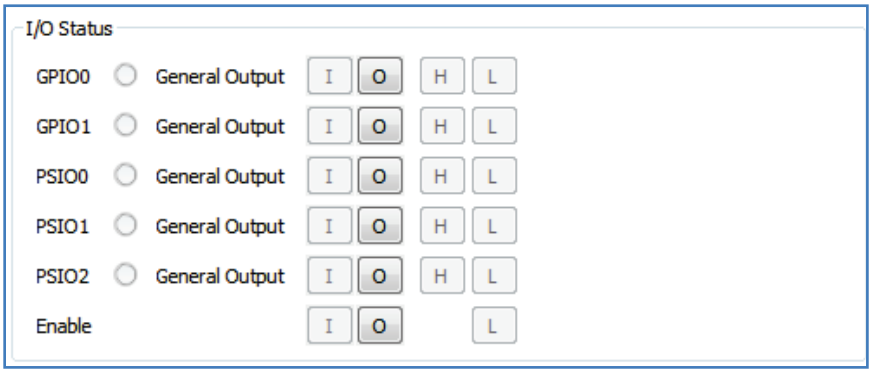
Channel Control Section:



The channel control section allows you to control the four output channels and the LDO 3.3 supply. You can turn the supplies on and off individually or in groups (if they have been assigned to groups in the "Power Sequence" design window). To the right of the on/off enable buttons are two columns of indicators. The first column shows if the output is in regulation and the second column indicates if a fault occurred. The output voltages (Vout) and output currents (Iout) for the channel are shown in the columns to the right.

The icon in the column to the far right is a pull down menu to allow you to increase or decrease the output voltage for the channel. (Please note that the output voltage can only be increased to the maximum allowed by the "Range (V)" you selected on the "Channel" design window.)

I/O Status Section:



This section has indicators that show the status of the GPIO and PSIO pins plus the function that the pin has been configured for.

SAVING YOUR WORK:

The "File" menu in the far upper left of the window gives you the option to save your project and to open new projects. Please remember that if you modify or start a new project you need to flash the project to the chip or the module for it to take effect.

DOCUMENT REVISION HISTORY

Revision	Date	Description
1.0.0	10/08/2012	Initial release of document
1.1.0	12/19/2013	Document updated for 5.1-rXX release

FOR FURTHER ASSISTANCE

Email: powertechsupport@exar.com

customersupport@exar.com

Exar Technical Documentation: http://www.exar.com/TechDoc/default.aspx?

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EXAR CORPORATION

HEADQUARTERS AND SALES OFFICES

48720 Kato Road

Fremont, CA 94538 – USA

Tel.: +1 (510) 668-7000

Fax: +1 (510) 668-7030

www.exar.com

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