ENVISIONING • EMPOWERING • EXCELLING

Quad MxL7213 100A Multiphase

EVK User Manual

Revision History

Document No.	Release Date	Change Description
018UMR00	11/21/19	Initial Release

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Introduction

The Quad MxL7213 100A Multiphase Evaluation Board provides a platform to evaluate the features and performance of four MxL7213 Power Modules connected in parallel to supply up to a 100A load. Each MxL7213 is a dual 13A Power Module which are optimized for powering Telecom, Networking and Industrial equipment. This manual covers both the BGA and LGA evaluation boards versions of this 100A multiphase application.

Quick EVK Set Up and Start Up

Factory Settings

In addition to utilizing the 4.5V to 16V input voltage range of the MxL7213's and the 100A maximum load current rating capabilities of using the four MxL7213 Power Modules together, the evaluation board has been set up with the factory default configurations shown below for quick set up and operation. **Do not exceed the EVK maximum load current rating.**

The factory default configuration (Table 2) for the MxL7213 Evaluation Board is:

- V_{IN} = 4.5V to 16V
- V_{OUT} = 1.0V ±1.5%. For other V_{OUT} see Jumpers JP4 - JP8 VOUT SELECT.
- I_{OUT} = 0A to 100A
- 500kHz switching frequency
- Run is enabled for both channels of all 4 of the MxL7213's (all 8 channels). See RUN, Jumper JP2.
- Continuous current mode using internal clock. To use an external clock, see EXT_CLK, Jumper JP1
- One pin output voltage ramp up and down tracking programmability
- A 6.5ms soft-start is selected for all channels
- Sensing diode biasing at 100µA for internal temperature sense

Quick Start Up

To quickly see the regulator in operation:

1. Use the factory settings and default configuration. If other settings or components are desired, apply them before the next steps and see Set-Up Options for more.
2. With a power supply turned off and within a V_{IN} specification of 4.5V to 16V (12V typical), connect it to VIN and GND with short, thick leads. Use test pins VIN+ and VIN- to monitor VIN and GND respectively. See locations in Figure 1.
3. For the output, connect a meter and electronic load initially set to 0A, that will be no more than the above maximum I_{OUT} (100A), to VOUT and GND with short / thick leads capable of this current. See setup and locations in Figure 1.
4. Turn on the power supply and check V_{OUT}. Check to make sure that JP2 is on the ON position. The EVK will power up and (factory default) regulate the output at 1V ±1.5% (0.985V to 1.015V).
5. Set or vary the load (do not exceed the maximum I_{OUT}) and check V_{OUT} and other desired performance levels such as regulation and efficiency.

See Configuration and I/O Interfaces and Load Transient Circuit for more on testing and monitoring.

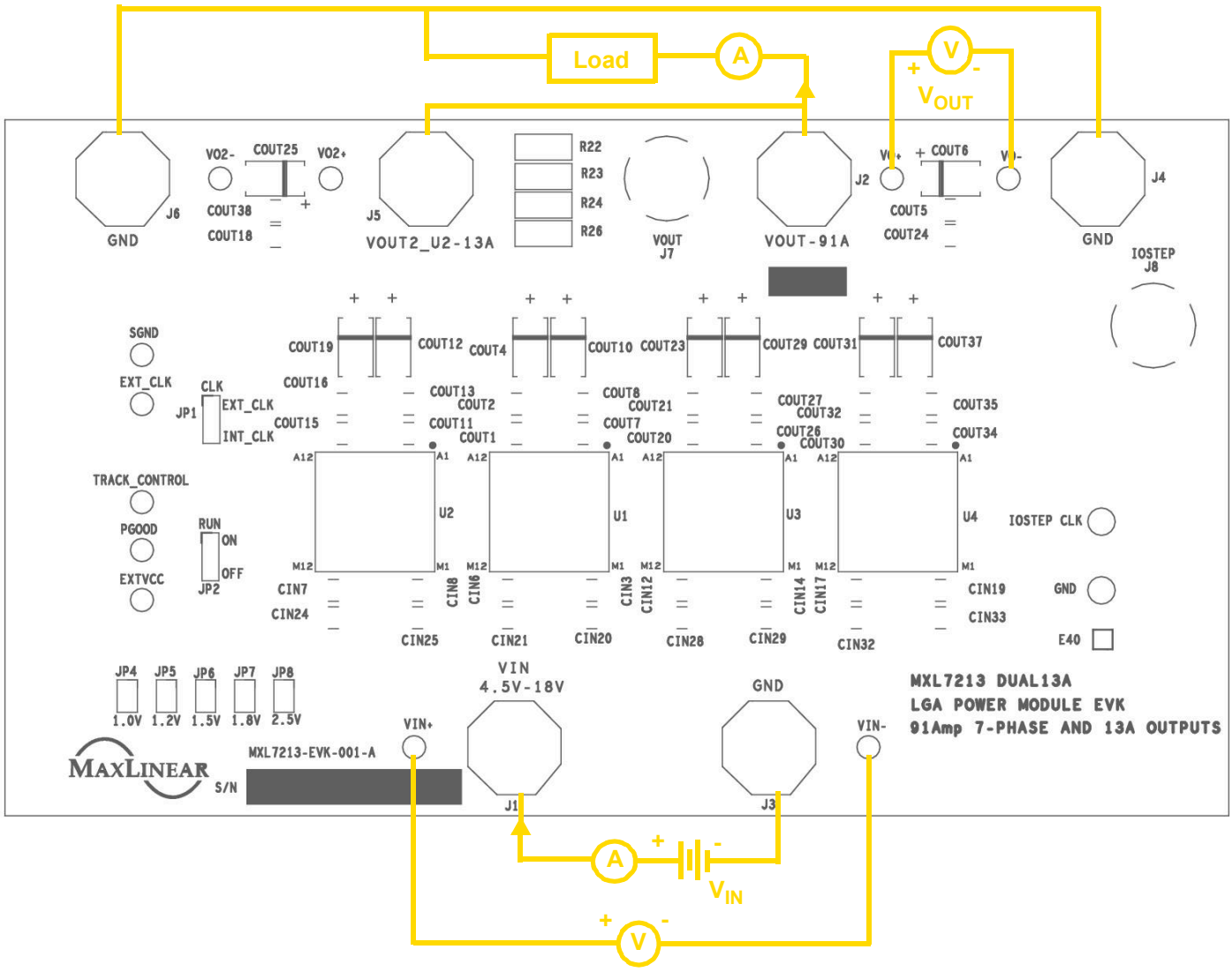


Figure 1: Monitoring V_{IN} and V_{OUT}

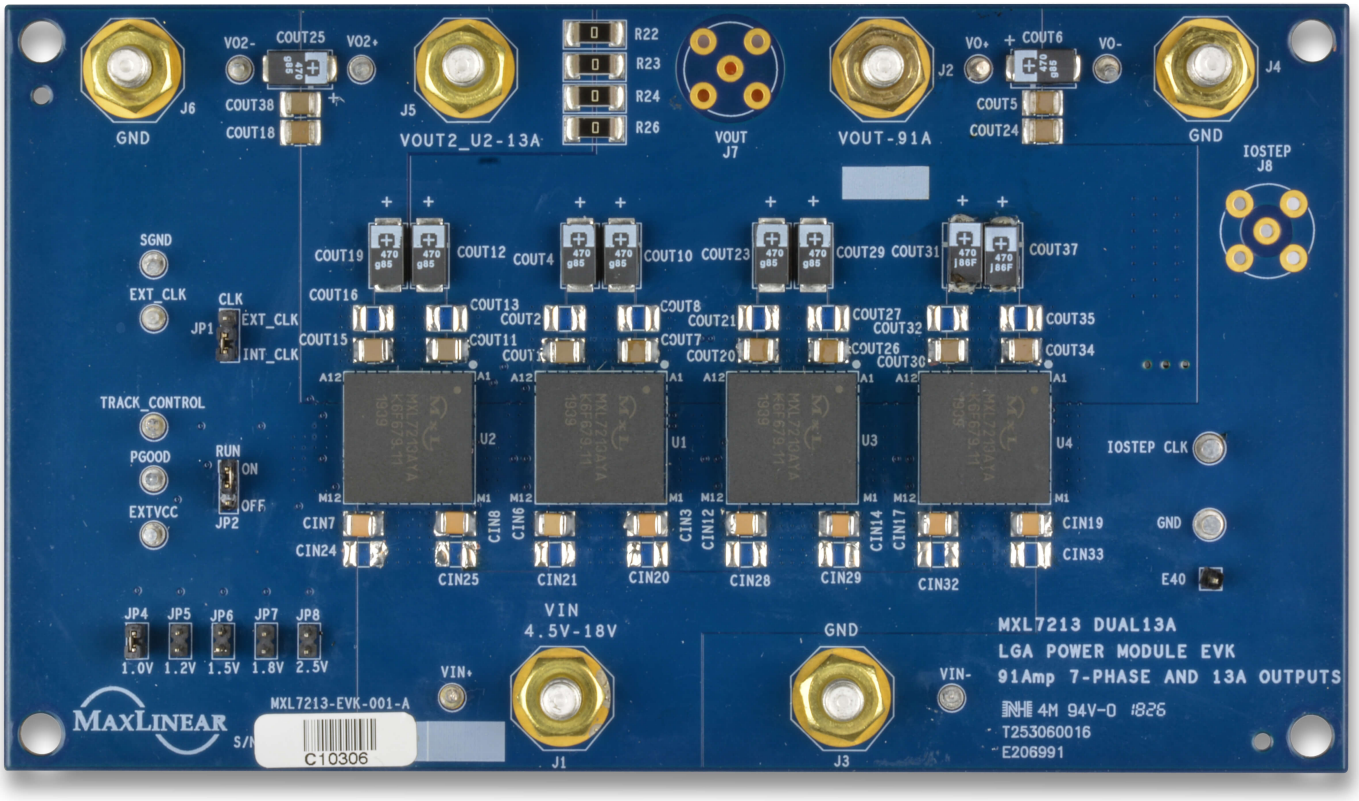


Figure 2: Top View of MxL7213 100A Multiphase EVK

Reference Documentation

Please refer to the MxL7213 Data Sheet for additional information about the MxL7213. The datasheet includes a full list of IC features, pinout, pin descriptions, typical performance characteristics and external component calculations. This manual is meant to be used in conjunction with the datasheet.

This manual provides MxL7213EVK Schematic, MxL7213EVK PCB Layers and MxL7213EVK Bill of Materials that can be utilized to assist in your board design. The schematics are also available on the MxL7213 product page.

Ordering Information

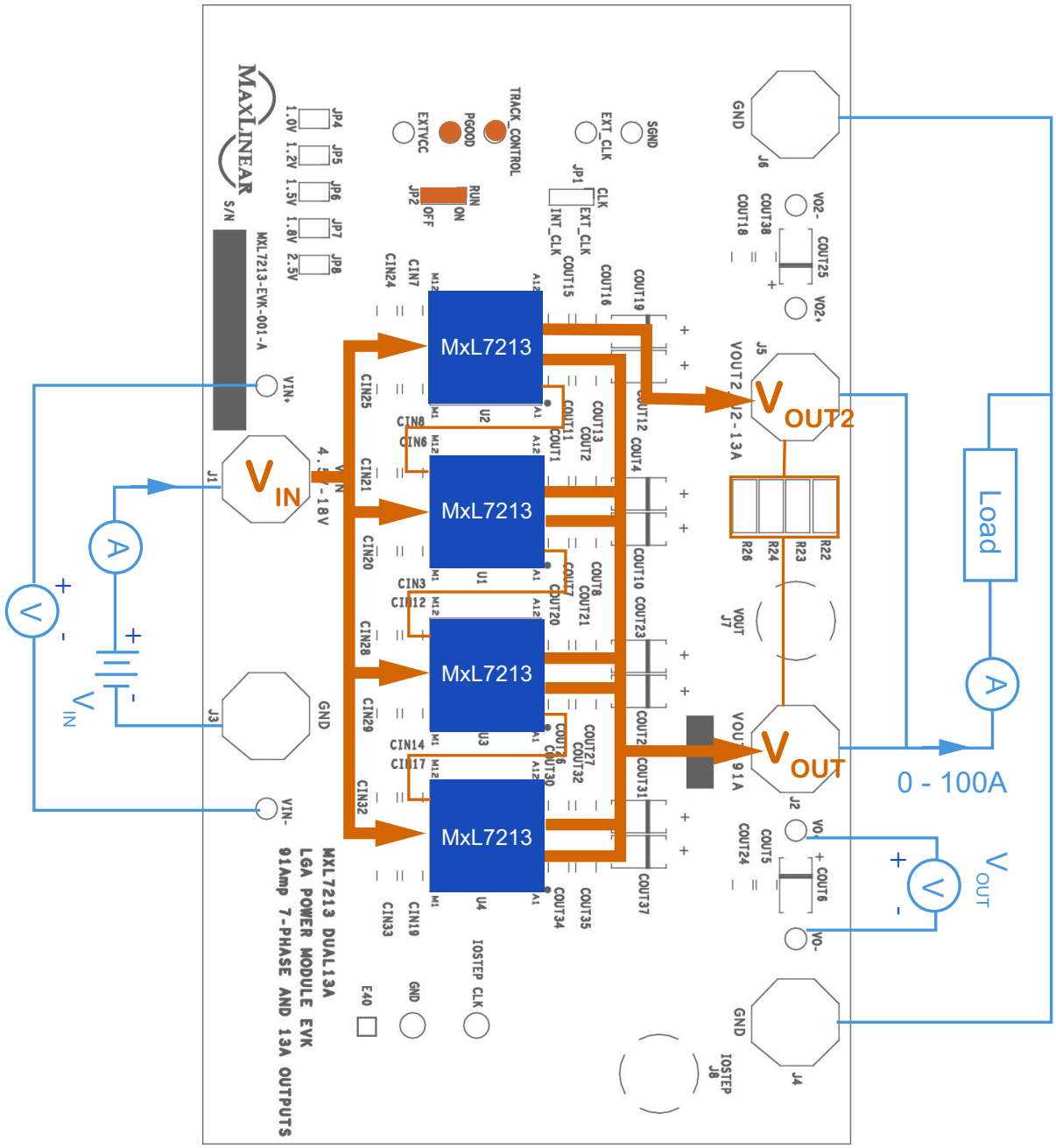
Table 1: Evaluation Board Ordering Part Number(1)

Power Module	Evaluation Board	Description
MxL7213-AYA-T	MxL7213-EVK-2	Quad MxL7213 LGA Power Module Multiphase EVK
MxL7213-ABA-T	MxL7213-EVK-4	Quad MxL7213 BGA Power Module Multiphase EVK

1. Refer to www.maxlinear.com/MxL7213 for most up-to-date Ordering Information.

Evaluation Board Overview

The block diagram shown in Figure 3 illustrates the 7 MxL7213 channels connected in parallel with the 8th channel as the master and the connection points for V_{IN}, V_{OUT}, and V_{OUT2}. Also represented are the CLKOUT to MODE_PLLIN connections between the 4 MXL7213 ICs.



V_{OUT} and V_{OUT2} connected via R22, R23, R24 and R26

VFB of all 8 channels connected

RUN of all 8 channels connected and connected to JP2

TRACK of all 8 channels connected and connected to TRACK_CONTROL point on board

PGOOD of all 8 channels (with pullups) connected and connected to PGOOD point on board

Figure 3: Quad MxL7213 100A Multiphase EVK Block Diagram

Configuration and I/O Interfaces

EXT_CLK, Jumper JP1

Jumper J1 provides an option to connect and synchronize to an external clock or use an internal clock (default). See EXT_CLK, Jumper JP1.

RUN, Jumper JP2

Jumper JP2 enables (ON) or disables (OFF) all 8 channels. See RUN, Jumper JP2.

TRACK_CONTROL

The board's output voltage tracks the voltage on the TRACK_CONTROL test point when applied.

PGOOD

A PGOOD test point is provided for all 8 channels. PGOOD signals are tied to INTVCC through 10kΩ resistors.

EXTVCC

A connection point is provided to inject EXTVCC, if desired.

IOSTEP CLK

Used to test load transients. See Load Transient Circuit.

Set-Up Options

Jumpers are factory installed per Table 2 to configure the EVK for operation. Jumper and testing options are described in the next sections. Refer to the product datasheet for additional information.

Table 2: Factory Settings

Jumper	Label	Factory Setting	Description
JP1	CLK	Jumper 2-3	Internal clock
JP2	RUN	Jumper 1-2	On
VOUT SELECT			
JP4	1.0V	Jumper 1-2	V_{OUT} = 1.0V selected
JP5	1.2V	No Jumper	
JP6	1.5V	No Jumper	
JP7	1.8V	No Jumper	
JP8	2.5V	No Jumper	

Jumper JP1 CLK

Table 3: JP1 Options

Jumper Options	Description
Jumper 1-2	External clock may be applied to synchronize to.
Jumper 2-3 (default)	Internal clock.

Jumper JP2 RUN

Table 4: JP2 Options

Jumper Options	Description
Jumper 1-2 (default)	On, all channels are enabled.
Jumper 2-3	Off, all channels are disabled.

Jumpers JP4 - JP8 VOUT SELECT

Table 5: JP4 - JP8 Options

Jumper	Jumper Options	Description
JP4	Jumper 1-2 (default)	V_{OUT} = 1.0V selected only.
	No jumper	V_{OUT} = 1.0V not selected.
JP5	Jumper 1-2	V_{OUT} = 1.2V selected only.
	No jumper (default)	V_{OUT} = 1.2V not selected.
JP6	Jumper 1-2	V_{OUT} = 1.5V selected only.
	No jumper (default)	V_{OUT} = 1.5V not selected.
JP7	Jumper 1-2	V_{OUT} = 1.8V selected only.
	No jumper (default)	V_{OUT} = 1.8V not selected.
JP8	Jumper 1-2	V_{OUT} = 2.5V selected only.
	No jumper (default)	V_{OUT} = 2.5V not selected.

Test Interfaces

Load Transient Circuit

A load transient circuit is provided to allow optional testing of load transients. The IOSTEP clock input is used to drive the transient signal. The load step generated by the FET (Q1) is very fast; the step slew rate is >40A/µs for a 6.5A transient load test case.

To measure load transient response, use the circuit shown in Figure 4. Populate R56 and R57 and apply a small duty cycle pulse signal to the IOSTEP CLK input (~ 1%). Adjust the amplitude of the IOSTEP CLK pulse to set the load current. Start at a pulse amplitude of 2V and increase while monitoring the IOSTEP (J8) voltage. The load current at IOSTEP CLK (E19) is 5mV/A. For an example, a 100A load will occur when a 500mV pulse is observed at E19.

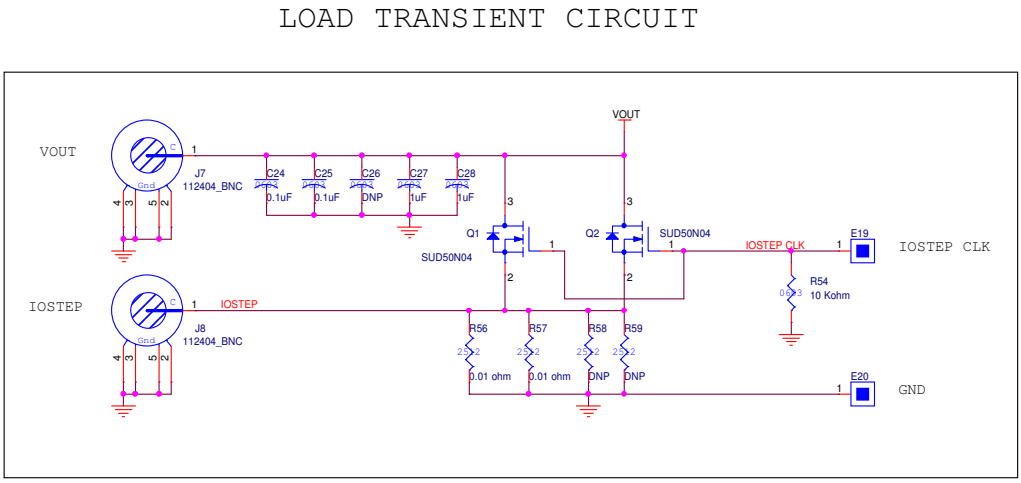


Figure 4: Load Transient Circuit

Performance

Efficiency

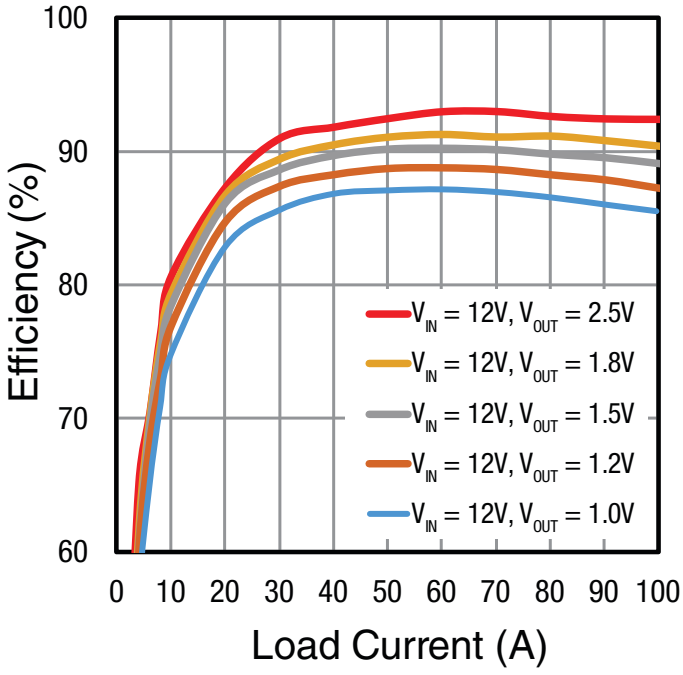


Figure 5: Measured Efficiency (V_{IN} = 12V, f_{SW} = 500kHz)

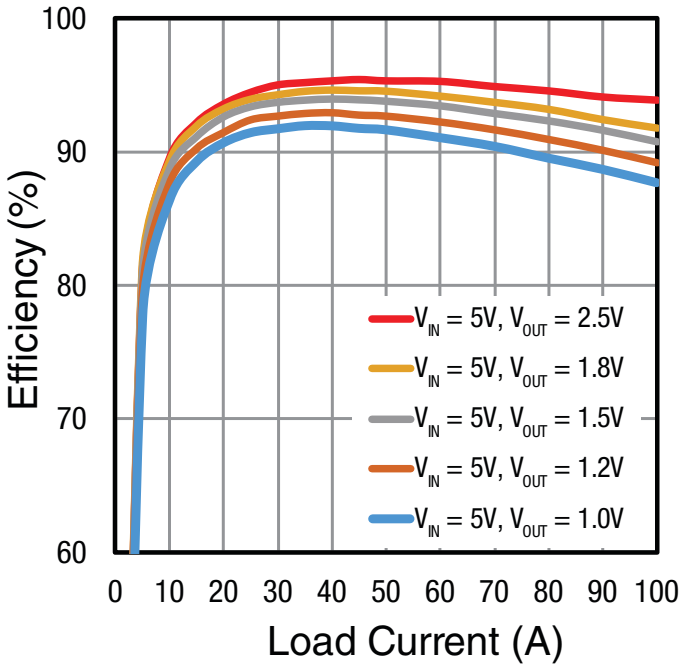


Figure 6: Measured Efficiency (V_{IN} = 5V, f_{SW} = 500kHz)

Load Transient Response

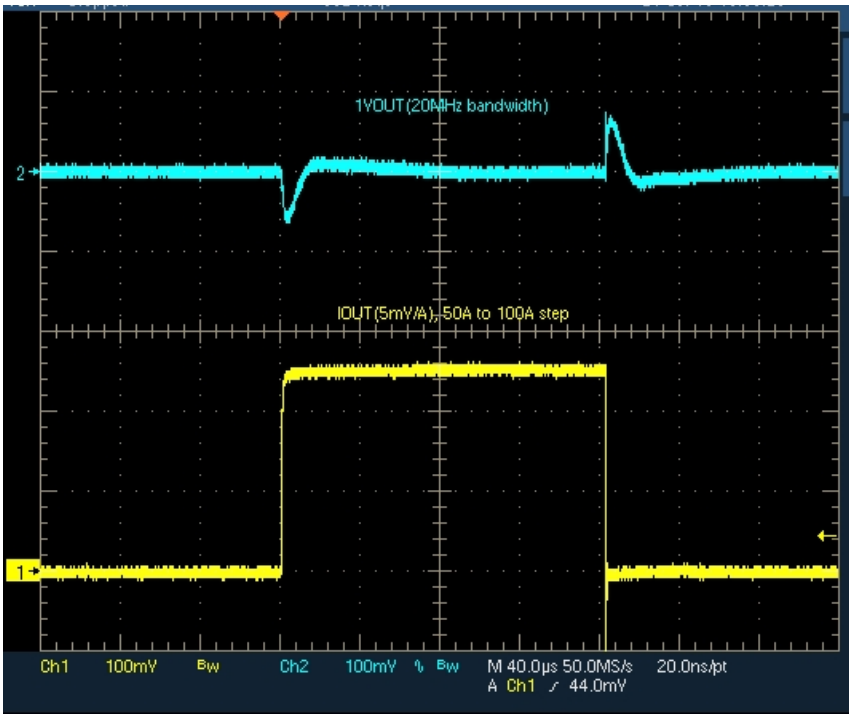
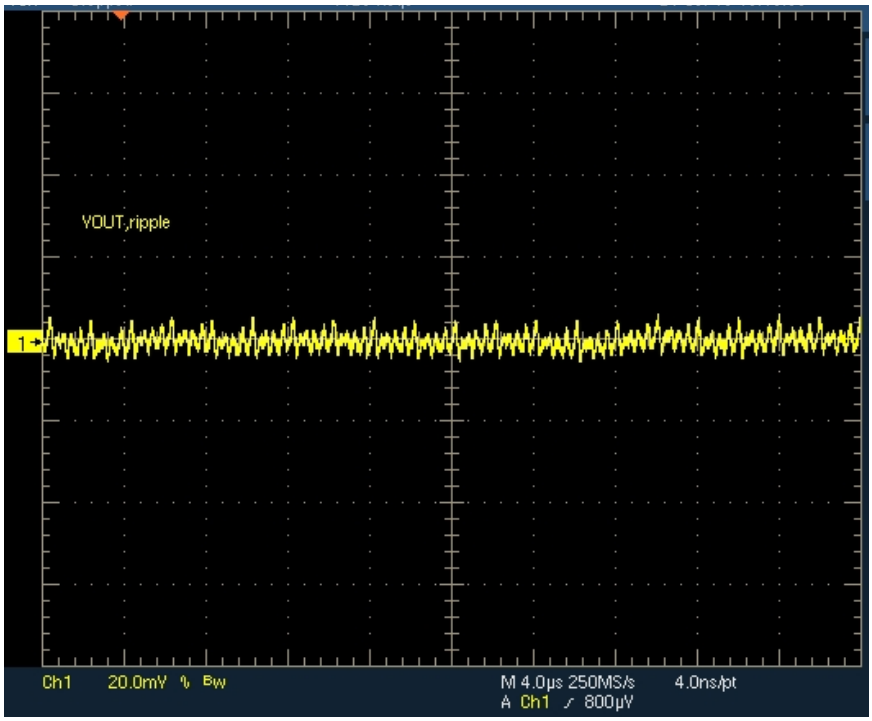


Figure 7: Load Transient Response, 50A to 100A (V_{IN} = 12V, V_{OUT} = 1V)

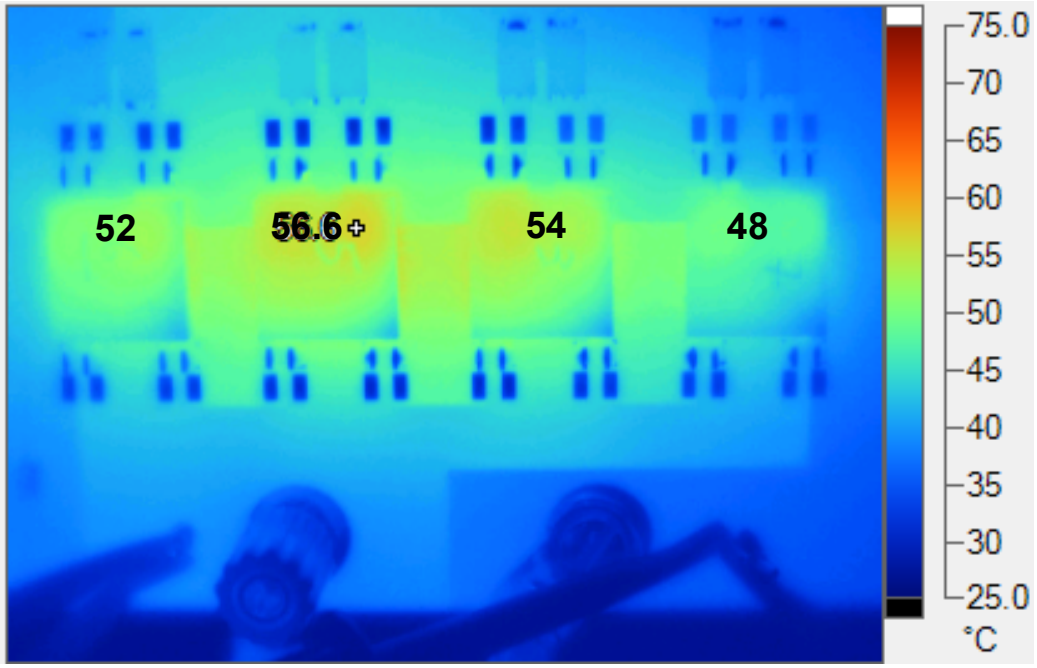
Output Ripple



2. 100A load on J7 with standard demo circuit default setup.

Figure 8: Measured Output Voltage Ripple (V_{IN} = 12V, V_{OUT} = 1V, Load = 100A)

Thermal



3. Ambient temperature = 23.3°C, airflow = 200LFM, no heat sink.

Figure 9: Thermal Capture (V_{IN} = 12V, V_{OUT} = 1V, Load = 100A)

MxL7213EVK Schematic

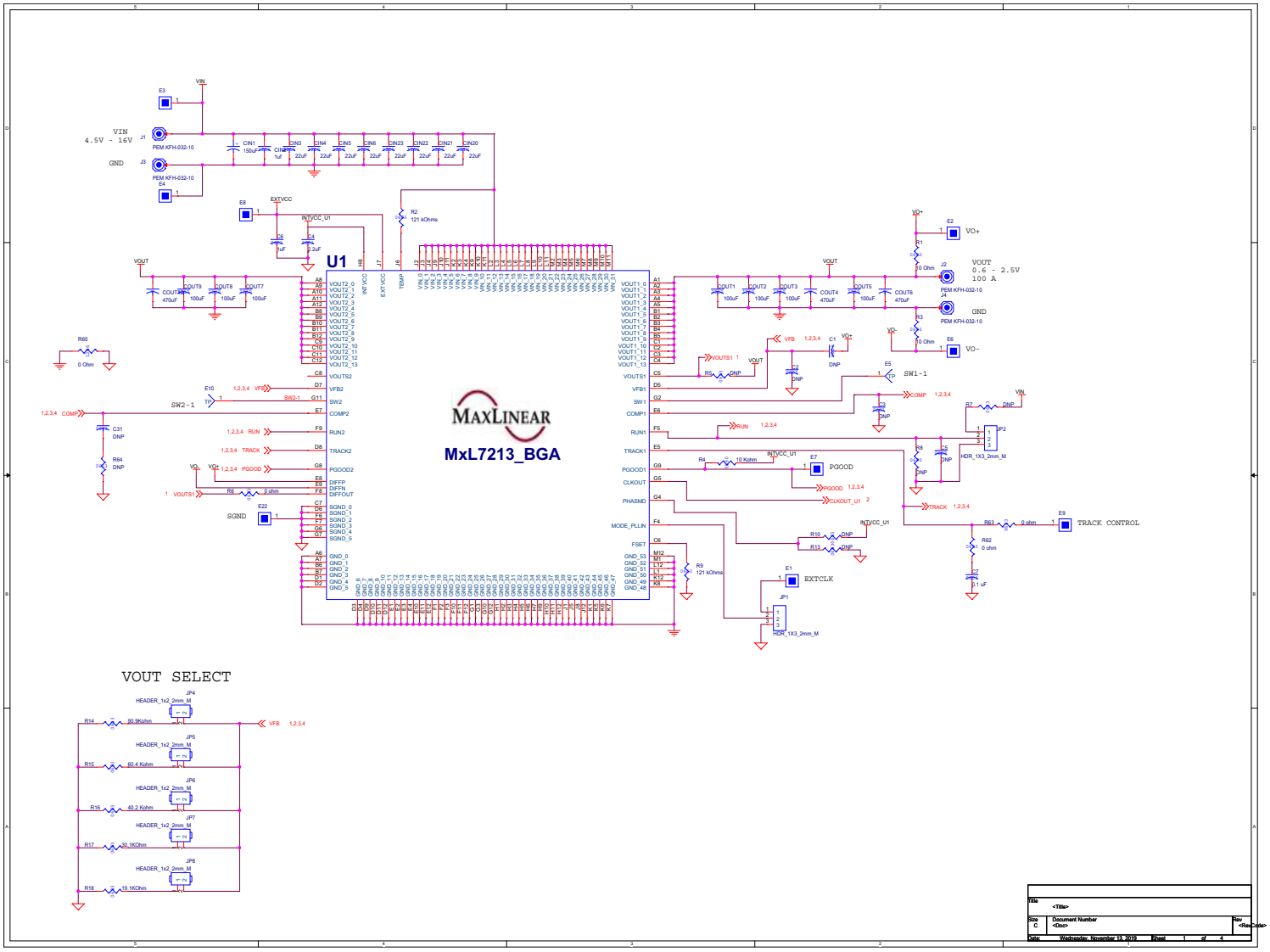


Figure 10: EVK Schematic

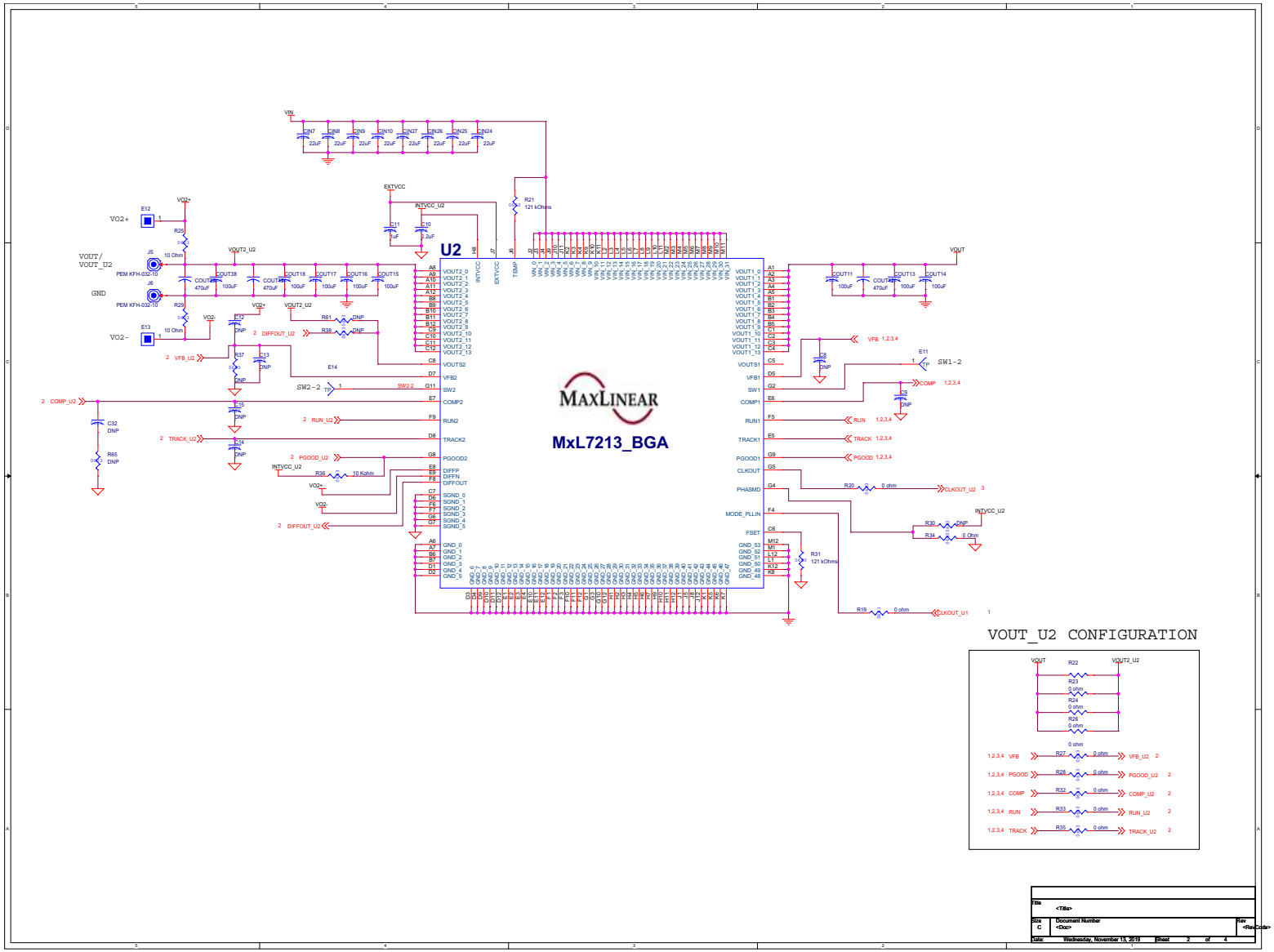


Figure 11: EVK Schematic, Continued

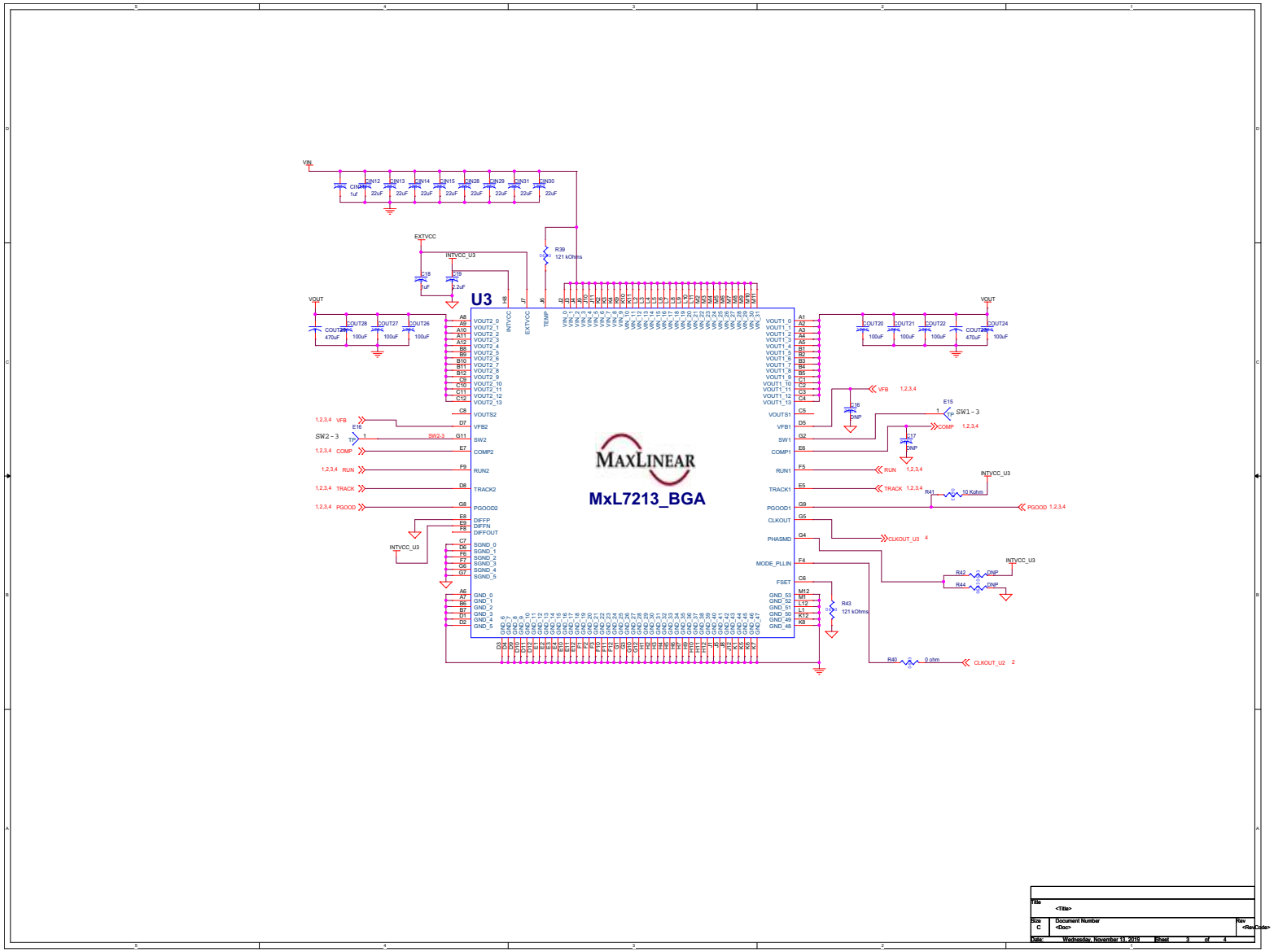


Figure 12: EVK Schematic, Continued

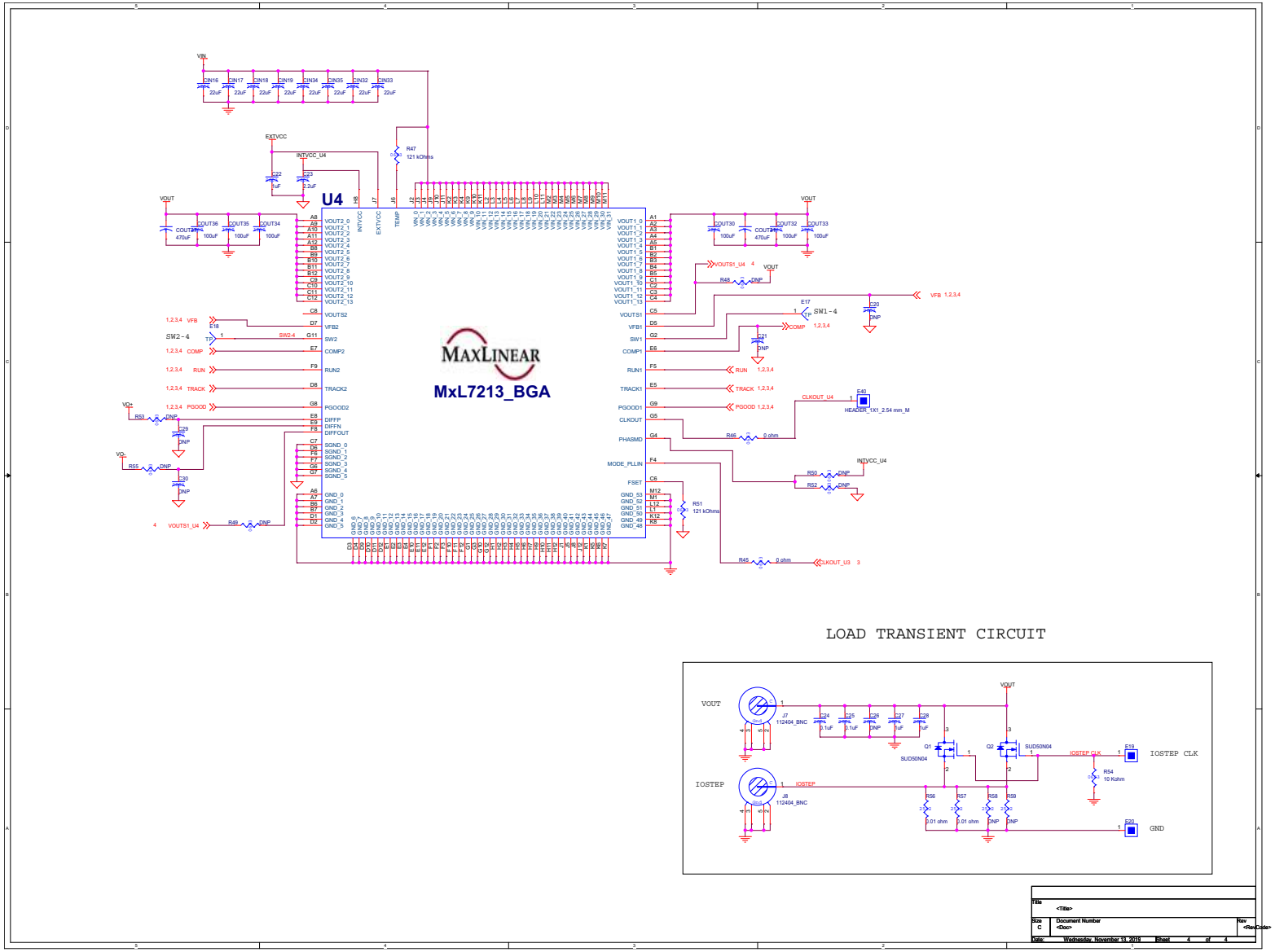


Figure 13: EVK Schematic, Continued

MxL7213EVK PCB Layers

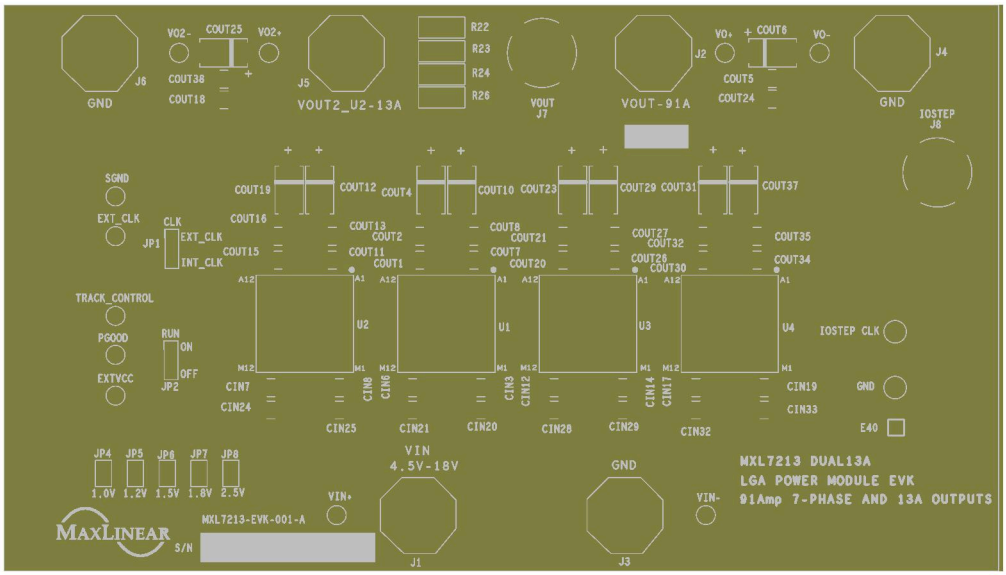


Figure 14: EVK PCB Silkscreen Top

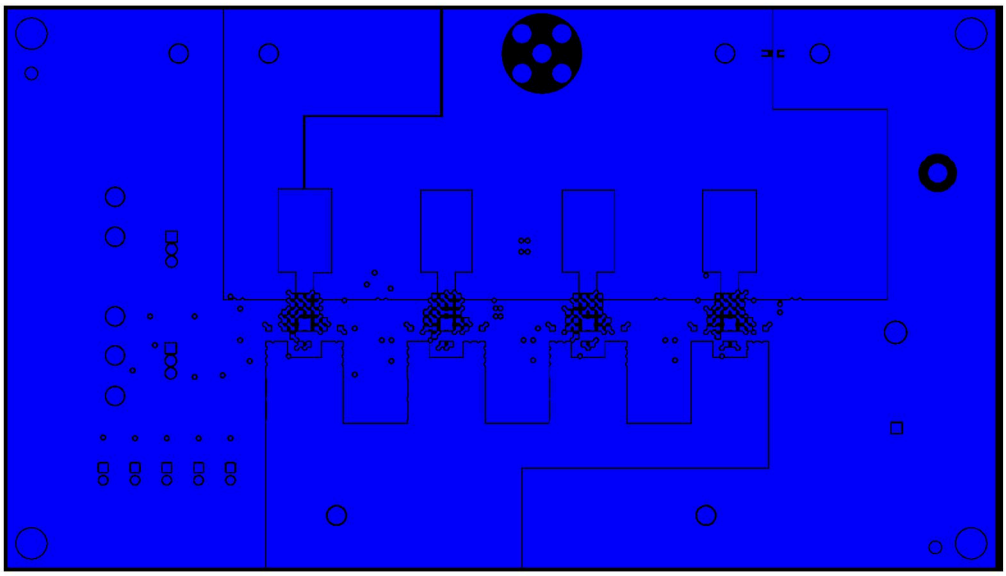


Figure 15: EVK PCB Layer 1

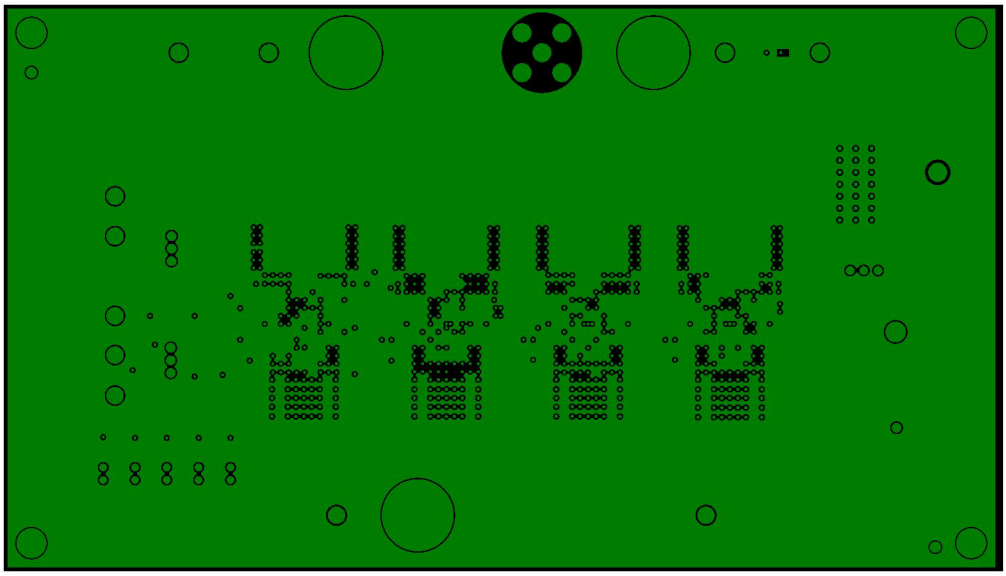


Figure 16: EVK PCB Layer 2

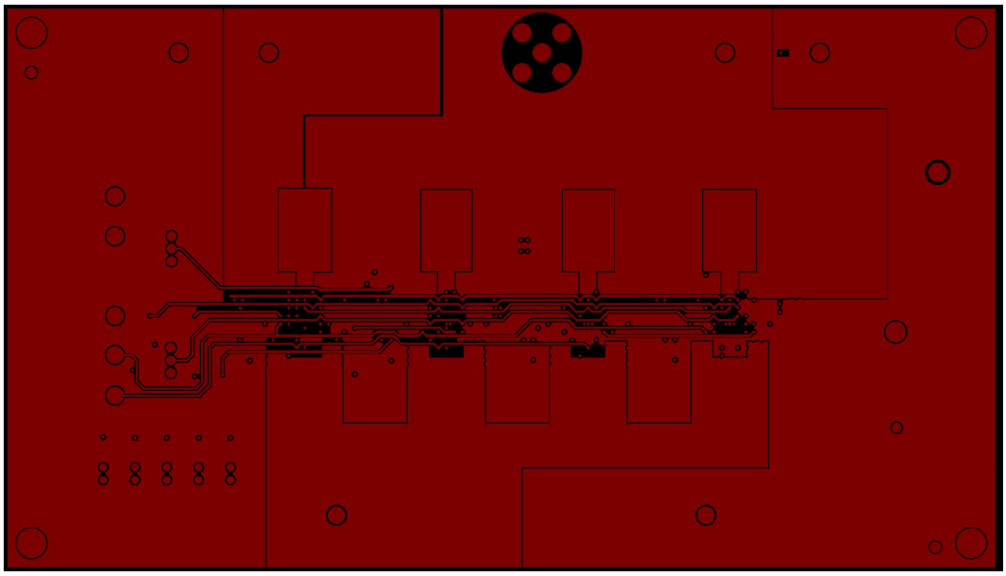


Figure 17: EVK PCB Layer 3

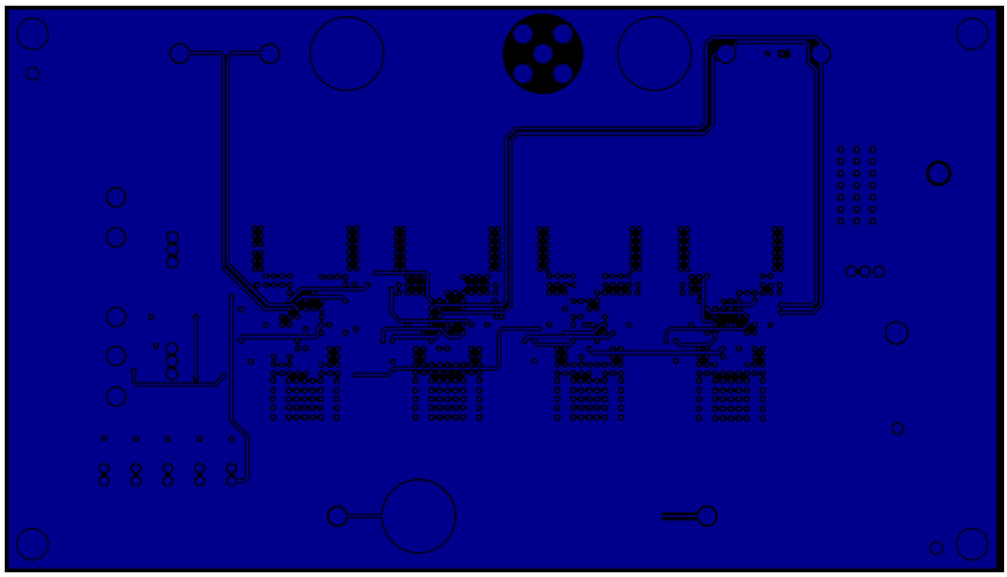


Figure 18: EVK PCB Layer 4

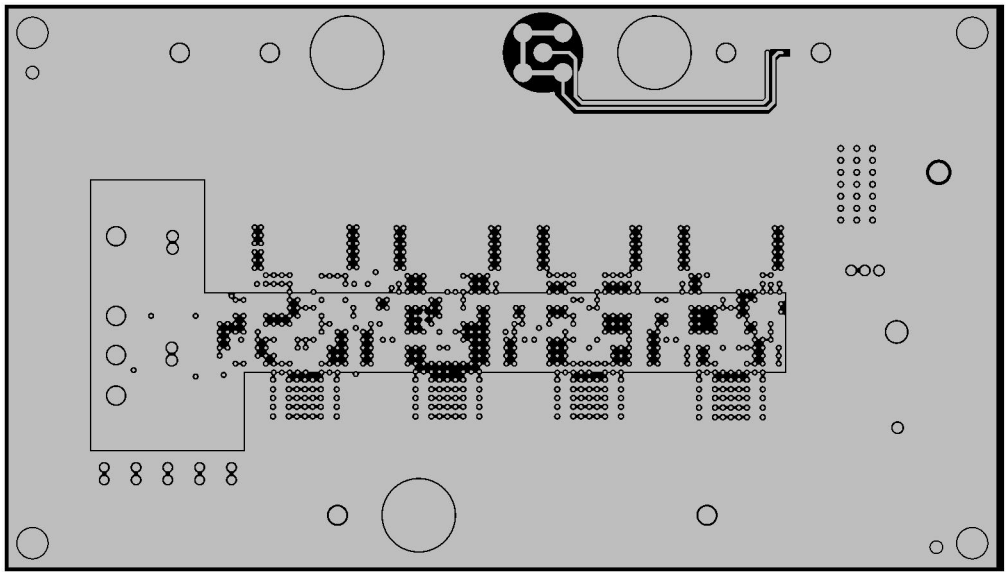


Figure 19: EVK PCB Layer 5

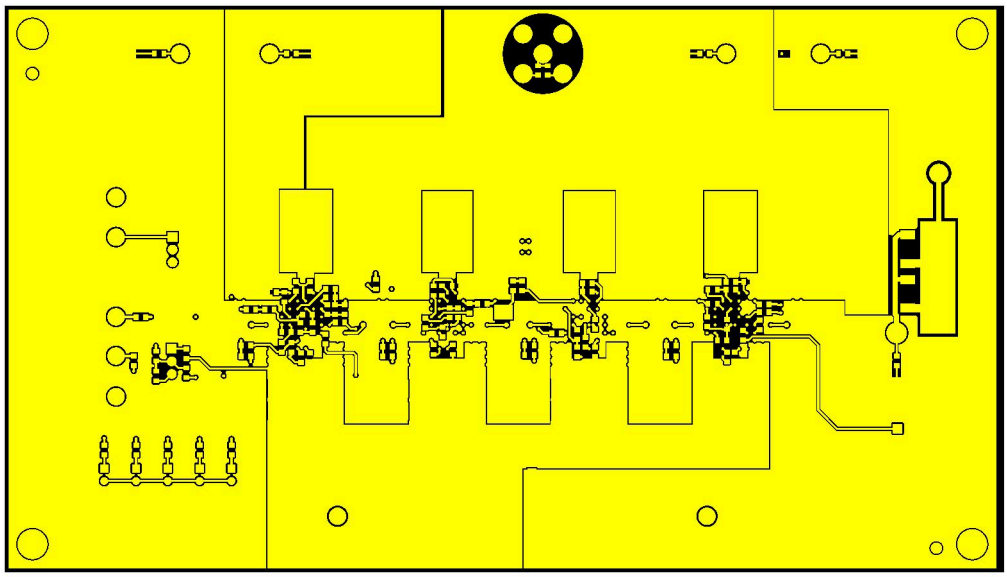


Figure 20: EVK PCB Layer 6

Figure 21: EVK PCB Silkscreen Bottom

MxL7213EVK Bill of Materials

Table 6: EVK Bill of Materials

Item	Qty	Reference Designator	Description	Manufacturer / Part Number
1	16	CIN3, CIN4, CIN5. CIN6, CIN7, CIN8, CIN9, CIN10, CIN12, CIN13, CIN14, CIN15, CIN16, CIN17, CIN18, CIN19	CAP X5R 22UF 25V 10% 1210	Murata GRM32ER61226KE15
2	8	COUT1, COUT7, COUT11, COUT15, COUT20, COUT26, COUT30, COUT34	CAP X5R 100UF 10V 20% 1210	Taiyo Yuden LMK325BJ107MN-T
3	8	COUT4, COUT10, COUT12, COUT19, COUT23, COUT29, COUT31, COUT37	CAP POSCAP 470UF 4V 20% 7343	Sanyo 4TPE470MCL
4	4	C4, C10, C18, C22	CAP X5R 2.2UF 10V 20% 0603	Taiyo Yuden LMK107BJ225MA
5	1	C7	CAP X7R 0.1UF 25V 10% 0603	AVX 06033C104KAT2A
6	1	R14	RES, CHIP 90.9K 0.06W 1% 0603	Vishay CRCW060390K9FKEA
7	4	R9, R31, R43, R51	RES, CHIP 121K 0.06W 1% 0603	Vishay CRCW0603121KFKEA
8	2	R1, R3	RES, CHIP 10 0.06W 5% 0603	Vishay CRCW060310R0JNEA
9	4	U1, U2, U3, U4	IC, POWER MODULES	MaxLinear MxL7213-AYA-T (LGA version) MaxLinear MxL7213-ABA-T (BGA version)
10	4	COUT5, COUT18, COUT24, COUT38	CAP X5R 100UF 10V 20% 1210	Taiyo Yuden LMK325BJ107MN-T
11	2	COUT6, COUT25	CAP POSCAP 470UF 4V 20% 7343	Sanyo 4TPE470MCL
12	1	C25	CAP X7R 0.1UF 25V 10% 0603	AVX 06033C104KAT2A
13	1	CIN1	CAP ALUM 150UF 25V 25% SUNCON-8	Suncon 25CE150AX

Table 6: (Continued) EVK Bill of Materials

Item	Qty	Reference Designator	Description	Manufacturer / Part Number
14	2	CIN2, CIN11	CAP X5R 1UF 25V 10% 1210	Taiyo Yuden TMK325BJ105KM
15	0	COUT2, COUT3, COUT8, COUT9, COUT13, COUT14, COUT16, COUT17, COUT21, COUT22, COUT27, COUT28, COUT32, COUT33, COUT35, COUT36 (OPT)	DNP	
16	0	C1, C2, C3, C5, C8, C9, C12, C13, C14, C15, C16, C17, C20, C21, C26, C29, C30 (OPT)	DNP	
17	6	C6, C11, C19, C23, C27, C28	CAP X7R 1UF 10V 10% 0603	Taiyo Yuden LMK107BJ105KA
18	1	C24	CAP X7R 0.01UF 100V 10% 0603	AVX 06031C103KAT2A
19	2	Q1, Q2	MOSFET N-CH 30V DPAK (TO-252)	Vishay SUD50N03-09P
20	4	R2, R21, R39, R47	RES, CHIP 121K 0.06W 1% 0603	Vishay CRCW0603121KFKEA
21	2	R25, R29	RES, CHIP 10 0.06W 5% 0603	Vishay CRCW060310R0JNEA
22	4	R4, R36, R41, R54	RES, CHIP 10K 0.06W 5% 0603	Vishay CRCW060310K0JNEA
23	0	R5, R7, R8, R10, R13, R30, R37, R38, R42, R44, R48, R49, R50, R52, R53, R55, R61 (OPT)	DNP	
24	14	R6, R19, R20, R27, R28, R32, R33, R34, R35, R40, R45, R46, R62, R63	RES/JUMPER, CHIP 0 OHM 1/16W 1 AMP 0603	Vishay CRCW060360K4FKEA
25	1	R15	RES, CHIP 60.4K 0.06W 1% 0603	Vishay CRCW060340K2FKEA
26	1	R16	RES, CHIP 40.2K 0.06W 1% 0603	Vishay CRCW060330K1FKEA
27	1	R17	RES, CHIP 30.1K 0.06W 1% 0603	Vishay CRCW060319K1FKEA
28	1	R18	RES, CHIP 19.1K 0.06W 1% 0603	Vishay CRCW060310K0JNEA

Table 6: (Continued) EVK Bill of Materials

Item	Qty	Reference Designator	Description	Manufacturer / Part Number
29	4	R22, R23, R24, R26	RES 0 OHM 2010	Tepro (Nakoma) RNH6083
30	2	R56, R57	RES 0.010 2W 1% 2512	Vishay WSL-2512-R01000-F-EA
31	0	R58, R59 (OPT)	RES 2512	
32	1	R60	RES/JUMPER, CHIP 0 OHM 1/4W 1 AMP 1206	Vishay CRCW12060000ZOEA
33	2	JP1, JP2	3 PIN HEADER SINGLE ROW	Wurth
34	5	JP4, JP5, JP6, JP7, JP8	2 PIN HEADER SINGLE ROW	

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