

# PowerArchitect 4 Quick Start Guide

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## Introduction:

PowerArchitect 4 (PA4) is Exar's intuitive and easy---to---use software for developing power supplies with the family of integrated power controllers. PA4 empowers engineers to create complex sequencing schemes, modify voltage, current and many other parameters in seconds. This guide intends to quickly introduce you to this powerful tool and start designing.

## **Downloading & Installation:**

- PA4 is provided on the supplied USB dongle for universal Power Management IC (PMIC) kits. If you do not have the USB dongle, you can download the latest version of PA4 from: <u>http://powerxr.exar.com.</u> You must register ( please follow the registration instructions).
- 2. Once downloaded, double---click ExarPowerArchitect\_setup.exe
- 3. After installing the software, you will need to plug in the evaluation, configuration or demo board in order to install the device driver (the driver is not automatically installed). First, plug---in the USB connector of the application board. Indicate to Windows that you would like to select the driver yourself and point to the directory where software is installed. Choose the driver file: **ExarAppBoard.inf** in the directory and follow the instructions to complete installation.
- 4. You should now be able to launch and recognize PA4 and boards.

## **Device Selector:**

The device selection window provides an option to choose between two families of programmable PMICs, XR77103 or XRP7704/08/13/14/40.



## XR77103

At this time XR77103 EVB should be powered up and XCM connected to PC USB port (see XR77103EVB User Manual for reference).

Clicking on the XR77103 radio button as shown above will bring up the configuration tab:

le He													
onfig	Overv	iew											
Syste	m											Registe	rs
Vin (V	)	12.00	•	UVLO (V)	7.0	•	I <sup>2</sup> C Addr	0x75				0x00	0x32
Freq (	(MHz)	0.5	•	Low Power	Enable	•	Phase	Ch 1/	2 - 0°, C	h 3 - 180° 👻		0x01	0x14
												0x02	0x8
Chan											1	0x03	0x12
Chan	nels			Peak Inductor								0x04	0x21
Outpu	ut 1	Vout (V)	1	Current Limit (A	) T delay	(ms)	T start (m	is) P	nase	Select		0x05	0x30
1	3	.3	•	3.5 👻	10.0	•	3.0	•	0		PGOOD	0x06	0x5
2	1	.8	•	3.5 👻	20.0	•	2.0	•	0			0x07	0x5
3	1	.2	-	3.5 -	30.0	•	1.0	-	80°	J-L		0x08	0x5
												0x09	0x42
												0x0A	0x4f
		Rea	IA E	Write	All	Progr	am	Disabl		Enable			04.11
Com	pensa	tion											
				(	Comp Free	(MHz)	0.5	•					
		Vin ()	0	Vout (V)	L (uH	)	Cout (uF)	Rcomp	(kohm)	Ccomp (nF)			
		12/5.0		1.0	2.2	1	22 x 3	10		4.7			
		12/5.0		1.2	2.2		22 x 3	10		4.7			
	Ĩ	12/5.0		1.5	3.3		22 x 3	20		4.7			
		12/5.0		1.8	3.3	Ţ,	22 x 2	20		4.7			
	i i	12/5.0	_	2.5	4.7	T)	22 x 2	20		4.7			
	1	12/5.0	-	3.3	4.7		22 x 1	20		4.7			
	i i	12		5.0	6.8	1	22 x 1	20		4.7			

In the lower left corner, PA4 will display information that it is communicating with XCM. In addition, it will prompt the user that it found XR77103 at the I<sup>2</sup>C address shown in the I<sup>2</sup>C address box.

#### **System Settings**

Under system settings, user can select:

- Vin in Volts this value need to match actual Vin supplied to the device. PA4 will use this number for duty ratio and UVLO calculations
- **UVLO** limit in Volts for Vin of 9V or 12V, both settings (7V and 4.2V) can be used. However, when Vin is 5V, the UVLO limit must be set at 4.2V.
- I<sup>2</sup>C Address the box displays the address PA4 is found at. XR77103 I2C address can be 0x74 or 0x75 (7-bit hex representation) depending on the state of the A0 pin (pin #3). This box cannot be used to set the address.
- **Switching Frequency** in MHz user can select switching frequency from 0.3MHz to 2.2MHz in 0.1MHz steps. PA4 will limit switching frequency selection based on the device minimum on time.
- **Low Power** mode this box enables or disables the low power mode. Enabling the low power mode allows pulse skipping operation to minimize power losses at light loads on all channels.
- **Phase** relationship among channels in degrees user can select phasing between channels; all channels can operate in phase or one channel operates 180° out of phase with the other two channels.

#### **Channel Settings**

The channel section covers parameters that are set for channels individually.

- **Vout** in Volts user can select output voltage from 0.8V to 6.0V in 50mV steps. The pull down menu is active during operation for purpose of dynamic voltage scaling. PA4 will limit voltage selection based on the device minimum on time.
- **Peak Inductor Current Limit** in Amperes User can select peak inductor current limit from 1A to 4A in 0.5A steps.
- **Start-up delay time** in milliseconds User can select different start-up delay times referenced to the EN pin going high. The times are relative to switching frequency; PA4 takes this into account.
- **Start-up time** in milliseconds User can select different start-up rates. The times are relative to switching frequency; PA4 takes this into account.
- **Phase** relationship among channels in degrees This box will display current phase setting stored in the device. The box cannot be edited.
- **Select** Checking the select boxes a user selects which channel will be enabled at the EN pin going high.

#### Power Good

Power Good indicator is the only live feedback from the running device. PA4 will constantly poll the signal. Only selected channels affect Power Good.

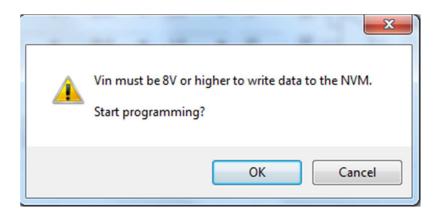
#### **Configuration Programming and Reading**

Customer configuration can be written to run time registers or permanently stored into Non-Volatile Memory

(NVM).

Use the "Write All" button to write to the run time resisters. All registers (0x00 to 0x0A) get written using this function in a numerical sequence.

Clicking on the "Program" button will initiate the process of storing the configuration data into NVM.



PA4 will prompt the user to make sure Vin is above 8V in order to programming process to go through. The device running from Vin below 8V cannot be programmed. Confirming that Vin is above 8V, a user initiates the programming process. PA4 pulls the device nWR pin to logic low and starts sending the configuration bytes to the device NVM.

Neither writing nor programming function is available while the device is regulating.

The "Read All" button initiates reading of all run time registers (0x00 to 0x0A). The read values are displayed in the "Registers" column to the right. PA4 will also update the configuration selectors based on the read values. The reading function is available in the running system.

#### Enable/Disable Channels

Using "Enable" and "Disable" buttons, PA4 will control start-up and shut-down of the selected channels. Once channels are enabled, PA4 will disable most of the configuration selectors, as well as the writing and programming routines.

nfig Ov	anview							
System							Regist	are
Vin (V)	12.00	UVLO (V)	7.0 -	I <sup>2</sup> C Addr	075		0x00	0x32
	12.00		7.0 *	J	0x75			
Freq (MH	iz) 0.5	Low Power	Enable 👻	Phase	Ch 1/2 - 0°, C	h 3 - 180° 👻	0x01	0x14
							0x02	0x8
Channe							0x03	0x12
Chaline	10	Peak Inductor					0x04	0x21
Output	Vout (V)	Current Limit (A)	T delay (ms	) T start (n	ns) Phase S	Select	0x05	0x30
1	3.3 👻	3.5 💌	10.0	- 3.0	~ 0°		0x06	0x5
2	1.8 -	3.5 👻	20.0	- 2.0	~ 0°		• 0x07	0x5
3	1.2 -	3.5 👻	30.0	-	v 180°		0x08	0x5
							0x09	0x42
	Read A	Write A	dl Pro	ogram	Disable	Enable	0x0A	0x4f
Compe	nsation	c	omp Freq (Mł	Hz) 0.5	•			
	Vin (V)	Vout (V)	L (uH)	Cout (uF)	Rcomp (kohm)	Comp (oE)		
	12/5.0	1.0	2.2	22 x 3	10	4.7		
	12/5.0	1.2	2.2	22 x 3	10	4.7		
	12/5.0	1.5	3.3	22 x 3	20	4.7		
	12/5.0	1.8	3.3	22 x 2	20	4.7		
	12/5.0	2.5	4.7	22 x 2	20	4.7		
	12/5.0	3.3	4.7	22 x 1	20	4.7		
	12	5.0	6.8	22 x 1	20	4.7		

The only dynamic change allowed is voltage scaling. Again, reading run time register values is permitted.

#### **Frequency Compensation**

PA4 will display static tables listing recommended component values for properly frequency compensating the device. The drop down menu selects between two operating conditions: 0.5MHz and 1MHz switching frequency.

#### Menu

Under the menu selection, user can find a way to save new, load existing design.

File	Help	
45	Load	1
	Save As	
	Export	۰
	Exit	

Moreover, the NVM configuration can be exported in the Intel hex format.

File	PowerArchitect 4	the local division of the local division of the
	Load Save As	
	Export +	Intel Hex
	Exit	Low Power Enable -

## XRP7704/08/13/14/40 Family

Selecting this family will bring up the configuration selector window.

## **Configuration Selector:**

The configuration window provides the user with the option to choose the version of the board that is being modified. If you do not have an evaluation or demo board attached or do not want to start from this wizard, press **Cancel**. This in turn, forces the software to customize menus and options particular to that version. For example, if the user is trying to do a design based around the XRP7714 Evaluation Board, then the software will customize the menus so that the user will have the ability to configure four channels. As a further example, selecting the XRP7713EVB---DM01 option will only allow the user to configure three channels. For ease of understanding the basic configuration of each option is available in the right side of the configuration menu box.

Create New Configuration Based	d on Template		
XRP7714EVB	Configurati	on Template Descripti	on
© XRP7740EVB-Version A	х	RP7714 Evaluation Template	Board
© XRP7740EVB-Version B		Input Voltage: 1	2V
	Channel	Output Voltage	Max. Current
© XRP7704EVB	1	3.30V	3.00A
© XRP7708EVB	2	2.50V	3.00A
O XRF // OCLVD	3	1.80V	3.00A
© XRP7713EVB-DMO1	4	1.00V	3.00A
	Create Configur	ation	

## **Power Design:**

The power stages of the supply are designed within the **Power Design tab**. This is a key section in generating the configuration file for a given design.

ile <u>D</u> ebug Help		
Current File: C:\svn_local\DPS_GU	I\xrp7704app\test.cfg	
verview Demo Power Design	Digital Design Customer Info	
	General Vin Operating Max 12.0 🖨 UVLO Warn 4.8 🚔 UVLO Fault 4.7	A V
	Clock Faults Switching Freq 300kHz  Over Temp Shutdown (c	c) 155.0
	System Clock 38.4MHz / 128 Over Temp Restart (C	c) 135.0
	Reset Chip on clearing of Ignore Faults on: OTP OCP OVP	-
	Channel 1	Program Chip
	Vin 12.00 Vout 3.30 Vout 3.30 Vout Compared by the compared by	nize Gate Charge
	Tstart (ms) 2.00 Tstop (ms) 2.00 Low Fet: Fairchild FDS	8984 30mΩ
	Rise (ms)         3.25         Fall (ms)         2.00         Capacitor:         2x 65uF 6.           PG delay (s)         0.400         PG %         30.00         Inductor:         4.89uH 16.	
	Shdn Thresh 0.10 + OVP Level 3.900 •	
	Faults will follow on: CH2 CH3 CH4 Advanced	Edit

General: Vin (Nominal input voltage), UVLO (Under Voltage Lock Out) warning thresholds and fault thresholds are entered in this General Box. This is where the input voltages to the controller are defined. This is not necessarily where the input voltages for the power stages are entered IF they are different from the input voltage to the controller.

**Clock:** Switching Frequency of the buck converters is specified here. The pop---up table shows clock frequencies of the chip's internal voltage controlled oscillator for the digital logic in the first row. The digital clock is divided into power switching frequencies displayed in relative columns. There is no real advantage to choosing one digital clock frequency over another so choose the switching frequency that is desired.

Faults: OTP (Over Temperature Protection) shutdown and OTP restart points are specified here. Check the box to reset the chip after clearing UVLO condition if you want the controller to forget its volatile configuration every time the fault clears. This requires reprogramming of the registers. If you want the part to retain its configuration then uncheck this box. By choosing any combination of OTP, OCP, OVP PowerArchitect Quick Start and UVLO, the user can choose to ignore certain faults for troubleshooting, debugging, etc...

**Channel Design:** This is where the input voltage, output voltage, and output currents are specified for each channel. Inputs here are used to automatically pick components and determine control loop coefficient values. Also here is where you define your sequencing timing with Tstart, Rise, Tstop, and Fall. Other functions are also configured here such as the shutdown threshold, PGOOD percentage threshold, PGOOD delay, and fault behavior parameters. Lastly, the default values for phase are Ch1 @  $0^{\circ}$ , Ch2 @  $90^{\circ}$ , Ch3 @  $180^{\circ}$  & CH4 @  $270^{\circ}$  degrees.

Active Shutdown on Fault: This configures the fault behavior of a channel to latch the low side FET ON to discharge the output capacitors when a fault happens. This will bring the output voltage down very rapidly. If this box is unchecked a fault will cause a channel to simply stop switching. This is also known astri---statingthe output.

Faults will follow on CH2/CH3/CH4: Specifies whether the channel being configured fault in conjunction with the selected channels if that channel faults.

Automatically Pick Components: Allows PA4to select appropriate FETs, capacitors and inductor for each channel. Once satisfied with the components for a channel, this can be unchecked so that components will remain fixed. It is also an option to check Optimize FETs (Minimize Gate Charge) to optimize the high and low FETs for minimal gate charge for this channel. Components selected will be displayed in this area and can be edited in the Edit window (see the Edit button description below).

Advanced...: This button brings up a window for optimizing the PID loop. See the section on the PID Calculator Window below for more information.

**Edit**...: This button will bring up a window that allows the user to specify component values they would like to use for the channel being edited. Pressing the Edit button will bring up the Part Editor window (see picture below). In this window one can override any component or value automatically selected by the GUI. These values will be saved in the configuration file and automatically used in the PID loop calculations for each channel.

gh FET		Low FET		Capacitor			Inductor	
Manufacturer F	airchild	Manufacturer	Fairchild	Quant	tity	2	Manufacturer W	/urth
Part Number F	DS8984	Part Number	FDS8984	Manufacturer	NA		Part Number 74	44310200
RDSON (mOhn	n) 30.0	RDSON (mOh	nm) 30.0	Part Number	C32	25X5R0J476M	Inductance (uH)	4.9
gate Charge (no	c) 7.0	Qgate Charge (r	nC) 7.0	Capacitance (	uF)	65.0	IDC Max	6.5
				ESR (mOh	nm)	30.0	DCR (mOhm)	16.5
				Vrat	ting	6.3		
			ОК	Cancel				

*Note:* If **Optimize FETs (Minimize Gate Charge)** option in channel design is selected, there would be separate columns for each FET.

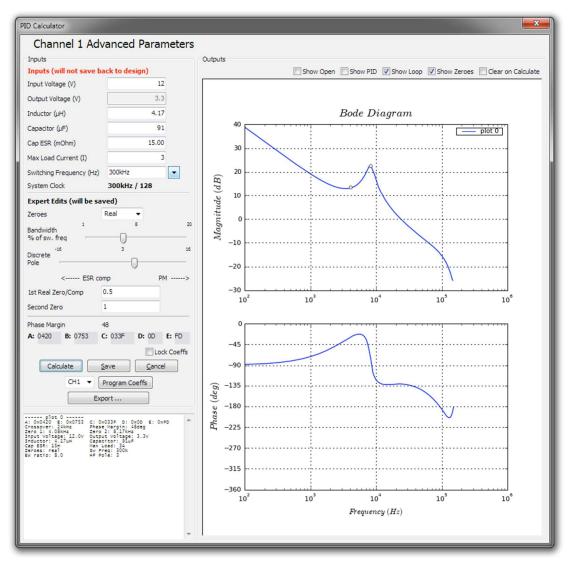
After editing each channel, select File: Save Design... and save the settings to a configuration file.

#### **Programming Chip (Volatile Memory)**

After customizing the design and saving the settings to a configuration file, one can program the volatile memory to test the design. In order to program the chip, one needs to make sure that the power is applied to the input pins of the EVB and that the board is connected (File: Board Search will confirm if the board is connected or not). If the board is not connected, then the Demo tab will be grayed out. After confirming that the board is connected, press the **Program Chip** button. If the program executes properly, a window will pop up stating success! Once volatile memory has been programmed successfully, one can go to the demo tab and verify the design.

## **PID Calculator:**

The PID Calculator is accessed by clicking on the Advanced button in the Power Design tab and is used to calculate PID coefficients (i.e. register settings for the feedback loop parameters) for that particular channel.



Keep Input Voltage, Max Load Current & Switching Frequency at default values. Default settings are usually not changed. The proper use for changing these values is to check the Lock Coeffs box and plot curves for several "what if?" scenarios such as the minimum and maximum input values, extreme tolerance deviations of the components, etc. Manually entered values are not saved here.

Inductance: This is set to true inductance in circuit at full load.

**Note:** The GUI automatically de---rates the inductance by 15% from its no load rating. This must be accounted for if different inductors than those selected by the GUI are used. For instance some inductors are used at an operating point that is de---rated to different values, which is best done by inflating the inductance value using the Edit button on the Power Design tab.

**Capacitance:** Set it to what you believe is the true output capacitance.

**Note:** Based on the output voltage, the GUI automatically de---rates the ceramic capacitors it recommends because ceramic capacitors lose capacitance with DC bias. This must be accounted for if different capacitors than those selected by the GUI are used. For instance if polymer electrolytic capacitors are used they will be improperly de---rated between the part selector window and the Advanced window. Just like with inductors above, the proper way to adjust for this is to inflate the inductance value using the Edit button on the Power Design Tab to compensate.

**Cap ESR:** If changing the capacitor or using a capacitor style other than ceramic, then be sure to enter the correct ESR for that component here. ESR plays a big role in control loop calculations so it needs to be an accurate value. Remember that manually entered values are NOT SAVED here.

Inductance, Capacitance & ESR: These physical component values affect the control loop gain & phase. If adjustments to the PID loop below don't give an acceptable result, then it may be necessary to look at different components.

**Note:** Manual changes are **NOT** saved and must be entered using the **Edit** window for that particular channel.

**Expert Edits:** Expert Edits are used to optimize the control loop. The bandwidth slider is used to set loop bandwidth as a % of switching frequency. Generally speaking more bandwidth yields a better transient response and can help minimize the amount of capacitance needed for any given desired transient response. Typically from 5---15% is a solid performing range. The Discrete Pole slider is an input for manipulating a high frequency pole. The best practical use of this slider is for manipulating the amount

of phase and gain margin that are achieved in the control loop. Next, zeros can be set as a % of the crossover frequency here. Zeroes counter the effect of the two poles introduced by the inductor and capacitor. Generally their default positions are solid values. One can also select Complex Zeros in Zeros dropdown menu. Generally complex zeroes are not necessary and real zeroes should be used. Computed PID Coefficients and Phase Margin are shown in below the Expert Edits.

Note: Phase Margin will appear in **bold red** if it is less than 45°.

Select Lock Coeffs to fix the computed control loop coefficients after making any expert edits. Locking coefficients is necessary if you want to plot new gain and phase curves after making any changes to the inputs such as input voltage, output current, or inductance without PA4recalculating the control loop PID coefficients.

Click **Calculate** after making changes to see what effect it has on the loop. If the Lock Coeffs box is checked, then the calculate button is relabeled at **Plot**. When satisfied, click **Save** and changes will be saved to the configuration file next time it is saved to disc.

**Note:** One can program chip's volatile memory directly by clicking **Program Coeffs** button. This will **NOT** be saved to the configuration file if you exit the PIC Calculator window unless **Save** is pressed afterward. Pressing **Save** closes the PID Calculator window.

#### Programming Chip (Volatile Memory) after adjusting PID Coefficients:

After customizing the design and saving the settings to a configuration file, one can program the volatile memory to test the design. In order to program the chip, one needs to make sure that the power is applied to the input pins of the EVB and the board is connected via USB to a personal computer.

PA4may automatically detect the controller. However, if it is not found, then selecting **Board Search** in the **File menu** will search the PC's com ports and confirm if the board is connected or not. If the board is not connected, then the **Demo** tab will be grayed out. After confirming that the board is connected and no warning messages are seen, press the **Program Chip** button. If the program executes properly, a window will pop up stating **success!** Once volatile memory has been programmed successfully, one can go to the **Demo** tab and verify the design.

**Note:** If a warning message stating that the phase margin for one or more channels is less than the minimum recommended 45 degrees shows, then one can resolve this by using the Advanced button in the Power Design tab for that channel.

## **Digital Design:**

GPIOs and other I---O parameters are programmed under Digital Design tab.

🗴 Exar PowerArchitect - ver 3.00	D					
File <u>D</u> ebug Help						
Current File: C:\svn_local\DPS_C	GUI\xrp7704a	p\test.cfg				
Overview Demo Power Design	Digital Desig	Customer I	nfo			
	I2C Serial C	-				
	Are you g	oing to use I2C	Hardware Address	0 🚔 🔲 Use GPIO3	to control LSB of I2C address.	
	No @					
	Standby LD					
	Vout					
	3.3 V	I2C Com	mand Only			
	© 5.0 V					
		GPIO AN	D I2C command			
		Immediat				
	Channel Cor	nfig				
	Ch1 Enab	e	Ch2 Enable	Ch3 Enable	Ch4 Enable	
	I2C On	y	I2C Only	I2C Only	I2C Only	
	O GPIO O	GPIO Only     GPIO Only		GPIO Only	GPIO Only	
	GPIO A	ND I2C	GPIO AND I2C	C GPIO AND I2C	C GPIO AND I2C	
	Immedia	ate	Immediate	Immediate	Immediate	
	Synchroniza	tion				
	CLK_IN	(III)	CLK_OUT / SYNC_OUT			
	SYNC_IN		ernal Oscillatori			
	-GPIO Chann					
	GPTO Chann					
	GPIO 0 Dis		•	ve before continuing to this s		
	GPIO 1 Cor	ntrolled by GPI	O_ACTIVE reg ▼			
	GPIO 2 Cor	ntrolled by GPI	O_ACTIVE reg ▼			
	GPIO 3 Dis	able	•			
	GPIO 4	12C - 5	SDA			
	GPIO 5	12C - :	SCL			
				Apply		
					Update to Chip	

#### **I2C Serial Config:**

It is advisable to check the Yes box next to Are you going to use I2C? By setting it to No, you will lose the ability to talk to the chip. If you program the NVM memory with the box check No and then cycle the power the ability to talk to the part via I2C will be lost permanently. Use GPIO3 to control LSB of I2C address to configure the default address on a blank part to change from 0x00 to 0x01.

Note: This requires a hardware addition of a 100k pull---up resistor to VDDA on GPIO3.

The purpose of this is to make it possible for a microprocessor to address multiple blank chips on the same I2C bus. The intent is that a microprocessor will be able to command this second address without conflict, and load the registers to make the controller respond properly to the 0x01 address (or any other address from 0 to 64). After a new address has been assigned in the I2C address register GPI03 can be reconfigured to be used for any of the other GPI0 capabilities. The pull---up resistor present will not impact this functionality.

#### Standby LDO Config:

This pane is used to select which output voltage will be generated by the standby linear regulator. The enabling method for the linear regulator is also chosen here from the radial button menu. Of particular note is the GPIO AND I2C command selection. In this case there is a logical AND to enable the rail. Thus both an I2C command to set the enabling bit in a register is required as well as a GPIO toggle (set in the GPIO Channel Configuration section – see below).

#### **Channel Config:**

As above, these panels are used to select the enabling mechanism for each channel. The **Immediate** option will power the rail as soon as the controller has stable input voltages. **GPIO Only** will wait for an assigned GPIO pin to toggle to its active state (set in the GPIO Channel Configuration section – see below). **I2C Only** is the default in the PA4and requires an I2C command to turn the channel on. Lastly the **GPIO AND I2C** selection is a logical AND to enable the channel. Thus both an I2C command to set the enabling bit in a register is required as well as a GPIO toggle

#### Synchronization:

This option is used to assign the GPIO pins necessary to be a master or a slave for synchronizing multiple controllers. Auto Switch back to Internal Oscillator to instruct a slave synchronized controller to revert to its own voltage controlled oscillator if the clock signals present on the assigned GPIO pins fall out of the acceptable frequency range for synchronization. If this option is not selected then the absence of a clock on the GPIO with an acceptable range of the controllers programmed frequency will cause the controller to stop activity until the clock becomes present.

#### **GPIO Channel Configuration:**

This box is used to customize GPIO functionality. If any channel to be enabled is set to **GPIO Only** or **GPIO AND I2C**, as mentioned above, it is up to the user to make sure to configure a GPIO to enable

appropriate channel(s). Several other warnings and faults can be sent to the GPIO output and Inputs/Outputs can be set Active High or Active Low.

Click Apply to save settings when GPIO configuration is complete. Update to Chip will write any changes made on this tab to the active controller if desired.

Note: Save configuration file after completing modifications to the Digital Design.

#### Demo:

The Demo tab is a good place to do some basic telemetry, margining, four corners testing, and development work in real time. The Demo tab reflects most of the telemetry available to the user for polling including PGOOD (power good) status, voltage measurements of peak switch current, output voltage, input voltage, junction temperature, and GPIO status.

	n_local\DPS_GUI\	orp7704app\test.cfg						
erview Demo p	ower Design Dig	ital Design Custom	er Info					
Channel Config								
Output	Status	SetP	oint Vout	easured Iout	I limit (A)	T start (ms) T stop	(ms) Phase	PGood Control
1		3.30	0.16V	n/a	7.333 🚔	2.000 2.000	0°	ON OFF
2		2.50	2.52V	0.000 A	7.000	2.000 🚔 2.000	90°	ON OFF
3		1.80	0.08V	n/a	7.166	2.000 2.000	180°	
4		1.00	0.08V	n/a	7.166	2.000 2.000	270°	
LDO		3.3V	•					ON OFF
								All ON OFF
General		GPIO Config						
Vin	10.6V		GPI00	GPI01	GPI02	GPI03	GPI04	GPI05
Junction Tem	p 32°C	Configuration	Disabled	Disabled	Disabled	Disabled	SDA	SCL
soft	reset	Status	1	1	1	1		
		Toggle Pin	HL	HL	HL	HL		
Board Connected C	OM19		i2c addres	s 0 🗘 Set	ti2c Address	Program Chip Upda	ate All 🔽 Aut	to-Update 2 sec

- When "Vin" is applied to the demo board, the contents of the '**NVM**' (Non---Volatile Memory) are transferred to the volatile state machine register **memory**. Initially, every part received from Exar will be blank (un---programmed NVM).
- To load a previously customized setup, select a configuration file by selecting Load Design from the file menu. If you do not have a configuration file, then skip this step and proceed to the Power Design section to find out more about creating a configuration.

#### **Channel Config:**

This section displays status of each channel, measured values of Vout and lout. It allows the user to modify the set point for 'I limit (A)', Start and Stop times for each channel, and the target voltage for each output. Users can also turn any particular Channel **ON** or **OFF**. Users can also use the ""**AII**" option to turn all the channels ON or OFF simultaneously.

#### General:

Nominal input voltage (**Vin**) and **Junction Temp** values are displayed here. **Junction Temp** represents current junction temperature of the part not the ambient temperature of the circuit board. Controllers can also be reset by pressing the **soft reset** button.

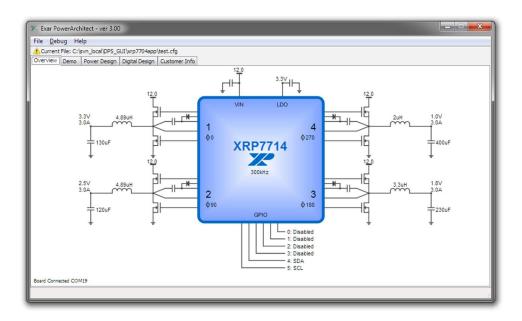
#### **GPIO Config:**

When the GPIO configuration in the Digital Design tab is changed, the description of the configured GPIO will change in the Configuration box. The **Status** box informs the user whether the current logic level on the GPIO pin is logic high or logic low. The **Toggle Pin** will show [**H**] [**L**] highlighted to represent what the user has selected on a particular **GPIO** pin if it has been configured as an input. Thus the user can control the GPIOs as an input using the toggle buttons.

The last option in the demo tab is fairly explanatory. The controller can have its **I<sup>2</sup>C address** reassigned and set. The **Program Chip** button will update the register values in the controller with the current values determined by the PowerArchitect. This is the button used for programming blank chips with saved configuration files and updating the chip with changes made in the PowerArchitect. Lastly there are options for controlling how often the PA4will poll the controller for information to populate the **Demo** tab. If the Auto----Update box is selected then the polling will occur at a rate set in the text box to the right of the check box. If the **Auto----Update** box is not checked, then the **Update All** button will need to be clicked for the Demo tab to refresh all the data fields.

#### **Overview:**

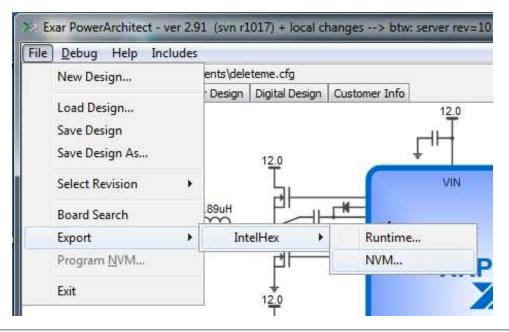
After programming non-volatile memory, the schematic of the chip program that was created can be viewed in overview tab. This includes Vin (for each channel), V<sub>out</sub> & I<sub>out</sub>, inductance and capacitance values for each channel. The GPIO settings are also displayed.



## **Customer Info:**

You can use this tab as a template for submitting application information to Exar for obtaining a quotation, technical feedback or prototype parts via email. You will need to attach the **configuration** file AND the **Intel Hex** file in order to obtain programmed samples.

Current File: C:\svn_local\DPS_GUI\xrp7704app\test.cfg	
Overview Demo Power Design Digital Design Customer Info	
Comments       Edit         Timestamp       Wed, 07 Jul 2010 15:27:05 +0800         Company       Example Inc         Contact       Joe Smith         Phone       510-123-4565         Email       me@exar.com         Program       Please find my XRP7704 Configuration         Program       Please find my XRP7704 Configuration         Program       Please find my XRP7704 Configuration         Part Number       Contact: Joe Smith         Comments       Comments         Program ::       Program ::         Program ::       Program ::         Comments       MDSSUM: 34780e54c5a2b37c2502f31         Thanks.       Thanks.	n attached.



**Note:** It is important that if you want to receive programmed parts from either Exar or Exar's distribution partners, you MUST include both the configuration file and the IntelHex file (see above graphic).

## **Other Features:**

#### **Program NVM**

After customizing the design and saving the settings to a configuration file, if required, one can then program the Non---Volatile Memory (NVM) of the controller.

Note: It is not recommended to program the evaluation or demo boards.

In order to program the chip, you need to make sure that the power is applied to the input pins of the evaluation or demo board, and that the board is connected is connected via USB to a personal computer with PA4installed. If the PA4does not find the evaluation board present on a COM port, then select **Board Search** from the **File** menu. It will confirm if the board is connected or not. If the board is not connected, then the **Demo** tab will be grayed out. In the **File** menu, select **Program NVM....** A warning dialog telling you the chip has already been programmed will pop up. Click **OK** to bypass the warning message and proceed. Next you will see a popup window showing the **Registers to be Programmed**. Users can inspect the registers for accuracy before clicking **OK**. Finally users will see a dialog box asking to make sure that they would like to proceed with programming NVM since it is a permanent action.

**Note:** Make sure that **GPIO**s are programmed such that the chip can be enabled once the **NVM** is programmed.

≫: Ek	ar PowerArchitect -	ver 3.00				
File	Debug Help					
	New Design	μ	I\xrp7704app\test	t.cfg		
-	Load Design		Digital Design Cu	stomer Info	r cump	
	Save Design		Switchin	ng Freg 300kHz 💌	Over Temp Shutdown (C) 155.0 🚔	*
	Save Design As		S	ystem Clock 38.4MHz / 128	Cver Temp Restart (C) 135.0 🚔	
-	Select Revision	_			Reset Chip on dearing of UVLO warning	
-				Wait!		×
	Board Search			Wart!		
	Export	•				
	Program NVM			💦 This chip H	ias already been programmed. NVM	is one time
	Exit		Channel 1	— 🚺 programm		
			Vin	L: Programm	ing this chip could cause unexpecte	ed results.
			Phase (deg)	Def		
			Tstart (ms)	2.		
			Rice (ms)			OK
			Harse (me)			
			DO HALLY (	0.4		
	Registers to	o ha D	PG delay (s)			
	Registers to	o be P	P3 delay (s) rogrammed			
		o be P New		1		
	Addr r 0x0A: 0	New 0x80	Current (0x00)	RegName SET I2C SLAVE ADDR		
	Addr r 0x0A: ( 0x0B: (	New	Current (0x00) (0x00)	RegName SET_I2C_SLAVE_ADDR SET_I2C_DISABLE		Ê
	Addr f 0x0A; ( 0x0B: ( 0x0D: ( 0x0D: ( 0x0E; (	New 0x80 0x00 0x04 0x04 0x00	rogrammed Current (0x00) (0x00) (0x00) (0x00)	RegName SET I2C SLAVE ADDR SET_I2C_DISABLE VERSION_BYTE GUI_VERSION_I I	Programming NVM?	
	Addr r 0x0A: ( 0x0B: ( 0x0D: ( 0x0C: ( 0x0E: (	New 0x80 0x00 0x04 0x00 0x64	rogrammed Current (0x00) (0x00) (0x00) (0x00) (0x00)	RegName SET I2C SLAVE ADDR SET_I2C_DISABLE VERSION_BYTE GUI_VERSION_I GUI_VERSION_L		
	Addr ( 0x0A: ( 0x0B: ( 0x0C: ( 0x0C: ( 0x0C: ( 0x0F: ( 0x18: (	New 0x80 0x00 0x04 0x04 0x00	rogrammed Current (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00)	RegName SET I2C SLAVE ADDR SET_I2C_DISABLE VERSION_BYTE GUI_VERSION_I I		
	Addr ( 0x0A; ( 0x0D; ( 0x0D; ( 0x0C; ( 0x0C; ( 0x18; ( 0x19; ( 0x14; (	New 0x80 0x00 0x04 0x00 0x64 0x1F 0x04 0x50	rogrammed Current (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00)	RegName SET I2C SLAVE ADDR SFT_I2C_DISABI F VERSION_BYTE GUI_VERSION_I I GUI_VERSION_I SET_COEFF_A_SS_LB_CI SET_COEFF_B_SS_LB_CA	You are about to pr	ogram the NVM!
	Addr ( 0x0A; ( 0x0B; ( 0x0C; ( 0x0C; ( 0x0F; ( 0x18; ( 0x19; ( 0x1A; ( 0x1B; ()	New 0x80 0x00 0x04 0x00 0x64 0x1F 0x1F 0x04	rogrammed Current (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00)	REGNAME SET I2C SLAVE ADDR SET_I2C_DISABLE VERSION_BYTE GUI_VERSION_L SET_COEFF_A_SS_HB_C SET_COEFF_B_SS_HB_C SET_COEFF_B_SS_HB_C	You are about to pr Are you sure you su	
	Addr ( 0x0A: ( 0x0B: ( 0x0D: ( 0x0C: ( 0x1A: ( 0x1A: ( 0x1B: ( 0x1A: ( 0x1B: ( 0x1C: ( 0x1D: ())))))))))))))))))))))))))))))))))))	New Dx80 Dx00 0x04 0x00 0x64 0x1F 0x04 0x50 0x07 0x3D 0x03	Current (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00)	RegName SET I2C SLAVE ADDR SET_I2C_DISABLE VERSION_BYTE GUI_VERSION_LI GUI_VERSION_LI SET_COEFF_A_SS_LB_CI SET_COEFF_A_SS_LB_CI SET_COEFF_C_SS_LB_CI SET_COEFF_C_SS_LB_CI SET_COEFF_C_SS_LB_CI SET_COEFF_C_SS_LB_CI	You are about to pr Are you sure you su	ogram the NVM!
	Addr 1 0x0A: ( 0x0B: ( 0x0D: ( 0x0C: ( 0x0C: ( 0x1B: ( 0x19: ( 0x1B: ( 0x1B: ( 0x1B: ( 0x1C: ( 0x1E: ()	New 0x80 0x00 0x04 0x00 0x64 0x1F 0x04 0x50 0x07 0x3D 0x07 0x3D 0x02	Current (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00)	REGNAME SET I2C SLAVE ADDR SET I2C DISABLE VERSION_BYTE GUI_VERSION_L SET_COEFF_A_SS_HB_C SET_COEFF_B_SS_HB_C SET_COEFF_B_SS_HB_C SET_COEFF_B_SS_HB_C SET_COEFF_C_SS_HB_C SET_COEFF_C_SS_HB_C SET_COEFF_D_SS_CH1	You are about to pr Are you sure you su	ogram the NVM!
	Addr 1 0x0A: 0 0x0B: 0 0x0C: 0 0x0F: 0 0x1B: 0 0x1B: 0 0x1B: 0 0x1B: 0 0x1C: 0 Ux1D: 0 0x1E: 0	New Dx80 Dx00 0x04 0x00 0x64 0x1F 0x04 0x50 0x07 0x3D 0x03	Current (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00) (0x00)	RegName SET I2C SLAVE ADDR SFT_I2C_DISABLE VERSION_BYTE GUI_VERSION_LI GUI_VERSION_LI SET_COEFF_A_SS_LB_CI SET_COEFF_A_SS_LB_CI SET_COEFF_C_SS_LB_CI SET_COEFF_C_SS_LB_CI SET_COEFF_C_SS_LB_CI SET_COEFF_C_SS_LB_CI	You are about to pr Are you sure you su	ogram the NVM!
	Addr         I           0x0A;         0           0x0B;         0           0x0D;         0           0x0D;         0           0x0F;         0           0x1B;         0           0x1B;         0           0x1B;         0           0x1B;         0           0x1B;         0           0x1C;         0           0x1C;         0           0x1D;         0           0x1E;         0           0x1E;         0           0x20;         0           0x21;         0	New 0x80 0x00 0x04 0x00 0x64 0x50 0x1F 0x04 0x50 0x07 0x30 0x07 0x30 0x00 0x07 0x30 0x00 0x0	Current (0x00)	RegName SET I2C SLAVE ADDR SET I2C SLAVE ADDR SET_C_DISABLE VERSION_I GUI_VERSION_I SET_COEFF_A_SS_HB_C SET_COEFF_B_SS_HB_C SET_COEFF_B_SS_HB_C SET_COEFF_C_SS_HB_C SET_COEFF_C_SS_HB_C SET_COEFF_D_SS_CHI SET_COEFF_D_SS_CHI SET_COEFF_CASS_CHI	You are about to pr Are you sure you su	ogram the NVM! re you want to do this?
	Addr         I           0x0A;         0           0x0B;         0           0x0D;         0           0x0D;         0           0x0F;         0           0x1B;         0           0x1B;         0           0x1B;         0           0x1B;         0           0x1B;         0           0x1C;         0           0x1C;         0           0x1D;         0           0x1E;         0           0x1E;         0           0x20;         0           0x21;         0	New 0x80 0x00 0x04 0x00 0x64 0x1F 0x04 0x50 0x07 0x07 0x30 0x07 0x00 0x07 0x00 0x00	Current (0x00)	RegName SET I2C SLAVE ADDR SET_I2C_DISABLE VERSION_BYTE GUI_VERSION_L SET_COEFF_A_SS_LB_CI SET_COEFF_A_SS_LB_CI SET_COEFF_B_SS_LB_CI SET_COEFF_C_SS_LB_CI SET_COEFF_C_SS_LB_CI SET_COEFF_C_SS_HB_CI SET_COEFF_C_SS_HB_CI SET_COEFF_C_SS_CHI SET_VOUT_TARGET_CHI	You are about to pr Are you sure you su	ogram the NVM! re you want to do this?
	Addr         I           0x0A;         0           0x0B;         0           0x0D;         0           0x0D;         0           0x0F;         0           0x1B;         0           0x1B;         0           0x1B;         0           0x1B;         0           0x1B;         0           0x1C;         0           0x1C;         0           0x1D;         0           0x1E;         0           0x1E;         0           0x20;         0           0x21;         0	New 0x80 0x00 0x04 0x00 0x64 0x50 0x1F 0x04 0x50 0x07 0x30 0x07 0x30 0x00 0x07 0x30 0x00 0x0	Current (0x00)	RegName SET I2C SLAVE ADDR SET I2C SLAVE ADDR SET_C_DISABLE VERSION_I GUI_VERSION_I SET_COEFF_A_SS_HB_C SET_COEFF_B_SS_HB_C SET_COEFF_B_SS_HB_C SET_COEFF_C_SS_HB_C SET_COEFF_C_SS_HB_C SET_COEFF_D_SS_CHI SET_COEFF_D_SS_CHI SET_COEFF_CASS_CHI	You are about to pr Are you sure you su	ogram the NVM! re you want to do this?

#### Peek / Poke:

In the **Debug** menu, the **Peek/Poke** feature is used to read and write register addresses directly. Selecting this option opens the Debug: Peek/Poke window as seen below. One can enter the register address after the '0x' and click **Read** or **Write** to manipulate the register content.

Peek / Poł	œ	
Register	0x	xrp7704 🔻
Data	0x	hex 🗸
Re	ad	Write

## **Design Explorer:**

In the **Debug** menu, the **Design Explorer** feature allows the user to view the contents of the configuration file. It shows all the components of the design contained in one place. Users cannot edit the information here; it is merely for informational purposes only.

Chip Cor	nfig				
Refresh		Кеу	Value	'Customer' :	
Register	s	Chip Customer ch1 components C Fet L Res_ratio User	1.0 •	{ 'Name':" 'Contact':" 'Timestamp': 'Wed, 07 Jul 2010 14:51:15 +0800' 'Comments':" 'Phone':" 'ProgramNumber':" 'PartNumber':" 'Email':"	
OA	80	SET I2C SLAV			
0B	00	SET_I2C_DISABLE			
OD	04	VERSION_BYTE			
0E	00	GUI_VERSION_H			
OF	64	GUI_VERSION_L			
18	1F	SET_COEFF_A_SS_LB_CH1			
19	04	SET_COEFF_A_SS_HB_CH1			
1A	50	SET_COEFF_B_SS_LB_CH1			
1B	07	SET_COEFF_B_SS_HB_CH1			
1C	3D	SET_COEFF_C_SS	LB_CH1		-
		Generate By	tes Prog	ram Chip	

## **Customer Support:**

Should you need additional support, please contact your local Application Engineer or send an email to powerxr@exar.com.