

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

March 2007 Rev 2.0.0

GENERAL DESCRIPTION

The XRT94L33 is a highly integrated SONET/SDH terminator designed for E3/DS3/STS-1 mapping/de-mapping functions from either the STS-3 or STM-1 data stream. The XRT94L33 interfaces directly to the optical transceiver

The XRT94L33 processes the section, line and path overhead in the SONET/SDH data stream and also performs ATM and PPP PHY-layer processing. The processing of path overhead bytes within the STS-1s or TUG-3s includes 64 bytes for storing the J1 bytes. Path overhead bytes can be accessed through the microprocessor interface or via serial interface.

The XRT94L33 uses the internal E3/DS3 De-Synchronizer circuit with an internal pointer leak algorithm for clock smoothing as well as to remove the jitter due to mapping and pointer movements. These De-Synchronizer circuits do not need any external clock reference for its operation.

The SONET/SDH transmit blocks allow flexible insertion of TOH and POH bytes through both Hardware and Software. Individual POH bytes for the transmitted SONET/SDH signal are mapped either from the XRT94L33 memory map or from external interface. A1, A2 framing pattern, C1 byte and H1, H2 pointer byte are generated.

The SONET/SDH receive blocks receive SONET STS-3 signal or SDH STM-1 signal and perform the necessary transport and path overhead processing.

The XRT94L33 provides a line side APS (Automatic Protection Switching) interface by offering redundant receive serial interface to be switched at the frame boundary.

The XRT94L33 provides 3 Mappers for performing STS-1/VC-3 to STS-1/DS3/E3 mapping function, one for each STS-1/DS3/E3 framers.

A PRBS test pattern generation and detection is implemented to measure the bit-error performance.

A general-purpose microprocessor interface is included for control, configuration and monitoring.

APPLICATIONS

- Network switches
- Add/Drop Multiplexer
- W-DCS Digital Cross Connect Systems

FEATURES

- Provides DS3/ E3 mapping/de-mapping for up to 3 tributaries through SONET STS-1 or SDH AU-3 and/or TUG-3/AU-4 containers
- Generates and terminates SONET/SDH section, line and path layers
- Integrated SERDES with Clock Recovery Circuit
- Provides SONET frame scrambling and descrambling
- Integrated Clock Synthesizer that generates 155 MHz and 77.76 MHz clock from an external 12.96/19.44/77.76 MHz reference clock
- Integrated 3 E3/DS3/STS-1 De-Synchronizer circuit that de-jitter gapped clock to meet 0.05Ulpp jitter requirements
- Access to Line or Section DCC
- Level 2 Performance Monitoring for E3 and DS3
- Supports mixing of STS-1E and DS3 or E3 and DS3 tributaries
- OTOPIA Level 2 interface for ATM or level 2P for Packets
- E3 and DS3 framers for both Transmit and Receive directions
- Complete Transport/Section Overhead Processing and generation per Telcordia and ITU standards
- Single PHY and Multi-PHY operations supported
- Full line APS support for redundancy applications
- Loopback support for both SONET/SDH as well as E3/DS3/STS-1
- Boundary scan capability with JTAG IEEE 1149
- 8-bit microprocessor interface
- 3.3 V ± 5% Power Supply; 5 V input signal tolerance
- -40°C to +85°C Operating Temperature Range

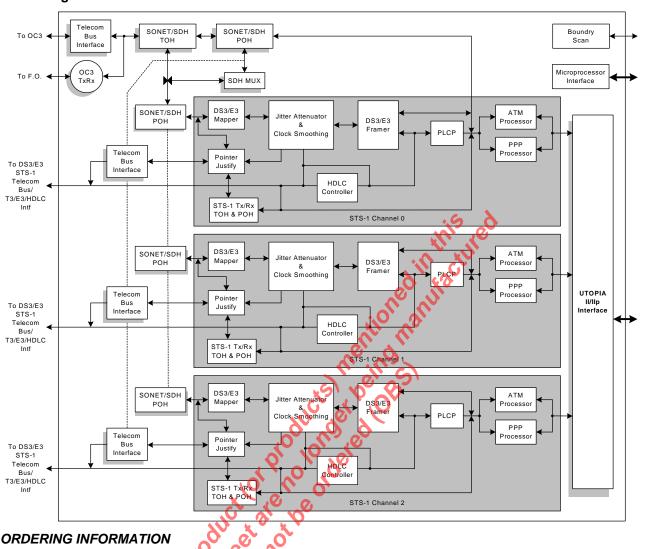
Available in a 504 Ball TBGA package



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Block Diagram of the XRT94L33



PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT94L33IB	27 x 27 504 Lead TBGA	-40°C to +85°C

1.0 XRT94L33 REGISTERS FOR SONET ATM/PPP APPLICATIONS

1.1 THE OVERALL REGISTER MAP WITHIN THE XRT94L33

The XRT94L33 employs a direct Addressing Scheme. The Address Locations for each of the "Register Groups" (or Register pages) is presented in the Table below.

Table 1: The Address Register Map for the XRT94L33

Address Location	REGISTER NAME	DEFAULT VALUE
	OPERATION CONTROL BLOCK REGISTERS	
0x0000 – 0x00FF	Reserved	
0x0100	Operation Control Register – Byte 3	0x00
0x0101	Operation Control Register – Byte 2	0x00

0x0102	Reserved	0x00
0x0103	Operation Control Register – Byte 0	0x00
0x0104	Operation Status Register – Byte 3 (Device ID)	0xE3
0x0105	Operation Status Register – Byte 2 (Revision ID)	0x01
0x0106 – 0x010A	Reserved	0x00
0x010B	Operation Interrupt Status Register – Byte 0	0x00
0x010C - 0x010E	Reserved	0x00
0x010F	Operation Interrupt Enable Register – Byte 0	0x00
0x0110 – 0x0111	Reserved	0x00
0x0112	Operation Block Interrupt Status Register – Byte 1	0x00
0x0113	Operation Block Interrupt Status Register – Byte 0	0x00
0x0114 – 0x0115	Reserved	0x00
0x0116	Operation Block Interrupt Enable Register - Byte 1	0x00
0x0117	Operation Block Interrupt Enable Register Byte 0	0x00
0x0118 – 0x0119	Reserved	0x00
0x011A	Reserved	0x00
0x011B	Mode Control Register – Byte 0	0x00
0x011C - 0x011E	Reserved	0x00
0x011F	Loop-back Control Register - Byte 0	0x00
0x0120	Channel Interrupt Indicator – Receive SONET POH Processor Block	0x00
0x0121	Reserved	0x00
0x0122	Channel Interrupt Indicator – DS3/E3 framer Block	0x00
0x0123	Channel Interrupt Indicator – Receive STS-1 POH Processor Block	0x00
0x0124	Channel Interrupt Indicator – Receive STS-1 TOH Processor Block	0x00
0x0125	Reserved 0	0x00
0x0126	Channel Interrupt Indicator – STS-1/DS3/E3 Mapper Block	0x00
0x0127	Reserved	0x00
0x0128	Reserved	0x00
0x0129	Reserved	0x00
0x012A – 0x012F	Reserved	0x00
0x0130	Reserved	0x11
0x0131	Reserved	0x00
0x0132	Interface Control Register – Byte 1	0x00



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

0x0133	Interface Control Register – Byte 0	0x00
0x0134	STS-3/STM-1 Telecom Bus Control Register – Byte 3	0x00
0x0135	STS-3/STM-1 Telecom Bus Control Register – Byte 2	0x00
0x0136	Reserved	0x00
0x0137	STS-3/STM-1 Telecom Bus Control Register – Byte 0	0x00
0x0138	Reserved	0x00
0x0139	Interface Control Register – Byte 2 – STS-3 Telecom Bus 2	0x00
0x013A	Interface Control Register – Byte 1 – STS-3 Telecom Bus 1	0x00
0x013B	Interface Control Register – Byte 0 – STS-3 Telecom Bus 0	0x00
0x013C	Interface Control Register – STS-1 Telecom Bus Interrupt Register	0x00
0x013D	Interface Control Register – STS-1 Telecom Bus Interrupt Status Register	0x00
0x013E	Interface Control Register – STS-1 Telecom Bus Interrupt Register # 2	0x00
0x013F	Interface Control Register – STS-1 Telecom Bus Interrupt Enable Register	0x00
0x0140 - 0x0146	Reserved	0x00
0x0147	Operation General Purpose Input/Output Register	0x00
0x0148 - 0x0149	Reserved	0x00
0x014A	Reserved	0x00
0x014B	Operation General Purpose Input/Output Direction Register – Byte 0	0x00
0x014C -0x014E	Reserved	0x00
0x014F	Reserved	0x00
0x0150	Operation Output Control Register – Byte 1	0x00
0x0151 -0x0152	Reserved	0x00
0x0153	Operation Output Control Register – Byte 0	0x00
0x0154	Operation Slow Speed Port Control Register – Byte 1	0x00
0x0155 – 0x0156	Reserved	0x00
0x0157	Operation Slow Speed Port Control Register –Byte 0	0x00
0x0158	Operation – DS3/E3/STS-1 Clock Frequency Out of Range Detection – Direction Register	0x00
0x0159	Reserved	0x00
0x015A	Operation – DS3/E3/STS-1 Clock Frequency – DS3 Out of Range Detection Threshold Register	0x00
0x015B	Operation – DS3/E3/STS-1 Clock Frequency – STS-1/E3 Out of Range Detection Threshold Register	0x00
0x015C	Reserved	0x00
0x015D	Operation – DS3/E3/STS-1 Frequency Out of Range Interrupt Enable Register	0x00

	- Byte 0	
0x015E	Reserved	0x00
0x015F	Operation – DS3/E3/STS-1 Frequency Out of Range Interrupt Status Register – Byte 0	0x00
0x0160 – 0x017F	Reserved	0x00
0x0180	APS Mapping Register	0x00
0x0181	APS Control Register	0x00
0x0182 – 0x0193	Reserved	0x00
0x0194	APS Status Register	0x00
0x0195	Reserved	0x00
0x0196	APS Status Register	0x00
0x0197	APS Status Register	0x00
0x0198	APS Interrupt Register	0x00
0x0199	Reserved	0x00
0x019A	APS Interrupt Register	0x00
0x019B	APS Interrupt Register	0x00
0x019C	APS Interrupt Register	0x00
0x019D	Reserved	0x00
0x019E	APS Interrupt Enable Register	0x00
0x019F	APS Interrupt Enable Register	0x00
0x01A0 – 0x01FF	Reserved	0x00
	LINE INTERFACE CONTROL REGISTERS	
0x0302	Receive Line Interface Control Register – Byte 1	0x00
0x0303	Receive Line Interface Control Register – Byte 0	0x00
0x0304 – 0x0306	Reserved	0x00
0x0307	Receive Line Status Register	0x00
0x0308 -0x030A	Reserved	0x00
0x030B	Receive Line Interrupt Register	0x00
0x030C - 0x030E	Reserved	0x00
0x030F	Receive Line Interrupt Enable Register	0x00
0x0310 – 0x0382	Reserved	0x00
0x0383	Transmit Line Interface Control Register	0x00
	RECEIVE/TRANSMIT UTOPIA INTERFACE REGISTERS	
0x0384 - 0x0502	Reserved	0x00



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

0x0503	Receive UTOPIA Control Register – Byte 0	0x8F
0x0504 - 0x0512	Reserved	0x00
0x0513	Receive UTOPIA Port Address	0x00
0x0514 - 0x0516	Reserved	0x00
0x0517	Receive UTOPIA Port Number	0x00
0x0518 - 0x0582	Reserved	0x00
0x0583	Transmit UTOPIA Control Register – Byte 0	0x8F
0x0584 - 0x0592	Reserved	0x00
0x0593	Transmit UTOPIA Port Address	0x00
0x0594 – 0x0596	Reserved	0x00
0x0597	Transmit UTOPIA Port Number	0x00
0x0598 - 0x1102	Reserved	0x00
	RECEIVE STS-3 TOH PROCESSOR BLOCK CONTROL REGISTERS	•
0x1103	Receive STS-3 Transport Control Register – Byte 0	0x00
0x1104 – 0x1105	Reserved	0x00
0x1106	Receive STS-3 Transport Status Register – Byte 1	0x00
0x1107	Receive STS-3 Transport Status Register Byte 0	0x02
0x1108	Reserved	0x00
0x1109	Receive STS-3 Transport Interrupt Status Register – Byte 2	0x00
0x110A	Receive STS-3 Transport Interrupt Status Register – Byte 1	0x00
0x110B	Receive STS-3 Transport Interrupt Status Register – Byte 0	0x00
0x110C	Reserved	0x00
0x110D	Receive STS-3 Transport Interrupt Enable Register – Byte 2	0x00
0x110E	Receive STS-3 Fransport Interrupt Enable Register – Byte 1	0x00
0x110F	Receive STS-3 Transport Interrupt Enable Register – Byte 0	0x00
0x1110	Receive STS-3 Transport B1 Error Count – Byte 3	0x00
0x1111	Receive STS-3 Transport B1 Error Count – Byte 2	0x00
0x1112	Receive STS-3 Transport B1 Error Count – Byte 1	0x00
0x1113	Receive STS-3 Transport B1 Error Count – Byte 0	0x00
0x1114	Receive STS-3 Transport B2 Error Count – Byte 3	0x00
0x1115	Receive STS-3 Transport B2 Error Count – Byte 2	0x00
0x1116	Receive STS-3 Transport B2 Error Count – Byte 1	0x00
0x1117	Receive STS-3 Transport B2 Error Count – Byte 0	0x00

0x1118	Receive STS-3 Transport REI-L Error Count – Byte 3	0x00
0x1119	Receive STS-3 Transport REI-L Error Count – Byte 2	0x00
0x111A	Receive STS-3 Transport REI-L Error Count – Byte 1	0x00
0x111B	Receive STS-3 Transport REI-L Error Count – Byte 0	0x00
0x111C	Reserved	0x00
0x111D - 0 x111E	Reserved	0x00
0x111F	Receive STS-3 Transport K1 Byte Value	0x00
0x1120 - 0x1122	Reserved	0x00
0x1123	Receive STS-3 Transport K2 Byte Value	0x00
0x1124 - 0x1126	Reserved	0x00
0x1127	Receive STS-3 Transport S1 Byte Value	0x00
0x1128 - 0x112A	Reserved	0x00
0x112B	Receive STS-3 Transport – In-Sync Threshold Value	0x00
0x112C, 0x112D	Reserved	0x00
0x112E	Receive STS-3 Transport – LOS Threshold Value – MSB	0xFF
0x112F	Receive STS-3 Transport – LOS Threshold Value – LSB	0xFF
0x1130	Reserved	0x00
0x1131	Receive STS-3 Transport - SF Set Monitor Interval - Byte 2	0x00
0x1132	Receive STS-3 Transport – SP Set Monitor Interval – Byte 1	0x00
0x1133	Receive STS-3 Transport - SF Set Monitor Interval – Byte 0	0x00
0x1134 – 0x1135	Reserved	0x00
0x1136	Receive STS-3 Transport – SF Set Threshold – Byte 1	0x00
0x1137	Receive STS-3 Transport – SF Set Threshold – Byte 0	0x00
0x1138, 0x1139	Reserved	0x00
0x113A	Receive STS 3 Transport – SF Clear Threshold – Byte 1	0x00
0x113B	Receive STS-3 Transport – SF Clear Threshold – Byte 0	0x00
0x113C	Reserved	0x00
0x113D	Receive STS-3 Transport – SD Set Monitor Interval – Byte 2	0x00
0x113E	Receive STS-3 Transport – SD Set Monitor Interval – Byte 1	0x00
0x113F	Receive STS-3 Transport – SD Set Monitor Interval – Byte 0	0x00
0x1140, 0x1141	Reserved	0x00
0x1142	Receive STS-3 Transport – SD Set Threshold – Byte 1	0x00
0x1143	Receive STS-3 Transport – SD Set Threshold – Byte 0	0x00





0x1144, 0x1145	Reserved	0x00
0x1146	Receive STS-3 Transport – SD Clear Threshold – Byte 1	0x00
0x1147	Receive STS-3 Transport – SD Clear Threshold – Byte 0	0x00
0x1148 – 0x114A		
	Reserved	0x00
0x114B	Receive STS-3 Transport – Force SEF Condition	0x00
0x114C, 0x114E	Reserved	0x00
0x114F	Receive STS-3 Transport – Receive J0 Trace Buffer Control	0x00
0x1150, 0x1151	Reserved	0x00
0x1152	Receive STS-3 Transport – SD Burst Error Count Tolerance – Byte 1	0x00
0x1153	Receive STS-3 Transport – SD Burst Error Count Tolerance Byte 6	0x00
0x1154, 0x1155	Reserved	0x00
0x1156	Receive STS-3 Transport – SF Burst Error Count Tolerance - Byte 1	0x00
0x1157	Receive STS-3 Transport – SF Burst Error Count Tolerance – Byte 0	0x00
0x1158	Reserved	0x00
0x1159	Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 2	0xFF
0x115A	Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 1	0xFF
0x115B	Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 0	0xFF
0x115C	Reserved	0x00
0x115D	Receive STS-3 Transport - Receive SF Clear Monitor Interval – Byte 2	0xFF
0x115E	Receive STS-3 Transport – Receive SF Clear Monitor Interval – Byte 1	0xFF
0x115F	Receive STS-3 Transport - Receive SF Clear Monitor - Byte 0	0xFF
0x1160 - 0x1162	Reserved	0x00
0x1163	Receive STS-3 Transport - Auto AIS Control Register	0x00
0x1164 - 0x1166	Reserved	0x00
0x1167	Receive STS-3 Transport – Serial Port Control Register	0x00
0x1168 – 0x116A	Reserved	0x00
0x116B	Receive STS-3 Transport – Auto AIS (in Downstream STS-1s) Control Register	0x000
0x116C - 0x1179	Reserved	0x00
0x117A	Receive STS-3 Transport – TOH Capture Indirect Address	0x00
0x117B	Receive STS-3 Transport – TOH Capture Indirect Address	0x00
0x117C	Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x117D	Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x117E	Receive STS-3 Transport – TOH Capture Indirect Data	0x00

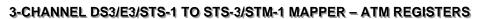
0x117F	Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x1180 - 0x11FF	Reserved	0x00
Receiv	E STS-3/STM-1 TOH PROCESSOR BLOCK - RECEIVE JO (SECTION) TRACE MESSAGE BU	JFFER
0x1300 – 0x133F	Receive STS-3/STM-1 TOH Processor Block – Receive J0 (Section) Trace Message Buffer – Expected and Received	0x00
0x1340 – 0x13FF	Reserved	0x00
	TRANSMIT STS-3 TOH PROCESSOR BLOCK CONTROL REGISTERS	
0x1800 - 0x1901	Reserved	0x00
0x1902	Transmit STS-3 Transport – SONET Transmit Control Register – Byte 1	0x00
0x1903	Transmit STS-1 Transport – SONET Transmit Control Register – Byte 0	0x00
0x1904 – 0x1915	Reserved	0x00
0x1916	Reserved	0x00
0x1917	Transmit STS-3 Transport – Transmit A1 Error Mask – Low Register – Byte 0	0x00
0x1918 – 0x191D	Reserved	0x00
0x191E	Reserved	0x00
0x191F	Transmit STS-3 Transport – Transmit A2 Error Mask – Low Register – Byte 0	0x00
0x1920 - 0x1921	Reserved	0x00
0x1923	Transmit STS-3 Transport – B1 Byte Error Mask Register	0x00
0x1924 - 0x1925	Reserved	0x00
0x1926	Reserved	0x00
0x1927	Transmit STS-3 Transport – Transmit B2 Byte Error Mask Register – Byte 0	0x00
0x1928 – 0x192A	Reserved	0x00
0x192B	Transmit STS-3 Transport – Transmit B2 Bit Error Mask Register – Byte 0	0x00
0x192C - 0x192D	Reserved	0x00
0x192E	Transmit STS-3 Transport – K1K2 (APS) Value Register – Byte 1	0x00
0x192F	Transmit STS-3 Transport – K1K2 (APS) Value Register – Byte 0	0x00
0x1930 – 0x1931	Reserved	0x00
0x1933	Transmit STS-3 Transport – RDI-L Control Register	0x00
0x1934 – 0x1936	Reserved	0x00
0x1937	Transmit STS-3 Transport – M0M1 Byte Value Register	0x00
0x1938 – 0x193A	Reserved	0x00
0x193B	Transmit STS-3 Transport – S1 Byte Value Register	0x00
0x193C - 0x193E	Reserved	0x00
0x193F	Transmit STS-3 Transport – F1 Byte Value Register	0x00



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

0x1940 - 0x1942	Reserved	0x00
0x1943	Transmit STS-3 Transport – E1 Byte Value Register	0x00
0x1944	Reserved	0x00
0x1945	Reserved	0x00
0x1946	Reserved	0x00
0x1947	Transmit STS-3 Transport – E2 Byte Value Register	0x00
0x1948 – 0x194A	Reserved	0x00
0x194B	Transmit STS-3 Transport – J0 Byte Value Register	0x00
0x194C - 0x194E	Reserved	0x00
0x194F	Transmit STS-3 Transport – J0 Byte Control Register	0x00
0x1950 - 0x1952	Reserved	0x00
0x1953	Transmit STS-3 Transport – Serial Port Control Register	0x00
0x1954 -0x19FF	Reserved	0x00
TRAN	ISMIT STS-3 TOH PROCESSOR BLOCK – TRANSMIT 0 (SECTION) TRACE MESSAGE BUFI	FER
0x1B00 – 0x1B3F	Transmit STS-3 TOH Processor Block – Transmit J0 (Section) Trace Message Buffer	0x00
0x1B40 - 0x1BFF	Reserved	0x00
	REDUNDANT RECEIVE STS-3 TOH PROCESSOR BLOCK CONTROL REGISTERS	
0x1600 - 0x1702	Reserved	
0x1703	Redundant Receive STS-3 Transport Control Register – Byte 0	0x00
0x1704 – 0x1705	Reserved	0x00
0x1706	Redundant Receive STS 3 Transport Status Register – Byte 1	0x00
0x1707	Redundant Receive STS-3 Transport Status Register – Byte 0	0x02
0x1708	Reserved (2)	0x00
0x1709	Redundant Receive STS-3 Transport Interrupt Status Register – Byte 2	0x00
0x170A	Redundant Receive STS-3 Transport Interrupt Status Register – Byte 1	0x00
0x170B	Redundant Receive STS-3 Transport Interrupt Status Register – Byte 0	0x00
0x170C	Reserved	0x00
0x170D	Redundant Receive STS-3 Transport Interrupt Enable Register – Byte 2	0x00
0x170E	Redundant Receive STS-3 Transport Interrupt Enable Register – Byte 1	0x00
0x170F	Redundant Receive STS-3 Transport Interrupt Enable Register – Byte 0	0x00
0x1710	Redundant Receive STS-3 Transport B1 Error Count – Byte 3	0x00
0x1711	Redundant Receive STS-3 Transport B1 Error Count – Byte 2	0x00
0x1712	Redundant Receive STS-3 Transport B1 Error Count – Byte 1	0x00

0x1713	Redundant Receive STS-3 Transport B1 Error Count – Byte 0	0x00
0x1714	Redundant Receive STS-3 Transport B2 Error Count – Byte 3	0x00
0x1715	Redundant Receive STS-3 Transport B2 Error Count – Byte 2	0x00
0x1716	Redundant Receive STS-3 Transport B2 Error Count – Byte 1	0x00
0x1717	Redundant Receive STS-3 Transport B2 Error Count – Byte 0	0x00
0x1718	Redundant Receive STS-3 Transport REI-L Error Count – Byte 3	0x00
0x1719	Redundant Receive STS-3 Transport REI-L Error Count – Byte 2	0x00
0x171A	Redundant Receive STS-3 Transport REI-L Error Count – Byte 1	0x00
0x171B	Redundant Receive STS-3 Transport REI-L Error Count – Byte 0	0x00
0x171C	Reserved	0x00
0x171D - 0 x171E	Reserved	0x00
0x171F	Redundant Receive STS-3 Transport K1 Value	0x00
0x1720 - 0x1722	Reserved	0x00
0x1723	Redundant Receive STS-3 Transport K2 Value	0x00
0x1724 - 0x1726	Reserved	0x00
0x1727	Redundant Receive STS-3 Transport S1 Value	0x00
0x1728 – 0x172A	Reserved	0x00
0x172B	Redundant Receive STS-3 Transport - In-Sync Threshold Value	0x00
0x172C, 0x172D	Reserved	0x00
0x172E	Redundant Receive STS3 Transport – LOS Threshold Value – MSB	0xFF
0x172F	Redundant Receive STS-3 Transport – LOS Threshold Value – LSB	0xFF
0x1730	Reserved	0x00
0x1731	Redundant Receive STS-3 Transport – SF Set Monitor Interval – Byte 2	0x00
0x1732	Redundant Receive STS-3 Transport – SF Set Monitor Interval – Byte 1	0x00
0x1733	Redundant Receive STS-3 Transport – SF Set Monitor Interval – Byte 0	0x00
0x1734 - 0x1735	Reserved	0x00
0x1736	Redundant Receive STS-3 Transport – SF Set Threshold – Byte 1	0x00
0x1737	Redundant Receive STS-3 Transport – SF Set Threshold – Byte 0	0x00
0x1738, 0x1739	Reserved	0x00
0x173A	Redundant Receive STS-3 Transport – SF Clear Threshold – Byte 1	0x00
0x173B	Redundant Receive STS-3 Transport – SF Clear Threshold – Byte 0	0x00
0x173C	Reserved	0x00
0x173D	Redundant Receive STS-3 Transport – SD Set Monitor Interval – Byte 2	0x00





0x173E	Redundant Receive STS-3 Transport – SD Set Monitor Interval – Byte 1	0x00
0x173F	Redundant Receive STS-3 Transport – SD Set Monitor Interval – Byte 0	0x00
0x1740, 0x1741	Reserved	0x00
0x1742	Redundant Receive STS-3 Transport – SD Set Threshold – Byte 1	0x00
0x1743	Redundant Receive STS-3 Transport – SD Set Threshold – Byte 0	0x00
0x1744, 0x1745	Reserved	0x00
0x1746	Redundant Receive STS-3 Transport – SD Clear Threshold – Byte 1	0x00
0x1747	Redundant Receive STS-3 Transport – SD Clear Threshold – Byte 0	0x00
0x1748 – 0x174A	Reserved	0x00
0x174B	Redundant Receive STS-3 Transport – Force SEF Condition	0x00
0x174C, 0x174E	Reserved	0x00
0x174F	Redundant Receive STS-3 Transport – Receive J0 Trace Buffer Control	0x00
0x1750, 0x1751	Reserved	0x00
0x1752	Redundant Receive STS-3 Transport – SD Burst Error Count Tolerance – Byte 1	0x00
0x1753	Redundant Receive STS-3 Transport - SD Burst Error Count Tolerance - Byte 0	0x00
0x1754, 0x1755	Reserved	0x00
0x1756	Redundant Receive STS-3 Transport - SF Burst Error Count Tolerance - Byte 1	0x00
0x1757	Redundant Receive STS-3 Transport SF Burst Error Count Tolerance – Byte 0	0x00
0x1758	Reserved	0x00
0x1759	Redundant Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 2	0xFF
0x175A	Redundant Receive STS-3 Transport - Receive SD Clear Monitor Interval - Byte 1	0xFF
0x175B	Redundant Receive STS-3 Transport - Receive SD Clear Monitor Interval - Byte 0	0xFF
0x175C	Reserved	0x00
0x175D	Redundant Receive STS-3 Transport – Receive SF Clear Monitor Interval – Byte 2	0xFF
0x175E	Redundant Receive STS-3 Transport – Receive SF Clear Monitor Interval – Byte 1	0xFF
0x175F	Redundant Receive STS-3 Transport – Receive SF Clear Monitor – Byte 0	0xFF
0x1760 - 0x1762	Reserved	0x00
0x1763	Redundant Receive STS-3 Transport – Auto AIS Control Register	0x00

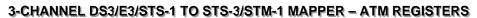
0x1764 – 0x1766	Reserved	0x00
0x1767	Redundant Receive STS-3 Transport – Serial Port Control Register	0x00
0x1768 – 0x176A	Reserved	0x00
0x176B	Redundant Receive STS-3 Transport – Auto AIS (in Downstream STS-1s) Control Register	0x000
0x176C - 0x1779	Reserved	0x00
0x177A	Redundant Receive STS-3 Transport – TOH Capture Indirect Address	0x00
0x177B	Redundant Receive STS-3 Transport – TOH Capture Indirect Address	0x00
0x177C	Redundant Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x177D	Redundant Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x177E	Redundant Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x177F	Redundant Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x1780 – 0x17FF	Reserved	0x00
	RECEIVE SONET POH PROCESSOR BLOCK CONTROL REGISTERS	
Note: N represen	ts the "Channel Number" and ranges in value from 0x02 to 0x04	
0xN000 – 0xN181	Reserved	0x00
0xN182	Receive SONET Path – Control Register – Byte 1	0x00
0xN183	Receive SONET Path – Control Register – Byte 0	0x00
0xN184, 0xN185	Reserved	0x00
0xN186	Receive SONET Path - Status Register - Byte 1	0x00
0xN187	Receive SONET Path Status Register – Byte 0	0x00
0xN188	Reserved	0x00
0xN189	Receive SONET Path - Interrupt Status Register - Byte 2	0x00
0xN18A	Receive SONET Path – Interrupt Status Register – Byte 1	0x00
0xN18B	Receive SONET Path – Interrupt Status Register – Byte 0	0x00
0xN18C	Reserved	0x00
0xN18D	Receive SONET Path – Interrupt Enable Register – Byte 2	0x00
0xN18E	Receive SONET Path – Interrupt Enable Register – Byte 1	0x00
0xN18F	Receive SONET Path – Interrupt Enable Register – Byte 0	0x00
0xN190 – 0xN192	Reserved	0x00
0xN193	Receive SONET Path – SONET Receive RDI-P Register	0x00
0xN194, 0xN195	Reserved	0x00
0xN196	Receive SONET Path – Received Path Label Register	0x00

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS



0xN198	Receive SONET Path – B3 Error Count Register – Byte 3	0x00
0xN199	Receive SONET Path – B3 Error Count Register – Byte 2	0x00
0xN19A	Receive SONET Path – B3 Error Count Register – Byte 1	0x00
0xN19B	Receive SONET Path – B3 Error Count Register – Byte 0	0x00
0xN19C	Receive SONET Path – REI-P Error Count Register – Byte 3	0x00
0xN19D	Receive SONET Path – REI-P Error Count Register – Byte 2	0x00
0xN19E	Receive SONET Path – REI-P Error Count Register – Byte 1	0x00
0xN19F	Receive SONET Path – REI-P Error Count Register – Byte 0	0x00
0xN1A0 - 0xN1A2	Reserved	0x00
0xN1A3	Receive SONET Path – Receiver J1 Control Register	0x00
0xN1A4, 0xN1A5	Reserved	
0xN1A6	Receive SONET Path – Pointer Value – Byte 1	0x00
0xN1A7	Receive SONET Path – Pointer Value – Byte 0	0x00
0xN1A8 – 0xN1AA	Reserved	0x00
0xN1AB	Receive SONET Path – Loss of Pointer – Concatenation Status Register	0x00
0xN1AC - 0xN1B2	Reserved	0x00
0xN1B3	Receive SONET Path – AIS - Concatenation Status Register	0x00
0xN1B4 - 0xN1BA	Reserved	0x00
0xN1BB	Receive SONET Path - AUTO Als Control Register	0x00
0xN1BC – 0xN1BE	Reserved	0x00
0xN1BF	Receive SONET Path Serial Port Control Register	0x00
0xN1C0 - 0xN1C2	Reserved	0x00
0xN1C3	Receive SONET Path SONET Receive Auto Alarm Register – Byte 0	0x00
0xN1C4 - 0xN1D2	Reserved	0x00
0xN1D3	Receive SONET Path – Receive J1 Capture Register	0x00
0xN1D4 – 0xN1D6	Reserved	0x00
0xN1D7	Receive SONET Path – Receive B3 Capture Register	0x00
0xN1D8 – 0xN1DA	Reserved	0x00
0xN1DB	Receive SONET Path – Receive C2 Capture Register	0x00
0xN1DC – 0xN1DE	Reserved	0x00
0xN1DF	Receive SONET Path – Receive G1 Byte Capture Register	0x00
0xN1E0 - 0xN1E2	Reserved	0x00

0xN1E3	Receive SONET Path – Receive F2 Byte Capture Register	0x00
0xN1E4 – 0xN1E6	Reserved	0x00
0xN1E7	Receive SONET Path – Receive H4 Byte Capture Register	0x00
)xN1E8 – 0xN1EA	Reserved	0x00
0xN1EB	Receive SONET Path – Receive Z3 Byte Capture Register	0x00
0xN1EC – 0xN1EE	Reserved	0x00
0xN1EF	Receive SONET Path – Receive Z4 (K3) Byte Capture Register	0x00
0xN1F0 – 0xN1F2	Reserved	0x00
0xN1F3	Receive SONET Path – Receive Z5 Byte Capture Register	0x00
0xN1F4 – 0xN1FF	Reserved	
F	RECEIVE SONET POH PROCESSOR BLOCK – RECEIVE J1 (PATH) TRACE MESSAGE BUFFE	R
Note: N repres	ents the "Channel Number" and ranges in value from 0x02 to 0x04	
0xN500 – 0xN53F	Receive SONET POH Processor Block – Receive 11 (Path) Trace Message	0x00
	Buffer – Expected and Received	
0xN540 – 0xN5FF	Reserved Receive ATM Cell Processor/ PPP Cell Processor Block Control Registers	0x00
	Reserved Receive ATM Cell Processor/ PPP Cell Processor Block Control Registers	0x00
	Buffer – Expected and Received Reserved	0x00 0x00
Note: N represe	Reserved Receive ATM Cell Processor/ PPP Cell Processor Block Control Registers ents the "Channel Number" and ranges in value from 0x02 to 0x04	
Note: N represe	Reserved Receive ATM Cell Processor/ PPP Cell Processor Block Control Registers and the "Channel Number" and ranges in value from 0x02 to 0x04 Receive ATM Control – Receive ATM Control Register - Byte 3	0x00
Vote: N represe 0xN700 0xN701	Reserved Receive ATM Cell Processor/ PPP Cell Processor Block Control Registers and ranges in value from 0x02 to 0x04 Receive ATM Control – Receive ATM Control Register - Byte 3 Receive ATM Control – Receive ATM Control Register – Byte 2	0x00 0x00
0xN700 0xN701 0xN702	Reserved Receive ATM Cell Processor/ PPP Cell Processor Block Control Registers and the "Channel Number" and ranges in value from 0x02 to 0x04 Receive ATM Control – Receive ATM Control Register - Byte 3 Receive ATM Control – Receive ATM Control Register – Byte 2 Receive ATM Control – Receive ATM Control Register – Byte 1	0x00 0x00 0x00
0xN700 0xN701 0xN702 0xN703 0xN704 –	Reserved Receive ATM Cell Processor/ PPP Cell Processor Block Control Registers and the "Channel Number" and ranges in value from 0x02 to 0x04 Receive ATM Control – Receive ATM Control Register - Byte 3 Receive ATM Control – Receive ATM Control Register - Byte 2 Receive ATM Control – Receive ATM Control Register - Byte 1 Receive ATM Cell/PPP Control – Receive ATM Control Register - Byte 0	0x00 0x00 0x00 0x00
0xN700 0xN701 0xN702 0xN703 0xN704 – 0xN706	Reserved Receive ATM Cell Processor/ PPP Cell Processor Block Control Registers and state "Channel Number" and ranges in value from 0x02 to 0x04 Receive ATM Control – Receive ATM Control Register - Byte 3 Receive ATM Control – Receive ATM Control Register – Byte 2 Receive ATM Control – Receive ATM Control Register – Byte 1 Receive ATM Cell/PPP Control – Receive ATM Control Register – Byte 0 Reserved	0x00 0x00 0x00 0x00 0x00
0xN700 0xN701 0xN702 0xN703 0xN704 - 0xN706 0xN707	Receive ATM Control Receive ATM Control Register - Byte 1 Receive ATM Control Receive ATM Control Register - Byte 1 Receive ATM Control Receive ATM Control Register - Byte 1 Receive ATM Control Receive ATM Control Register - Byte 1 Receive ATM Control Receive ATM Control Register - Byte 1 Receive ATM Control Receive ATM Control Register - Byte 0 Reserved Receive ATM Status Register- Channel 0	0x00 0x00 0x00 0x00 0x00
0xN700 0xN701 0xN702 0xN703 0xN704 - 0xN706 0xN707	Receive ATM Control Receive ATM Control Register - Byte 2 Receive ATM Control Receive ATM Control Register - Byte 1 Receive ATM Control Receive ATM Control Register - Byte 1 Receive ATM Control Receive ATM Control Register - Byte 1 Receive ATM Control Receive ATM Control Register - Byte 0 Receive ATM Control Receive ATM Control Register - Byte 0 Receive ATM Control Receive ATM Control Register - Byte 0 Reserved Receive ATM Status Register- Channel 0 Reserved	0x00 0x00 0x00 0x00 0x00 0x00
0xN700 0xN701 0xN702 0xN703 0xN704 - 0xN706 0xN707 0xN709 0xN708 - 0xN709 0xN70A	Receive ATM Cell/PPP Control Receive ATM Control Register – Byte 1 Receive ATM Cell/PPP Control Receive ATM Control Register – Byte 1 Receive ATM Control Receive ATM Control Register – Byte 1 Receive ATM Control Receive ATM Control Register – Byte 1 Receive ATM Control Receive ATM Control Register – Byte 1 Receive ATM Cell/PPP Control Receive ATM Control Register – Byte 0 Reserved Receive ATM Status Register – Channel 0 Reserved Receive ATM Interrupt Status Register – Byte 1	0x00 0x00 0x00 0x00 0x00 0x00 0x00
0xN700 0xN701 0xN702 0xN703 0xN704 - 0xN706 0xN707 0xN708 - 0xN709 0xN70A 0xN70B	Receive ATM Cell/PPP Control Receive ATM Control Register – Byte 0 Receive ATM Cell/PPP Control Receive ATM Control Register – Byte 1 Receive ATM Coll/PPP Control Receive ATM Control Register – Byte 0 Receive ATM Status Register – Channel 0 Receive ATM Cell/PPP Processor Interrupt Status Register – Byte 0	0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x0
0xN700 0xN701 0xN702 0xN703 0xN704 - 0xN706 0xN707 0xN708 - 0xN709 0xN70A 0xN70B 0xN70C - 0xN70D	Reserved Reserved Receive ATM Cell Processor/PPP Cell Processor Block Control Registers and the "Channel Number" and ranges in value from 0x02 to 0x04 Receive ATM Control – Receive ATM Control Register - Byte 3 Receive ATM Control – Receive ATM Control Register – Byte 2 Receive ATM Control – Receive ATM Control Register – Byte 1 Receive ATM Cell/PPP Control – Receive ATM Control Register – Byte 0 Reserved Receive ATM Status Register- Channel 0 Reserved Receive ATM Interrupt Status Register – Byte 1 Receive ATM Cell/PPP Processor Interrupt Status Register – Byte 0 Reserved	0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x0
0xN700 0xN701 0xN702 0xN703 0xN704 - 0xN706 0xN707 0xN708 - 0xN709 0xN70A 0xN70B 0xN70B 0xN70C - 0xN70D 0xN70E	Reserved Reserved Receive ATM Cell Processor/PPP Cell Processor Block Control Registers and the "Channel Number" and ranges in value from 0x02 to 0x04 Receive ATM Control – Receive ATM Control Register - Byte 3 Receive ATM Control – Receive ATM Control Register - Byte 2 Receive ATM Control – Receive ATM Control Register – Byte 1 Receive ATM Cell/PPP Control – Receive ATM Control Register – Byte 0 Reserved Receive ATM Status Register - Channel 0 Reserved Receive ATM Cell/PPP Processor Interrupt Status Register – Byte 0 Reserved Receive ATM Cell/PPP Processor Interrupt Status Register – Byte 0 Reserved Receive ATM Cell/PPP Processor Interrupt Status Register – Byte 0 Reserved	0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x0
0xN700 0xN701 0xN702 0xN703 0xN704 - 0xN706 0xN707 0xN708 - 0xN709 0xN70A 0xN70B 0xN70D 0xN70C - 0xN70D 0xN70F	Reserved Reserved Receive ATM Cell Processor/ PPP Cell Processor Block Control Registers and the "Channel Number" and ranges in value from 0x02 to 0x04 Receive ATM Control – Receive ATM Control Register - Byte 3 Receive ATM Control – Receive ATM Control Register - Byte 2 Receive ATM Control – Receive ATM Control Register – Byte 1 Receive ATM Cell/PPP Control – Receive ATM Control Register – Byte 0 Reserved Receive ATM Status Register - Channel 0 Reserved Receive ATM Cell/PPP Processor Interrupt Status Register – Byte 0 Reserved Receive ATM Cell/PPP Processor Interrupt Status Register – Byte 0 Reserved Receive ATM Cell/PPP Processor Block Interrupt Enable Register – Byte 1 Receive ATM Cell/PPP Processor Block Interrupt Enable Register – Byte 0	0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x0
0xN700 0xN701 0xN702 0xN703 0xN704 - 0xN706 0xN707 0xN708 - 0xN709 0xN70A 0xN70B 0xN70C - 0xN70D 0xN70E 0xN70F 0xN710	Reserved Receive ATM Cell Processor/ PPP Cell Processor Block Control Registers and the "Channel Number" and ranges in value from 0x02 to 0x04 Receive ATM Control – Receive ATM Control Register - Byte 3 Receive ATM Control – Receive ATM Control Register - Byte 2 Receive ATM Control – Receive ATM Control Register – Byte 1 Receive ATM Cell/PPP Control – Receive ATM Control Register – Byte 0 Reserved Receive ATM Status Register- Channel 0 Reserved Receive ATM Cell/PPP Processor Interrupt Status Register – Byte 0 Reserved Receive ATM Cell/PPP Processor Block Interrupt Enable Register – Byte 1 Receive ATM Cell/PPP Processor Block Interrupt Enable Register – Byte 1 Receive ATM Cell/PPP Processor Block Interrupt Enable Register – Byte 1 Receive ATM Cell/PPP Processor Block Interrupt Enable Register – Byte 0 Receive ATM Cell/PPP Processor Block Interrupt Enable Register – Byte 0 Receive ATM Cell/PPP Processor Block Interrupt Enable Register – Byte 3	0x00 0x00 0x00 0x00 0x00 0x00 0x00 0x0





	Receive PPP Processor – Receive Good PPP Packet Count Register – Byte 0	
0xN714	Receive ATM Cell Insertion/Extraction Memory Data Register – Byte 3 Receive PPP Processor – Receive FCS Error Count Register – Byte 3	0x00
0xN715	Receive ATM Cell Insertion/Extraction Memory Data Register – Byte 2 Receive PPP Processor – Receive FCS Error Count Register – Byte 2	0x00
0xN716	Receive ATM Cell Insertion/Extraction Memory Data Register – Byte 1 Receive PPP Processor – Receive FCS Error Count Register – Byte 1	0x00
0xN717	Receive ATM Cell Insertion/Extraction Memory Data Register – Byte 0 Receive PPP Processor – Receive FCS Error Count Register – Byte 0	0x00
0xN718	Receive ATM Programmable User Defined Field Register – Byte 3 Receive PPP Processor – Receive ABORT Count Register – Byte 3	0x00
0xN719	Receive ATM Programmable User Defined Field Register - Byte 2 Receive PPP Processor - Receive ABORT Count Register - Byte 2	0x00
0xN71A	Receive ATM Programmable User Defined Field Register - Byte 1 Receive PPP Processor - Receive ABORT Count Register - Byte 1	0x00
0xN71B	Receive ATM Programmable User Defined Field Register – Byte 0 Receive PPP Processor – Receive ABORT Count Register – Byte 0	0x00
0xN71C	Receive PPP Processor – Receive RUNT PRP Count Register – Byte 3	0x00
0xN71D	Receive PPP Processor – Receive RUNT PPP Count Register – Byte 2	0x00
0xN71E	Receive PPP Processor – Receive RUNT PPP Count Register – Byte 1	0x00
0xN71F	Receive PPP Processor Receive RUNT PPP Count Register – Byte 0	0x00
0xN720	Receive ATM Controller - Test Cell Header – Byte 1	0x00
0xN721	Receive ATM Controller Test Cell Header – Byte 2	0x00
0xN722	Receive ATM Controller – Test Cell Header – Byte 3	0x00
0xN723	Receive ATM Controller Test Cell Header – Byte 4	0x00
0xN724	Receive ATM Controller – Test Cell Error Counter – Byte 3	0x00
0xN725	Receive ATM Controller – Test Cell Error Counter – Byte 2	0x00
0xN726	Receive ATM Controller – Test Cell Error Counter – Byte 1	0x00
0xN727	Receive ATM Controller – Test Cell Error Counter – Byte 0	0x00
0xN728	Receive ATM Controller – Receive ATM Cell Count – Byte 3	0x00
0xN729	Receive ATM Controller – Receive ATM Cell Count – Byte 2	0x00
0xN72A	Receive ATM Controller – Receive ATM Cell Count – Byte 1	0x00
0xN72B	Receive ATM Controller – Receive ATM Cell Count – Byte 0	0x00
0xN72C	Receive ATM Controller – Receive ATM Discard Cell Count – Byte 3	0x00
0xN72D	Receive ATM Controller – Receive ATM Discard Cell Count – Byte 2	0x00

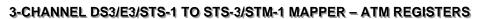
0xN72E	Receive ATM Controller – Receive ATM Discard Cell Count – Byte 1	0x00
0xN72F	Receive ATM Controller – Receive ATM Discard Cell Count – Byte 0	0x00
0xN730	Receive ATM Controller – Receive ATM Correctable HEC Cell Counter – Byte 3	0x00
0xN731	Receive ATM Controller – Receive ATM Correctable HEC Cell Counter – Byte 2	0x00
0xN732	Receive ATM Controller – Receive ATM Correctable HEC Cell Counter – Byte 1	0x00
0xN733	Receive ATM Controller – Receive ATM Correctable HEC Cell Counter – Byte 0	0x00
0xN734	Receive ATM Controller – Receive ATM Uncorrectable HEC Cell Counter – Byte 3	0x00
0xN735	Receive ATM Controller – Receive ATM Uncorrectable HEC Cell Counter – Byte 2	0x00
0xN736	Receive ATM Controller – Receive ATM Uncorrectable HEC Cell Counter – Byte 1	0x00
0xN737	Receive ATM Controller – Receive ATM Uncorrectable HEC Cell Counter – Byte 0 –Channel 0	0x00
0xN738 – 0xN742	Reserved	0x00
0xN743	Receive ATM Controller – Receive ATM Filter # 0 Control Register	0x00
0xN744	Receive ATM Controller – Receive ATM Filter # 0 Pattern – Header Byte 1	0x00
0xN745	Receive ATM Controller Receive ATM Filter # 0 Pattern – Header Byte 2	0x00
0xN746	Receive ATM Controller – Receive ATM Filter # 0 Pattern – Header Byte 3	0x00
0xN747	Receive ATM Controller Receive ATM Filter # 0 Pattern – Header Byte 4	0x00
0xN748	Receive ATM Controller – Receive ATM Filter # 0 Check – Header Byte 1	0x00
0xN749	Receive ATM Controller – Receive ATM Filter # 0 Check – Header Byte 2	0x00
0xN74A	Receive ATM Controller – Receive ATM Filter # 0 Check – Header Byte 3	0x00
0xN74B	Receive ATM Controller – Receive ATM Filter # 0 Check – Header Byte 4	0x00
0xN74C	Receive ATM Controller – Filter # 0 - Filtered Cell Count Register – Byte 3	0x00
0xN74D	Receive ATM Controller – Filter # 0 - Filtered Cell Count Register – Byte 2	0x00
0xN74E	Receive ATM Controller – Filter # 0 - Filtered Cell Count Register – Byte 1	0x00
0xN74F	Receive ATM Controller – Filter # 0 - Filtered Cell Count Register – Byte 0	0x00
0xN750 - 0xN752	Reserved	0x00
0xN753	Receive ATM Controller – Receive ATM Filter # 1 Control Register	0x00
0xN754	Receive ATM Controller – Receive ATM Filter # 1 Pattern – Header Byte 1	0x00
0xN755	Receive ATM Controller – Receive ATM Filter # 1 Pattern – Header Byte 2	0x00

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS



0xN756	Receive ATM Controller – Receive ATM Filter # 1 Pattern – Header Byte 3	0x00
0xN757	Receive ATM Controller – Receive ATM Filter # 1 Pattern – Header Byte 4	0x00
0xN758	Receive ATM Controller – Receive ATM Filter # 1 Check – Header Byte 1	0x00
0xN759	Receive ATM Controller – Receive ATM Filter # 1 Check – Header Byte 2	0x00
0xN75A	Receive ATM Controller – Receive ATM Filter # 1 Check – Header Byte 3	0x00
0xN75B	Receive ATM Controller – Receive ATM Filter # 1 Check – Header Byte 4	0x00
0xN75C	Receive ATM Controller – Filter # 1 – Filtered Cell Count Register – Byte 3	0x00
0xN75D	Receive ATM Controller – Filter # 1 - Filtered Cell Count Register – Byte 2	0x00
0xN75E	Receive ATM Controller – Filter # 1 - Filtered Cell Count Register – Byte 1	0x00
0xN75F	Receive ATM Controller – Filter # 1 - Filtered Cell Count Register – Byte 0	0x00
0xN760 – 0xN762	Reserved	0x00
0xN763	Receive ATM Controller – Receive ATM Filter # 2 Control Register	0x00
0xN764	Receive ATM Controller – Receive ATM Filter # 2 Pattern – Header Byte 1	0x00
0xN765	Receive ATM Controller – Receive ATM Filter# 2 Pattern – Header Byte 2	0x00
0xN766	Receive ATM Controller – Receive ATM Filter #2 Pattern – Header Byte 3	0x00
0xN767	Receive ATM Controller – Receive ATM Filter # 2 Pattern – Header Byte 4	0x00
0xN768	Receive ATM Controller – Receive ATM Filter # 2 Check – Header Byte 1	0x00
0xN769	Receive ATM Controller – Receive ATM Filter # 2 Check – Header Byte 2	0x00
0xN76A	Receive ATM Controller - Receive ATM Filter # 2 Check - Header Byte 3	0x00
0xN76B	Receive ATM Controller - Receive ATM Filter # 2 Check - Header Byte 4	0x00
0xN76C	Receive ATM Controller Filter # 2 - Filtered Cell Count Register – Byte 3	0x00
0xN76D	Receive ATM Controller – Filter # 2 - Filtered Cell Count Register – Byte 2	0x00
0xN76E	Receive ATM Controller - Filter # 2 - Filtered Cell Count Register - Byte 1	0x00
0xN76F	Receive ATM Controller – Filter # 2 - Filtered Cell Count Register – Byte 0	0x00
0xN770 – 0xN772	Reserved	0x00
0xN773	Receive ATM Controller – Receive ATM Filter # 3 Control Register	0x00
0xN774	Receive ATM Controller – Receive ATM Filter # 3 Pattern – Header Byte 1	0x00
0xN775	Receive ATM Controller – Receive ATM Filter # 3 Pattern – Header Byte 2	0x00
0xN776	Receive ATM Controller – Receive ATM Filter # 3 Pattern – Header Byte 3	0x00
0xN777	Receive ATM Controller – Receive ATM Filter # 3 Pattern – Header Byte 4	0x00
0xN778	Receive ATM Controller – Receive ATM Filter # 3 Check – Header Byte 1	0x00
0xN779	Receive ATM Controller – Receive ATM Filter # 3 Check – Header Byte 2	0x00

0xN77A	Receive ATM Controller – Receive ATM Filter # 3 Check – Header Byte 3	0x00
0xN77B	Receive ATM Controller – Receive ATM Filter # 3 Check – Header Byte 4	0x00
0xN77C	Receive ATM Controller – Filter # 3 - Filtered Cell Count Register – Byte 3	0x00
0xN77D	Receive ATM Controller – Filter # 3 - Filtered Cell Count Register – Byte 2	0x00
0xN77E	Receive ATM Controller – Filter # 3 - Filtered Cell Count Register – Byte 1	0x00
0xN77F	Receive ATM Controller – Filter # 3 - Filtered Cell Count Register – Byte 0	0x00
0xN780 – 0xN901	Reserved	0x00
	TRANSMIT ATM CELL PROCESSOR/ PPP PROCESSOR BLOCK REGISTERS	
Note: N repres	sents the "Channel Number" and ranges in value from 0x02 to 0x04	
0xNF00	Transmit ATM Cell Processor Control Register – Byte 3	0x00
0xNF01	Transmit ATM Cell Processor Control Register – Byte 2	0x00
0xNF02	Transmit ATM Cell Processor Control Register – Byte 1	0x00
0xNF03	Transmit ATM Cell/PPP Processor Control Register - Byte 0	0x00
0xNF04	Transmit ATM Status Register	0x00
0xNF05 – 0xNF0A	Reserved	0x00
0xNF0B	Transmit ATM Cell/PPP Processor Interrupt Status Register	0x00
0xNF0C – 0xNF0E	Reserved	0x00
0xNF0F	Transmit ATM Cell/PPP Processor Interrupt Enable Register	0x00
0xNF10 – 0xNF12	Reserved	0x00
0xNF13	Transmit ATM Cell Insertion/Extraction Memory Control Register	0x00
0xNF14	Transmit ATM Cell Insertion/Extraction Memory – Byte 3	0x00
0xNF15	Transmit ATM Cell Insertion/Extraction Memory – Byte 2	0x00
0xNF16	Transmit ATM Cell Insertion/Extraction Memory – Byte 1	0x00
0xNF17	Transmit ATM Cell Insertion/Extraction Memory – Byte 0	0x00
0xNF18	Transmit ATM Cell – Idle Cell Header Byte # 1 Register	0x00
0xNF19	Transmit ATM Cell – Idle Cell Header Byte # 2 Register	0x00
0xNF1A	Transmit ATM Cell – Idle Cell Header Byte # 3 Register	0x00
0xNF1B	Transmit ATM Cell – Idle Cell Header Byte # 4 Register	0x00
0xNF1C – 0xNF1E	Reserved	0x00
0xNF1F	Transmit ATM Cell – Idle Cell Payload Byte Register	0x00
0xNF20	Transmit ATM Cell – Test Cell Header Byte # 1 Register	0x00
0xNF21	Transmit ATM Cell – Test Cell Header Byte # 2 Register	0x00





0xNF22	Transmit ATM Cell – Test Cell Header Byte # 3 Register	0x00
0xNF23	Transmit ATM Cell – Test Cell Header Byte # 4 Register	0x00
0xNF24 – 0xNF27	Reserved	0x00
0xNF28	Transmit ATM Cell – Cell Count Register – Byte 3	0x00
0xNF29	Transmit ATM Cell – Cell Count Register – Byte 2	0x00
0xNF2A	Transmit ATM Cell – Cell Count Register – Byte 1	0x00
0xNF2B	Transmit ATM Cell – Cell Count Register – Byte 0	0x00
0xNF2C	Transmit ATM Cell – Discard Cell Count Register – Byte 3	0x00
0xNF2D	Transmit ATM Cell – Discard Cell Count Register – Byte 2	0x00
0xNF2E	Transmit ATM Cell – Discard Cell Count Register – Byte 1	0x00
0xNF2F	Transmit ATM Cell – Discard Cell Count Register – Byte 0	0x00
0xNF30	Transmit ATM Cell – HEC Byte Error Count Register Byte 3	0x00
0xNF31	Transmit ATM Cell – HEC Byte Error Count Register – Byte 2	0x00
0xNF32	Transmit ATM Cell – HEC Byte Error Count Register Byte 1	0x00
0xNF33	Transmit ATM Cell – HEC Byte Error Count Register – Byte 0	0x00
0xNF34	Transmit ATM Cell – Parity Error Count Register – Byte 3	0x00
0xNF35	Transmit ATM Cell – Parity Error Count Register – Byte 2	0x00
0xNF36	Transmit ATM Cell – Parity Error Count Register – Byte 1	0x00
0xNF37	Transmit ATM Cell – Parity Error Count Register – Byte 0	0x00
0xNF38 – 0xNF42	Reserved	0x00
0xNF43	Transmit ATM Controller Transmit ATM Filter # 0 Control Register	0x00
0xNF44	Transmit ATM Controller - Transmit ATM Filter # 0 Pattern - Header Byte 1	0x00
0xNF45	Transmit ATM Controller - Transmit ATM Filter # 0 Pattern - Header Byte 2	0x00
0xNF46	Transmit ATM Controller – Transmit ATM Filter # 0 Pattern – Header Byte 3	0x00
0xNF47	Transmit ATM Controller – Transmit ATM Filter # 0 Pattern – Header Byte 4	0x00
0xNF48	Transmit ATM Controller – Transmit ATM Filter # 0 Check – Header Byte 1	0x00
0xNF49	Transmit ATM Controller – Transmit ATM Filter # 0 Check – Header Byte 2	0x00
0xNF4A	Transmit ATM Controller – Transmit ATM Filter # 0 Check – Header Byte 3	0x00
0xNF4B	Transmit ATM Controller – Transmit ATM Filter # 0 Check – Header Byte 4	0x00
0xNF4C	Transmit ATM Cell – Cell Count Register – Byte 3	0x00
0xNF4D	Transmit ATM Cell – Cell Count Register – Byte 2	0x00
0xNF4E	Transmit ATM Cell – Cell Count Register – Byte 1	0x00

0xNF4F	Transmit ATM Cell – Cell Count Register – Byte 0	0x00
0xNF50 - 0xNF52	Reserved	0x00
0xNF53	Transmit ATM Controller – Transmit ATM Filter # 1 Control Register	0x00
0xNF54	Transmit ATM Controller – Transmit ATM Filter # 1 Pattern – Header Byte 1	0x00
0xNF55	Transmit ATM Controller – Transmit ATM Filter # 1 Pattern – Header Byte 2	0x00
0xNF56	Transmit ATM Controller – Transmit ATM Filter # 1 Pattern – Header Byte 3	0x00
0xNF57	Transmit ATM Controller – Transmit ATM Filter # 1 Pattern – Header Byte 4	0x00
0xNF58	Transmit ATM Controller – Transmit ATM Filter # 1 Check – Header Byte 1	0x00
0xNF59	Transmit ATM Controller – Transmit ATM Filter # 1 Check – Header Byte 2	0x00
0xNF5A	Transmit ATM Controller – Transmit ATM Filter # 1 Check - Header Byte 3	0x00
0xNF5B	Transmit ATM Controller – Transmit ATM Filter # 1 Check – Header Byte 4	0x00
0xNF5C	Transmit ATM Cell – Cell Count Register - Byte	0x00
0xNF5D	Transmit ATM Cell – Cell Count Register – Byte 2	0x00
0xNF5E	Transmit ATM Cell – Cell Count Register Byte	0x00
0xNF5F	Transmit ATM Cell – Cell Count Register – Byte 0	0x00
0xNF60 – 0xNF62	Reserved	0x00
0xNF63	Transmit ATM Controller - Transmit ATM Filter # 2 Control Register	0x00
0xNF64	Transmit ATM Controller Transmit ATM Filter # 2 Pattern – Header Byte 1	0x00
0xNF65	Transmit ATM Controller – Transmit ATM Filter # 2 Pattern – Header Byte 2	0x00
0xNF66	Transmit ATM Controller - Transmit ATM Filter # 2 Pattern - Header Byte 3	0x00
0xNF67	Transmit ATM Controller - Transmit ATM Filter # 2 Pattern - Header Byte 4	0x00
0xNF68	Transmit ATM Controller – Transmit ATM Filter # 2 Check – Header Byte 1	0x00
0xNF69	Transmit ATM Controller – Transmit ATM Filter # 2 Check – Header Byte 2	0x00
0xNF6A	Transmit ATM Controller – Transmit ATM Filter # 2 Check – Header Byte 3	0x00
0xNF6B	Transmit ATM Controller – Transmit ATM Filter # 3 Check – Header Byte 4	0x00
0xNF6C	Transmit ATM Cell – Cell Count Register – Byte 3	0x00
0xNF6D	Transmit ATM Cell – Cell Count Register – Byte 2	0x00
0xNF6E	Transmit ATM Cell – Cell Count Register – Byte 1	0x00
0xNF6F	Transmit ATM Cell – Cell Count Register – Byte 0	0x00
0xNF70 – 0xNF72	Reserved	0x00
0xNF73	Transmit ATM Controller – Transmit ATM Filter # 3 Control Register	0x00
0xNF74	Transmit ATM Controller – Transmit ATM Filter # 3 Pattern – Header Byte 1	0x00

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS



0xNF75 0x00 Transmit ATM Controller – Transmit ATM Filter # 3 Pattern – Header Byte 2 0xNF76 0x00 Transmit ATM Controller – Transmit ATM Filter # 3 Pattern – Header Byte 3 0xNF77 Transmit ATM Controller - Transmit ATM Filter # 3 Pattern - Header Byte 4 0x00 0xNF78 Transmit ATM Controller - Transmit ATM Filter # 3 Check - Header Byte 1 0x00 0xNF79 0x00 Transmit ATM Controller - Transmit ATM Filter # 3 Check - Header Byte 2 0xNF7A Transmit ATM Controller - Transmit ATM Filter # 3 Check - Header Byte 3 0x00 0xNF7B 0x00 Transmit ATM Controller – Transmit ATM Filter # 3 Check – Header Byte 4 0xNF7C 0x00 Transmit ATM Cell - Cell Count Register - Byte 3 0xNF7D 0x00 Transmit ATM Cell - Cell Count Register - Byte 2 0xNF7E Transmit ATM Cell - Cell Count Register - Byte 1 0x00 0xNF7F 0x00 Transmit ATM Cell - Cell Count Register - Byte 0 0xNF80 -0x00 Reserved 0xN102 RECEIVE STS-1 TOH AND POH PROCESSOR BLOCK REGISTERS N represents the "Channel Number" and ranges in value from 0x05 to 0x07 Note: 0xN103 0x00 Receive STS-1 Transport Control Register Byte 0 0xN104 - 0xN1050x00 Reserved 0xN106 Receive STS-1 Transport Status Register - Byte 1 0x00 0xN107 0x02 Receive STS-1 Transport Status Register - Byte 0 0xN108 Reserved 0x00 0xN109 Receive STS-1 Transport Interrupt Status Register - Byte 2 0x00 0xN10A Receive STS-1 Transport Interrupt Status Register - Byte 1 0x00 0xN10B Receive STS-1 Transport Interrupt Status Register – Byte 0 0x00 0xN10C Reserved 0 0x00 0xN10D Receive STS-1 Transport Interrupt Enable Register – Byte 2 0x00 0xN10E Receive STS-1 Transport Interrupt Enable Register – Byte 1 0x00 0xN10F 0x00 Receive STS-1 Transport Interrupt Enable Register – Byte 0 0xN110 0x00 Receive STS-1 Transport B1 Error Count - Byte 3 0x00 0xN111 Receive STS-1 Transport B1 Error Count - Byte 2 0xN112 Receive STS-1 Transport B1 Error Count - Byte 1 0x00 0xN113 0x00 Receive STS-1 Transport B1 Error Count - Byte 0 0xN114 0x00 Receive STS-1 Transport B2 Error Count - Byte 3 0x00 0xN115 Receive STS-1 Transport B2 Error Count - Byte 2 0xN116 0x00 Receive STS-1 Transport B2 Error Count - Byte 1

0xN117	Receive STS-1 Transport B2 Error Count – Byte 0	0x00
0xN118	Reserved	0x00
0xN119	Receive STS-1 Transport REI-L Error Count – Byte 3	0x00
0xN11A	Receive STS-1 Transport REI-L Error Count – Byte 2	0x00
0xN11B	Receive STS-1 Transport REI-L Error Count – Byte 1	0x00
0xN11C	Receive STS-1 Transport REI-L Error Count – Byte 0	0x00
0xN11D – 0xN11E	Reserved	0x00
0xN11F	Receive STS-1 Transport – Received K1 Byte Value	0x00
0xN120 – 0xN122	Reserved	0x00
0xN123	Receive STS-1 Transport – Received K2 Byte Value	0x00
0xN124 – 0xN126	Reserved	0x00
0xN127	Receive STS-1 Transport – Received S1 Byte Value	0x00
0xN128 – 0xN12D	Reserved	0x00
0xN12E	Receive STS-1 Transport – LOS Threshold Value – MSB	0xFF
0xN12F	Receive STS-1 Transport – LOS Threshold Value – LSB	0xFF
0xN130	Reserved	0x00
0xN131	Receive STS-1 Transport – Receive SF Set Monitor Interval – Byte 2	0x00
0xN132	Receive STS-1 Transport Receive SF Set Monitor Interval – Byte 1	0x00
0xN133	Receive STS-1 Transport – Receive SF Set Monitor Interval – Byte 0	0x00
0xN134, 0xN135	Reserved	0x00
0xN136	Receive STS-1 Transport - Receive SF Set Threshold - Byte 1	0x00
0xN137	Receive STS-1 Transport – Receive SF Set Threshold – Byte 0	0x00
0xN138 – 0xN139	Reserved	0x00
0xN13A	Receive STS-1 Transport – Receive SF Clear Threshold – Byte 1	0x00
0xN13B	Receive STS-1 Transport – Receive SF Clear Threshold – Byte 0	0x00
0xN13C	Reserved	0x00
0xN13D	Receive STS-1 Transport – Receive SD Set Monitor Interval – Byte 2	0x00
0xN13E	Receive STS-1 Transport – Receive SD Set Monitor Interval – Byte 1	0x00
0xN13F	Receive STS-1 Transport – Receive SD Set Monitor Interval – Byte 0	0x00
0xN140 – 0xN141	Reserved	0x00
0xN142	Receive STS-1 Transport – Receive SD Set Threshold – Byte 1	0x00
0xN143	Receive STS-1 Transport – Receive SD Set Threshold – Byte 0	0x00
0xN144, 0xN145	Reserved	0x00

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS



Rev 2.0.0

0xN146 0x00 Receive STS-1 Transport - Receive SD Clear Threshold - Byte 1 0xN147 0x00 Receive STS-1 Transport - SD Clear Threshold - Byte 0 0xN14B - 0xN14A Reserved 0x00 0xN14B Receive STS-1 Transport - Force SEF Condition 0x00 0xN14C - 0xN14E 0x00 Reserved 0xN14F Receive STS-1 Transport - Receive J0 Trace Buffer Control Register 0x00 0xN150 - 0xN151 Reserved 0xN152 0x00 Receive STS-1 Transport - Receive SD Burst Error Count Tolerance - Byte 1 0xN153 0x00 Receive STS-1 Transport – Receive SD Burst Error Count Tolerance → Byte 0 0xN154, 0xN155 0x00 Reserved 0xN156 0x00 Receive STS-1 Transport – Receive SF Burst Error Count Tolerance – Byte 1 0xN157 Receive STS-1 Transport - Receive SF Burst Error Count Tolerance - Byte 0 0x00 0xN158 0x00 Reserved 0xN159 Receive STS-1 Transport - Receive SD Clear Monitor Interval - Byte 2 0x00 Receive STS-1 Transport - Receive SD Clear Monitor Interval - Byte 1 0x00 0xN15A Receive STS-1 Transport - Receive SD Clear Monitor Interval - Byte 0 0xN15B 0x00 0xN15C 0x00 Reserved 0xN15D Receive STS-1 Transport - Receive SF Clear Monitor Interval - Byte 2 0x00 Receive STS-1 Transport Receive SF Clear Monitor Interval – Byte 1 0x00 0xN15E 0xN15F Receive STS-1 Transport - Receive SF Clear Monitor Interval - Byte 0 0x00 0xN160 - 0xN162 0x00 Reserved 0xN163 0x00 Receive STS-1 Transport - Auto AIS Control Register 0xN164 - 0xN16A 0x00 Reserved O 0xN16B 0x00 Receive STS1 Transport - Auto AIS (in Downstream STS-1s) Control Register 0xN16C - 0xN182 0x00 Reserved 0xN183 0x00 Receive STS-1 Path - Control Register - Byte 2 0xN184 - 0xN185 0x00 Reserved 0xN186 Receive STS-1 Path - Control Register - Byte 1 0xN187 0x00 Receive STS-1 Path - Status Register - Byte 0 0xN188 0x00 Reserved 0xN189 Receive STS-1 Path - Interrupt Status Register - Byte 2 0x00 0xN18A 0x00 Receive STS-1 Path - Interrupt Status Register - Byte 1 0xN18B 0x00 Receive STS-1 Path - Interrupt Status Register - Byte 0

0.11100		0.00
0xN18C	Reserved	0x00
0xN18D	Receive STS-1 Path – Interrupt Enable Register – Byte 2	0x00
0xN18E	Receive STS-1 Path – Interrupt Enable Register – Byte 1	0x00
0xN18F	Receive STS-1 Path – Interrupt Enable Register – Byte 0	0x00
0xN190 – 0xN192	Reserved	0x00
0xN193	Receive STS-1 Path – SONET Receive RDI-P Register	0x00
0xN194, 0xN195	Reserved	0x00
0xN196	Receive STS-1 Path – Received Path Label Value (C2 Byte) Register	0x00
0xN197	Receive STS-1 Path – Expected Path Label Value (C2 Byte) Register	0x00
0xN198	Receive STS-1 Path – B3 Error Count Register – Byte 3	0x00
0xN199	Receive STS-1 Path – B3 Error Count Register – Byte 2	0x00
0xN19A	Receive STS-1 Path – B3 Error Count Register - Byte	0x00
0xN19B	Receive STS-1 Path – B3 Error Count Register – Byte 0	0x00
0xN19C	Receive STS-1 Path – REI-P Error Count Register – Byte 3	0x00
0xN19D	Receive STS-1 Path – REI-P Error Count Register - Byte 2	0x00
0xN19E	Receive STS-1 Path – REI-P Error Count Register – Byte 1	0x00
0xN19F	Receive STS-1 Path – REI-P Error Count Register – Byte 0	0x00
0xN1A0 - 0xN1A5	Reserved	0x00
0xN1A6	Receive STS-1 Path Pointer Value - Byte 1	0x00
0xN1A7	Receive STS-1 Path - Pointer Value - Byte 0	0x00
0xN1A8 – 0xN1BA	Reserved	0x00
0xN1BB	Receive STS-1 Path – AUTO AIS Control Register	0x00
0xN1BC – 0xN1BE	Reserved	0x00
0xN1BF	Receive STS-1 Path – Serial Port Control Register	0x00
0xN1C0 - 0xN1C2	Reserved	0x00
0xN1C3	Receive STS-1 Path – SONET Receive Auto Alarm Register – Byte 0	0x00
0xN1C4 -0xN1D2	Reserved	0x00
0xN1D3	Receive STS-1 Path – Receive J1 Byte Capture Register	0x00
0xN1D4 – 0xN1D6	Reserved	0x00
0xN1D7	Receive STS-1 Path – Receive B3 Byte Capture Register	0x00
0xN1D8 – 0xN1DA	Reserved	0x00
0xN1DB	Receive STS-1 Path – Receive C2 Byte Capture Register	0x00

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

	Pagaiya CTC 1 Bath - Pagaiya C1 Buta Cantura Pagiator	
0vN1E0 = 0vN1E2	Receive STS-1 Path – Receive G1 Byte Capture Register	0x00
OXIVILO - UXIVIEZ	Reserved	0x00
0xN1E3	Receive STS-1 Path – Receive F2 Byte Capture Register	0x00
0xN1E4 - 0xN1E6	Reserved	0x00
0xN1E7	Receive STS-1 Path – Receive H4 Byte Capture Register	0x00
0xN1E8 – 0xN1EA	Reserved	0x00
0xN1EB	Receive STS-1 Path – Receive Z3 Byte Capture Register	0x00
0xN1EC – I 0xN1EE	Reserved	0x00
0xN1EF	Receive STS-1 Path – Receive Z4 (K3) Byte Capture Register	0x00
0xN1F0 – 0xN1F2	Reserved	0x00
0xN1F3	Receive STS-1 Path – Receive Z5 Byte Capture Register	0x00
0xN1F4 – 0xN1FF	Reserved	0x00
Re	eceive STS-1 TOH Processor Block – Receive J0 (Path) Trace Message Buffer	
Note: N represents	s the "Channel Number" and ranges in value from 0x05 to 0x07	
	Receive STS-1 POH Processor Block - Receive J0 (Path) Trace Message Buffer - Expected and Received	0x00
0xN340 - 0xN3FF	Reserved	0x00
Reci	EIVE STS-1 POH PROCESSOR BLOCK – RECEIVE J1 (PATH) TRACE MESSAGE BUFFER	
Note: N represents	s the "Channel Number" and ranges in Value from 0x05 to 0x07	
	Receive STS-1 POH Processor Block – Receive J1 (Path) Trace Message Buffer – Expected and Received	0x00
0xN540 - 0xN5FF	Reserved	0x00
Note: N represents	DS3/E3 MAPPER BLOCK REGISTER s the "Channel Number" and ranges in value from 0x02 to 0x04	
0xNA00 – 0xNB00 I	Unused	0x00
0xNB01	Mapper Control Register – Byte 2	0x00
0xNB02	Mapper Control Register – Byte 1	0x03
0xNB03	Mapper Control Register – Byte 0	0x80
0xNB04, 0xNB05	Unused	0x00
0xNB06	Receive Mapper Status Register – Byte 1	0x03
0xNB07	Receive Mapper Status Register – Byte 0	0x00
0xNB08 – 0xNB0A	Unused	0x00
0xNB0B	Receive Mapper Interrupt Status Register – Byte 0	0x00

0xNB0C – 0xNB0E	Unused	0x00
0xNB0F	Receive Mapper Interrupt Enable Register – Byte 0	0x00
0xNB10 – 0xNB12	Unused	0x00
0xNB13	T3/E3 Routing Register Byte	0x00
0xNB14 – 0xNBFF	Reserved	0x00
	TRANSMIT SONET POH PROCESSOR BLOCK REGISTERS	•
Note: N represen	ts the "Channel Number" and ranges in value from 0x02 to 0x04)	
0xN800 – 0xN981	Reserved	0x00
0xN982	Transmit SONET Path – SONET Control Register – Byte 1	0x00
0xN983	Transmit SONET Path – SONET Control Register – Byte 0	0x00
0xN984 – 0xN8992	Reserved	0x00
0xN993	Transmit SONET Path – Transmitter J1 Byte Value Register	0x00
0xN994 – 0xN995	Reserved	0x00
0xN996	Transmit SONET Path – B3 Byte Control Register	0x00
0xN997	Transmit SONET Path – B3 Byte Mask Register	0x00
0xN998 – 0xN99A	Reserved	0x00
0xN99B	Transmit SONET Path – Transmit C2 Byte Value Register	0x00
0xN99C - 0xN99E	Reserved	0x00
0xN99F	Transmit SONET Path - Transmit G1 Byte Value Register	0x00
0xN9A0 - 0xN9A2	Reserved	0x00
0xN9A3	Transmit SONET Path – Transmit F2 Byte Value Register	0x00
0xN9A4 – 0xN9A6	Reserved	0x00
0xN9A7	Transmit SONET Path – Transmit H4 Byte Value Register	0x00
0xN9A8 – 0xN9AA	Reserved	0x00
0xN9AB	Transmit SONET Path – Transmit Z3 Byte Value Register	0x00
0xN9AC – 0xN9AE	Reserved	0x00
0xN9AF	Transmit SONET Path – Transmit Z4 Byte Value Register	0x00
0xN9B0 - 0xN9B2	Reserved	0x00
0xN9B3	Transmit SONET Path – Transmit Z5 Byte Value Register	0x00
0xN9B4 – 0xN9B6	Reserved	0x00
0xN9B7	Transmit SONET Path – Transmit Path Control Register – Byte 0	0x00
0xN9B8 – 0xN9BA	Reserved	0x00



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

0xN9BB 0x00 Transmit SONET Path - Transmit J1 Control Register 0xN9BC -0x00 0xN9BE 0xN9BF Transmit SONET Path - Transmit Arbitrary H1 Pointer Register 0x94 0xN9C0 - 0xN9C2 Reserved 0x00 0xN9C3 Transmit SONET Path - Transmit Arbitrary H2 Pointer Register 0x00 0xN9C4 - 0xN9C5 0x00 0xN9C6 0x02 Transmit SONET Path - Transmit Pointer Byte Register - Byte 1 0xN9C7 Transmit SONET Path - Transmit Pointer Byte Register - Byte 0 0x0A 0xN9C8 0x00 Reserved Transmit SONET Path - RDI-P Control Register - Byte 2 0xN9C9 0x40 0xN9CA 0xC0 Transmit SONET Path – RDI-P Control Register – Byte 1 0xN9CB Transmit SONET Path - RDI-P Control Register - Byte 0 0xA0 0xN9CC -0x00 Reserved 0xN9CE 0xN9CF Transmit SONET Path - Transmit Path Serial Port Control Register 0x00 0xN9D0 - 0xN9FF 0x00 Reserved TRANSMIT SONET POH PROCESSOR BLOCK TRANSMIT 11 (PATH) TRACE MESSAGE BUFFER N represents the "Channel Number" and ranges in value from 0x02 to 0x04 Note: 0xND00 - 0xND3F Transmit SONET POH Processor Block Transmit J1 (Path) Trace Message 0x00 Buffer 0xND40 - 0xNEFF 0x00 Reserved TRANSMIT STS-1 TOH AND POH PROCESSOR BLOCK REGISTERS N represents the "Channel Numbers" and ranges in value from 0x05 to 0x07) Note: 0xN800 - 0xN901Reserved 0x00 0xN902 Transmit STS-1 Transport - SONET Transmit Control Register - Byte 1 0x00 0xN903 Transmit STS-1 Transport – SONET Transmit Control Register – Byte 0 0x00 0xN904 - 0xN9220x00 Reserved 0xN923 Transmit STS-1 Transport - B1 Byte Error Mask Register 0x00 0xN924 - 0xN92A 0x00 Reserved 0xN92B 0x00 Transmit STS-1 Transport – Transmit B2 Bit Error Mask Register – Byte 0 0xN92C - 0xN92D Reserved 0x00 0x00 0xN92E Transmit STS-1 Transport - K1K2 (APS) Value Register - Byte 1 0xN92F 0x00 Transmit STS-1 Transport - K1K2 (APS) Value Register - Byte 0 0xN930 - 0xN9320x00 Reserved

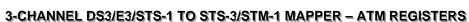
0xN933	Transmit STS-1 Transport – RDI-L Control Register	0x00
0xN934 – 0xN936	Reserved	0x00
0xN937	Transmit STS-1 Transport – M0M1 Value Register	0x00
0xN938 - 0xN93A	Reserved	0x00
0xN93B	Transmit STS-1 Transport – S1 Byte Value Register	0x00
0xN93C - 0xN93E	Reserved	0x00
0xN93F	Transmit STS-1 Transport – F1 Byte Value Register	0x00
0xN940 - 0xN942	Reserved	0x00
0xN943	Transmit STS-1 Transport – E1 Byte Value Register	0x00
0xN944 – 0xN946	Reserved	0x00
0xN947	Transmit STS-1 Transport – E2 Byte Value Register	0x00
0xN948 – 0xN94A	Reserved	0x00
0xN94B	Transmit STS-1 Transport – J0 Byte Value Register	0x00
0xN94C - 0xN94E	Reserved	0x00
0xN94F	Transmit STS-1 Transport – J0 Byte Control Register	0x00
0xN950 – 0xN981	Reserved	0x00
0xN982	Transmit STS-1 Path – SONET Control Register – Byte 1	0x00
0xN983	Transmit STS-1 Path – SQNET Control Register – Byte 0	0x00
0xN984 – 0xN992	Reserved	0x00
0xN993	Transmit STS-1 Path - Transmitter J1 Byte Value Register	0x00
0xN994 – 0xN995	Reserved	0x00
0xN996	Transmit STS-1 Path - B3 Byte Control Register	0x00
0xN997	Transmit STS-1 Path - B3 Byte Mask Register	0x00
0xN998 – 0xN99A	Reserved	0x00
0xN99B	Transmit STS-1 Path – Transmit C2 Byte Value Register	0x00
0xN99C - 0xN99E	Reserved	0x00
0xN99F	Transmit STS-1 Path – Transmit G1 Byte Value Register	0x00
0xN9A0 – 0xN9A2	Reserved	0x00
0xN9A3	Transmit STS-1 Path – Transmit F2 Byte Value Register	0x00
0xN9A4 – 0xN9A6	Reserved	0x00
0xN9A7	Transmit STS-1 Path – Transmit H4 Value Register	0x00
0xN9A8 – 0xN9AA	Reserved	0x00
0xN9AB	Transmit STS-1 Path – Transmit Z3 Value Register	0x00

Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

0xN9AC – 0xN9AE	Reserved	0x00
0xN9AF	Transmit STS-1 Path – Transmit Z4 Value Register	0x00
0xN9B0 - 0xN9B2	Reserved	0x00
0xN9B3	Transmit STS-1 Path – Transmit Z5 Value Register	0x00
0xN9B4 – 0xN9B6	Reserved	0x00
0xN9B7	Transmit STS-1 Path – Transmit Path Control Register – Byte 0	0x00
0xN9B8 - 0xN9BA	Reserved	0x00
0xN9BB	Transmit STS-1 Path – Transmit J1 Control Register	0x00
0xN9BC – 0xN9BE	Reserved	0x00
0xN9BF	Transmit STS-1 Path – Transmit Arbitrary H1 Pointer Register	0x94
0xN9C0 - 0xN9C2	Reserved	0x00
0xN9C3	Transmit STS-1 Path – Transmit Arbitrary H2 Pointer Register	0x00
0xN9C4 - 0xN9C5	Reserved	0x00
0xN9C6	Transmit STS-1 Path – Transmit Pointer Byte Register – Byte 1	0x02
0xN9C7	Transmit STS-1 Path – Transmit Pointer Byte Register – Byte 0	0x0A
0xN9C8	Reserved	0x00
0xN9C9	Transmit STS-1 Path – RDI-P Control Register – Byte 2	0x40
0xN9C2	Transmit STS-1 Path – RDI-P Control Register – Byte 1	0xC0
0xN9CB	Transmit STS-1 Path – RDI-P Control Register – Byte 0	0xA0
0xN9CC – 0xN9CE	Reserved	0x00
0xN9CF	Transmit STS-1 Path Transmit Path Serial Port Control Register	0x00
0xN9D0 -0xN9FF	Reserved	0x00
	NSMIT STS-1 TOH PROCESSOR BLOCK – TRANSMIT J0 (PATH) TRACE MESSAGE BUFFI Ints the "Channel Number" and ranges in value from 0x05 to 0x07	ER
0xNB00 – 0xNB3F	Transmit STS-1 POH Processor Block – Transmit J0 (Path) Trace Message Buffer	0x00
0xNB40 – 0xNBFF	Reserved	0x00
TRA	NSMIT STS-1 POH PROCESSOR BLOCK – TRANSMIT J1 (PATH) TRACE MESSAGE BUFFI	ER
Note: N represer	nts the "Channel Number" and ranges in value from 0x05 to 0x07	
0xND00 – 0xND3F	Transmit STS-1 POH Processor Block – Transmit J1 (Path) Trace Message Buffer	0x00
0xND40 – 0xNDFF	Reserved	0x00
	DS3/E3 FRAMER BLOCK REGISTERS	
Note: N represents the "Channel Number" and ranges in value from 0x02 to 0x04		

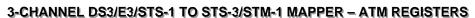
0xN300	Operating Mode Register	0x23
0xN301	I/O Control Register	0xA0
0xN302 – 0xN303	Reserved	0x00
0xN304	Block Interrupt Enable Register	0x00
0xN305	Block Interrupt Status Register	0x00
0xN306 – 0xN30B	Reserved	0x00
0xN30C	Test Register	0x00
0xN30D - 0xN30F	Reserved	0x00
0xN310	RxDS3 Configuration and Status Register RxE3 Configuration and Status Register # 1 – G.832 RxE3 Configuration and Status Register # 2 – G.751 RxDS3 Status Register	0x02
0xN311	RxDS3 Status Register RxE3 Configuration and Status Register # 2 – G.832 RxE3 Configuration and Status Register # 2 – G.751	0x67
0xN312	RxDS3 Interrupt Enable Register RxE3 Interrupt Enable Register # 1 – G.832 RxE3 Interrupt Enable Register # 1 – G.751	0x00
0xN313	RxDS3 Interrupt Status Register RxE3 Interrupt Enable Register # 2 – G.832 RxE3 Interrupt Enable Register # 2 – G.751	0x00
0xN314	RxDS3 Sync Detect Enable Register RxE3 Interrupt Status Register # 1 – G.832 RxE3 Interrupt Status Register # 1 – G.751	0x00
0xN315	RxE3 Interrupt Status Register # 2 – G.832 RxE3 Interrupt Status Register # 2 – G.751	0x00
0xN316	RxDS3 FEAC Register	0x7E
0xN317	RxDS3 FEAO Interrupt Enable/Status Register	0x00
0xN318	RxDS3 LAPD Control Register RxE3 LAPD Control Register	0x00
0xN319	RxDS3 LAPD Status Register RxE3 LAPD Status Register	0x00
0xN31A	RxE3 NR Byte Register – G.832 RxE3 Service Bit Register –G.751	0x00
0xN31B	RxE3 GC Byte Register – G.832	0x00
0xN31C	RxE3 TTB-0 Register – G.832	0x00





0xN31D 0x00 RxE3 TTB-1 Register - G.832 0x00 0xN31E RxE3 TTB-2 Register - G.832 0xN31F RxE3 TTB-3 Register -G.832 0x00 0xN320 0x00 RxE3 TTB-4 Register -G.832 0xN321 0x00 RxE3 TTB-5 Register -G.832 0xN322 RxE3 TTB-6 Register - G.832 0x00 0xN323 0x00 RxE3 TTB-7 Register - G.832 0xN324 0x00 RxE3 TTB-8 Register - G.832 0xN325 0x00 RxE3 TTB-9 Register – G.832 0xN326 RxE3 TTB-10 Register - G.832 0x00 0xN327 0x00 RxE3 TTB-11 Register -G.832 0xN328 0x00 RxE3 TTB-12 Register - G.832 0xN329 RxE3 TTB-13 Register - G.832 0x00 0x00 0xN32A RxE3 TTB-14 Register – G.832 0xN32B 0x00 RxE3 TTB-15 Register -G.832 0xN32C RxE3 SSM Register -G.832 0x00 0xN32D - 0xN32E 0x00 Reserved 0xN32F 0x00 RxDS3 Pattern Register 0x00 0xN330 TxDS3 Configuration Register TxE3 Configuration Register G.832 TxE3 Configuration Register - G.751 0xN331 TxDS3 FEAC Configuration and Status Register 0x00 0xN332 TxDS3 FEAC Register 0x7E 0xN333 TxDS3 LAPD Configuration Register 80x0 TxE3 LAPD Configuration Register 0xN334 TxDS3 LAPD Status/Interrupt Register 0x00 TxE3 LAPD Status/Interrupt Register 0x00 0xN335 TxDS3 M-Bit Mask Register TxE3 GC Byte Register - G.832 TxE3 Service Bits Register – G.751 0xN336 0x00 TxDS3 F-Bit Mask # 1 Register TxE3 MA Byte Register – G.832 0xN337 0x00 TxDS3 F-Bit Mask # 2 Register TxE3 NR Byte Register - G.832

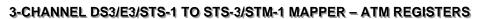
0xN338	TxDS3 F-Bit Mask # 3 Register	0x00
	TxE3 TTB-0 Register – G.832	
0xN339	TxDS3 F-Bit Mask # 4 Register	0x00
	TxE3 TTB-1 Register – G.832	
0xN33A	TxE3 TTB-2 Register – G.832	0x00
0xN33B	TxE3 TTB-3 Register – G.832	0x00
0xN33C	TxE3 TTB-4 Register – G.832	0x00
0xN33D	TxE3 TTB-5 Register – G.832	0x00
0xN33E	TxE3 TTB-6 Register – G.832	0x00
0xN33F	TxE3 TTB-7 Register – G.832	0x00
0xN340	TxE3 TTB-8 Register –G.832	0x00
0xN341	TxE3 TTB-9 Register – G.832	0x00
0xN342	TxE3 TTB-10 Register – G.832	0x00
0xN343	TxE3 TTB-11 Register – G.832	0x00
0xN344	TxE3 TTB-12 Register – G.832	0x00
0xN345	TxE3 TTB-13 Register – G.832	0x00
0xN346	TxE3 TTB-14 Register – G.832	0x00
0xN347	TxE3 TTB-15 Register –G.632	0x00
0xN348	TxE3 FA1 Error Mask Register – G.832	0x00
	TxE3 FAS Error Mask Upper Register – G.751	
0xN349	TxE3 FA2 Error Mask Register - G.832	0x00
	TxE3 FAS Error Mask Lower Register – G.751	
0xN34A	TxE3 BIP-8 Mask Register – G.832	0x00
	TxE3 BIP-4 Mask Register – G.751	
0xN34B	Tx SSB Register – G.832	0x00
0xN34C	TxDS3 Pattern Register	0x0C
0xN34D	Receive DS3/E3 AIS/PDI-P Alarm Enable Register	0x00
0xN34E	PMON Excessive Zero Count Register - MSB	0x00
0xN34F	PMON Excessive Zero Count Register- LSB	0x00
0xN350	PMON LCV Event Count Register - MSB	0x00
0xN351	PMON LCV Event Count Register - LSB	0x00
0xN352	PMON Framing Bit/Byte Error Count Register - MSB	0x00
0xN353	PMON Framing Bit/Byte Error Count Register - LSB	0x00
0xN354	PMON Parity Error Event Count Register - MSB	0x00





0xN355 0x00 PMON Parity Error Event Count Register - LSB 0xN356 0x00 PMON FEBE Event Count Register- MSB 0xN357 PMON FEBE Event Count Register - LSB 0x00 0xN358 PMON CP-Bit Error Count Register - MSB 0x00 0xN359 0x00 PMON CP-Bit Error Count Register - LSB 0xN35A PMON PLCP BIP-8 Error Count Register - MSB 0x00 0xN35B 0x00 PMON PLCP BIP-8 Error Count Register - LSB 0xN35C PMON PLCP Framing Byte Error Count Register - MSB 0x00 0xN35D 0x00 PMON PLCP Framing Byte Error Count Register – LSB 0xN35E 0x00 PMON PLCP FEBE Error Count Register - MSB 0xN35F 0x00 PMON PLCP FEBE Error Count Register - LSB 0xN360 - 0xN367 0x00 Reserved 0xN368 PMON PRBS Bit Error Count Register - MSB 0x00 0xN369 0x00 PMON PRBS Bit Error Count Register - LSB 0xN36A - 0xN36B 0x00 Reserved 0xN36C **PMON Holding Register** 0x00 0xN36D 0x00 One Second Error Status Register 0xN36E One Second - LCV Count Accumulator Register - MSB 0x00 0xN36F One Second - LCV Count Accumulator Register - LSB 0x00 0xN370 One Second - Parity Error Accumulator Register - MSB 0x00 0xN371 One Second - Parity Error Accumulator Register - LSB 0x00 0xN372 One Second - CP Bit Error Accumulator Register - MSB 0x00 0xN373 0x00 One Second - CP Bit Error Accumulator Register - LSB 0xN374 - 0xN37F 0x00 Reserved 0xN380 0x00 Reserved 0xN381 0x00 Line Interface Scan Register 0xN382 0x00 Reserved 0x00 0xN383 Transmit LAPD Byte Count Register 0xN384 0x00 Receive LAPD Byte Count Register 0xN385 - 0xN389 0x00 Reserved 0x06 0xN390 Receive PLCP Configuration and Status Register 0xN391 0x00 Receive PLCP Interrupt Enable Register 0xN392 Receive PLCP Interrupt Status Register 0x00

0xN393 – 0xN397	Reserved	0x00
0xN398	Transmit PLCP A1 Byte Error Mask Register	0x00
0xN399	Transmit PLCP A2 Byte Error Mask Register	0x00
0xN39A	Transmit PLCP BIP-8 Error Mask Register	0x00
0xN39B	Transmit PLCP G1 Byte Register	0x00
0xN39C – 0xN3AF	Reserved	0x00
0xN3B0	Transmit LAPD Memory Indirect Address Register	0x00
0xN3B1	Transmit LAPD Memory Indirect Data Register	0x00
0xN3B2	Receive LAPD Memory Indirect Address Register	0x00
0xN3B3	Receive LAPD Memory Indirect Data Register	0x00
0xN3B4 - 0xN3EF	Reserved	0x00
0xN3F0	Receive DS3/E3 Configuration Register – Secondary Frame Synchronizer Block – Byte 1	0x10
0xN3F1	Receive DS3/E3 Configuration Register Secondary Frame Synchronizer Block – Byte 0	0x10
0xN3F2	Receive DS3/E3 AIS/PDI-P Alarm Enable Register – Secondary Frame Synchronizer Block	0x00
0xN3F3 – 0xN3F7	Reserved	0x00
0xN3F8	Receive DS3/E3 Interrupt Enable Register – Secondary Frame Synchronizer Block	0x00
0xN3F9	Receive DS3/E3 Interrupt Status Register – Secondary Frame Synchronizer Block	0x00
	RECEIVE STS-3c POH PROCESSOR BLOCK	
0x1000 - 0x1181	Reserved	0x00
0x1182	Receive STS-3c Path Control Register – Byte 1	0x00
0x1183	Receive STS-3c Path – Control Register – Byte 0	0x00
0x1184 - 0x1185	Reserved	0x00
0x1186	Receive STS-3c Path – Status Register – Byte 1	0x00
0x1187	Receive STS-3c Path – Status Register – Byte 0	0x00
0x1188	Reserved	0x00
0x1189	Receive STS-3c Path – Interrupt Status Register – Byte 2	0x00
0x118A	Receive STS-3c Path – Interrupt Status Register – Byte 1	0x00
0x118B	Receive STS-3c Path – Interrupt Status Register – Byte 0	0x00
0x118C	Reserved	0x00
0x118D	Receive STS-3c Path – Interrupt Enable Register – Byte 2	0x00





0x118E	Receive STS-3c Path – Interrupt Enable Register – Byte 1	0x00
0x118F	Receive STS-3c Path – Interrupt Enable Register – Byte 0	0x00
0x1190 - 0x1192	Reserved	0x00
0x1193	Receive STS-3c Path – SONET Receive RDI-P Register	0x00
0x1194 – 0x1195	Reserved	0x00
0x1196	Receive STS-3c Path – Receive Path Label Byte (C2) Register	0x00
0x1197	Receive STS-3c Path – Expected Path Label Byte (C2) Register	0x00
0x1198	Receive STS-3c Path – B3 Error Count Register – Byte 3	0x00
0x1199	Receive STS-3c Path – B3 Error Count Register – Byte 2	0x00
0x119A	Receive STS-3c Path – B3 Error Count Register – Byte 1	0x00
0x119B	Receive STS-3c Path – B3 Error Count Register – Byte Q	0x00
0x119C	Receive STS-3c Path – REI-P Error Count Register Byte 3	0x00
0x119D	Receive STS-3c Path – REI-P Error Count Register – Byte 2	0x00
0x119E	Receive STS-3c Path – REI-P Error Count Register – Byte 1	0x00
0x119F	Receive STS-3c Path – REI-P Error Count Register – Byte 0	0x00
0x11A0 - 0x11A2	Reserved	0x00
0x11A3	Receive STS-3c Path – Receive 11 Byte Control Register	0x00
0x11A4 – 0x11A5	Reserved	0x00
0x11A6	Receive STS-3c Path – Pointer Value Register – Byte 1	0x00
0x11A7	Receive STS-3c Path Pointer Value Register – Byte 0	0x00
0x11A8 – 0x11AA	Reserved	0x00
0x11AB	Receive STS-3c Path Loss of Pointer – Concatenation Status Register	0x00
0x11AC - 0x11B2	Reserved	0x00
0x11B3	Receive STS-3c Path - AIS - Concatenation Status Register	0x00
0x11B4 – 0x11BA	Reserved	0x00
0x11BB	Receive STS-3c Path – Auto AIS Control Register	0x00
0x11BC - 0x11BE	Reserved	0x00
0x11BF	Receive STS-3c Path – Serial Port Control Register	0x00
0x11C0 - 0x11C2	Reserved	0x00
0x11C3	Receive STS-3c Path - SONET Receive Auto Alarm Register - Byte 0	0x00
0x11C4 -0x11D2	Reserved	0x00
0x11D3	Receive STS-3c Path – Receive J1 Byte Capture Register	0x00
0x11D4 - 0x11D6	Reserved	0x00

0x11D7	Receive STS-3c Path – Receive B3 Byte Capture Register	0x00
0x11D8 – 0x11DA	Reserved	0x00
0x11DB	Receive STS-3c Path – Receive C2 Byte Capture Register	0x00
0x11DC - 0x11DE	Reserved	0x00
0x11DF	Receive STS-3c Path – Receive G1 Byte Capture Register	0x00
0x11E0 - 0x11E2	Reserved	0x00
0x11E3	Receive STS-3c Path – Receive F2 Byte Capture Register	0x00
0x11E4 - 0x11E6	Reserved	0x00
0x11E7	Receive STS-3c Path – Receive H4 Byte Capture Register	0x00
0x11E8 - 0x11EA	Reserved	0x00
0x11EB	Receive STS-3c Path – Receive Z3 Byte Capture Register	0x00
0x11EC - 0x11EE	Reserved	0x00
0x11EF	Receive STS-3c Path – Receive Z4 (K3) Byte Capture Register	0x00
0x11F0 - 0x11F2	Reserved	0x00
0x11F3	Receive STS-3c Path – Receive Z5 Byte Capture Register	0x00
0x11F4 - 0x11FF	Reserved	0x00
RECEIVE	STS-3c POH Processor Block - Receive J1 (Path) Trace Message Buffer - S	STS-3c
0x1500 – 0x153F	Receive STS-3c POH Processor Block Receive J1 (Path) Trace Message Buffer	0x00
0x1540 - 0x15FF	Reserved	0x00
	TRANSMIT STS-3C POH PROCESSOR BLOCK	
0x1900 - 0x1981	Reserved	0x00
0x1982	Transmit STS-3c Path - SONET Control Register - Byte 1	0x00
0x1983	Transmit STS-3c Path - SONET Control Register- Byte 0	0x00
0x1984 - 0x1992	Reserved	0x00
0x1993	Transmit ST8-3c Path – Transmit J1 Byte Value Register	0x00
0x1994 – 0x1996	Reserved	0x00
0x1997	Transmit STS-3c Path – B3 Byte Mask Register	0x00
0x1998 – 0x199A	Reserved	0x00
0x199B	Transmit STS-3c Path – Transmit C2 Byte Value Register	0x00
0x199C - 0x199E	Reserved	0x00
0x199F	Transmit STS-3c Path – Transmit G1 Byte Value Register	0x00
0x19A0 - 0x19A2	Reserved	0x00
	Transmit STS-3c Path – Transmit F2 Byte Value Register	0x00

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

0x19A4 -0x19A6	Reserved	0x00					
0x19A7	Transmit STS-3c Path – Transmit H4 Byte Value Register	0x00					
0x19A8 - 0x19AA	Reserved	0x00					
0x19AB	Transmit STS-3c Path – Transmit Z3 Byte Value Register	0x00					
0x19AC - 0x19AE	Reserved	0x00					
0x19AF	Transmit STS-3c Path – Transmit Z4 Byte Value Register	0x00					
0x19B0 - 0x19B2	Reserved	0x00					
0x19B3	Transmit STS-3c Path – Transmit Z5 Byte Value Register	0x00					
0x19B4 - 0x19B6	Reserved	0x00					
0x19B7	Transmit STS-3c Path – Transmit Path Control Register – Byte 0	0x00					
0x19B8 - 0x19BA	Reserved	0x00					
0x19BB	Transmit STS-3c Path- Transmit J1 Byte Control Register	0x00					
0x19BC -0x19BE	Reserved	0x00					
0x19BF	Transmit STS-3c Path – Transmit Arbitrary H1 Byte Pointer Register	0x00					
0x19C0 - 0x19C2	Reserved	0x00					
0x19C3	Transmit STS-3c Path – Transmit Arbitrary H2 Byte Pointer Register	0x00					
0x19C4 - 0x19C5	Reserved	0x00					
0x19C6	Transmit STS-3c Path – Transmit Pointer Byte Register –Byte 1	0x00					
0x19C7	Transmit STS-3c Path – Transmit Pointer Byte Register – Byte 0	0x00					
0x19C8	Reserved	0x00					
0x19C9	Transmit STS-3c Path - RDI-P Control Register - Byte 2	0x00					
0x19CA	Transmit STS-3c Path RDI-P Control Register – Byte 1	0x00					
0x19CB	Transmit STS-3c Path - RDI-P Control Register - Byte 0	0x00					
0x19CC -0x19CE	Reserved	0x00					
0x19CF	Transmit STS-3@Path – Transmit Path Serial Port Control Register	0x00					
0x19D0 - 0x1AFF	Reserved	0x00					
TRANSMIT STS-3c POH PROCESSOR BLOCK – TRANSMIT J1 (PATH) TRACE MESSAGE BUFFER							
0x1D00 – 0x1D3F	Transmit STS-3c POH Processor Block –Transmit J1 (Path) Trace Message Buffer	0x00					
0x1D40 – 0x1DFF	Reserved	0x00					
L	I	I.					

1.2 THE OPERATION CONTROL BLOCK

The Operation Control Block is responsible for the following functions.

- Control of the Interrupt Structure (at the Highest Level within the XRT94L33)
- Control of the Clock Synthesizer block
- Control of the STS-3/STM-1 Telecom Bus Interface
- Control of the STS-1 Telecom Bus Interfaces

The register map for the Operation Control block is presented in the Table below. Additionally, a detailed description of each of the "Operation Control" Block registers is presented below.

1.2.1 OPERATION CONTROL BLOCK REGISTER

Table 2: Operation Control Register Address Map

Individual Register Address	Address Location	REGISTER NAME	DEFAULT VALUE
0x00	0x0100	Operation Control Register – Byte 3	0x00
0x01	0x0101	Operation Control Register Byte 2	0x00
0x02	0x0102	Reserved	0x00
0x03	0x0103	Operation Control Register Byte 0	0x00
0x04	0x0104	Operation Status Register - Byte 3 (Device ID)	0xE3
0x05	0x0105	Operation Status Register Byte 2 (Revision ID)	0x01
0x06 – 0x0A	0x0106 – 0x010A	Reserved	0x00
0x0B	0x010B	Operation Interrupt Status Register – Byte 0	0x00
0x0C - 0x0E	0x010C – 0x010E	Reserved	0x00
0x0F	0x010F	Operation Interrupt Enable Register – Byte 0	0x00
0x10 - 0x11	0x0110 - 0x0111	Reserved	0x00
0x12	0x0112	Operation Block Interrupt Status Register – Byte 1	0x00
0x13	0x0113	Operation Block Interrupt Status Register – Byte 0	0x00
0x14 - 0x15	0x0114 – 0x0115	Reserved	0x00
0x16	0x0116	Operation Block Interrupt Enable Register – Byte 1	0x00
0x17	0x0117	Operation Block Interrupt Enable Register – Byte 0	0x00
0x18 - 0x19	0x0118 – 0x0119	Reserved	0x00
0x1A	0x0111A	Reserved	0x00
0x1B	0x011B	Mode Control Register – Byte 0	0x00
0x1C - 0x1E	0x011C - 0x011E	Reserved	0x00
0x1F	0x011F	Loop-back Control Register – Byte 0	0x00

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

INDIVIDUAL REGISTER ADDRESS	Address Location	REGISTER NAME	DEFAULT VALUE
0x20	0x0120	Channel Interrupt Indicator – Receive SONET POH Processor Block	0x00
0x21	0x0121	Reserved	0x00
0x22	0x0122	Channel Interrupt Indicator – DS3/E3 framer Block	0x00
0x23	0x0123	Channel Interrupt Indicator – Receive STS-1 POH Processor Block	0x00
0x24	0x0124	Channel Interrupt Indicator – Receive STS-1 TOH Processor Block	0x00
0x25	0x0125	Reserved	0x00
0x26	0x0126	Channel Interrupt Indicator – STS-1/DS3/E3 Mapper Block	0x00
0x27	0x0127	Reserved	0x00
0x28	0x0128	Reserved	0x00
0x29	0x0129	Reserved	0x00
0x2A	0x012A	Reserved	0x00
0x2B - 0x2F	0x012B – 0x012F	Unused	0x00
0x2E	0x012E	Reserved	0x00
0x2F	0x012F	Reserved	0x00
0x30	0x0130	Reserved	0x00
0x31	0x0131	Reserved	0x00
0x32	0x0132	Interface Control Register – Byte 1	0x00
0x33	0x0133	Interface Control Register – Byte 0	0x00
0x34	0x0134	STS-3/STM-1 Telecom Bus Control Register – Byte 3	0x00
0x35	0x0135	STS-3/STM-1 Telecom Bus Control Register – Byte 2	0x00
0x36	0x0136	Reserved	0x00
0x37	0x0137	STS-3/STM-1 Telecom Bus Control Register – Byte 0	0x00
0x38	0x0138	Reserved	0x00
0x39	0x0139	Interface Control Register – Byte 2 – STS-1 Telecom Bus 2	0x00
0x3A	0x013A	Interface Control Register – Byte 1 – STS-1 Telecom Bus 1	0x00
0x3B	0x013B	Interface Control Register – Byte 0 – STS-1 Telecom Bus 0	0x00
0x3C	0x013C	Interface Control Register – STS-1 Telecom Bus Interrupt Register	0x00
0x3D	0x013D	Interface Control Register – STS-1 Telecom Bus Interrupt Status Register	0x00
0x3E	0x013E	Interface Control Register - STS-1 Telecom Bus Interrupt	0x00

0x00

0x00

0x82 - 0x93

0x94

0x0182 - 0x0193

0x0194

Reserved

APS Status Register

Rev 2.0.0

INDIVIDUAL REGISTER ADDRESS	Address Location	REGISTER NAME	DEFAULT VALUE
		Register # 2	
0x3F	0x013F	Interface Control Register – STS-1 Telecom Bus Interrupt Enable Register	0x00
0x40 - 0x45	0x0140 - 0x0145	Reserved	0x00
0x46	0x0146	Reserved	0x00
0x47	0x0147	Operation General Purpose Input/Output Register	0x00
0x48 - 0x49	0x0148 - 0x0149	Reserved	0x00
0x4A	0x014A	Reserved	0x00
0x4B	0x014B	Operation General Purpose Input/Output Direction Register	0x00
0x4C - 0x4F	0x014C – 0x014F	Reserved	0x00
0x50	0x0150	Operation Output Control Register – Byte 1	0x00
0x51 - 0x52	0x0151 -0x0152	Reserved	0x00
0x53	0x0153	Operation Output Control Register – Byte 0	0x00
0x54	0x0154	Operation Slow Speed Port Control Register – Byte 1	0x00
0x55 - 0x56	0x0155 – 0x0156	Reserved	0x00
0x57	0x0157	Operation Slow Speed Port Control Register –Byte 0	0x00
0x58	0x0158	Operation – DS3/E3/STS-1 Clock Frequency Out of Range Detection – Direction Register	0x00
0x59	0x0159	Reserved	0x00
0x5A	0x015A	Operation - DS3/E3/STS-1 Clock Frequency - DS3 Out of Range Detection Threshold Register	0x00
0x5B	0x015B	Operation - DS3/E3/STS-1 Clock Frequency - STS-1/E3 Out of Range Detection Threshold Register	0x00
0x5C	0x015C	Reserved	0x00
0x5D	0x015D	Operation – DS3/E3/STS-1 Frequency Out of Range Interrupt Enable Register – Byte 0	0x00
0x5E	0x015E	Reserved	0x00
0x5F	0x015F	Operation – DS3/E3/STS-1 Frequency Out of Range Interrupt Status Register – Byte 0	0x00
0x60 – 0x7F	0x0160 – 0x017F	Reserved	0x00
0x80	0x0180	APS Mapping Register	0x00
0x81	0x0181	APS Control Register	0x00

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

1.2.2 OPERATION CONTROL REGISTER DESCRIPTIONS

Table 3: Operation Control Register – Byte 3 (Address Location= 0x0100)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Ur	Configuration	on Control [1:0]			
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре		DESCRIPTION
Bit 7 – Bit 2	Unused	R/O	Please set to "0" for	normal operation.
Bit 1 – Bit 0	Configuration Control [1:0]	R/W	Configuration Con This READ/WRITE of the XRT94L33. The XRT94L33 ca ATM/PPP application channel DS3/E3/ST	bit-field permits the user to determine the configuration an be configured for both Mapper applications and ons. For Mapper applications, please refer to our "3-"S-1 To STS-3/STM-1 Mapper IC Datasheet". Operation Modes
	7,98	and.	01	1 PPP device. If the user set these bits to "01", the user is allowing the XRT94L33 to be configured as a 3 channel DS3/E3 ATM UNI/PPP/HDLC/Clear Channel to STS-3 device (See Figure 1)
			10	If the user set these bits to "10", the user is allowing the XRT94L33 to be configured as either a 3-channel STS-1/DS3/E3 to ATM/PPP device (See Figure 2) or as a 3 channel DS3/E3 to HDLC/CC device (See Figure 3).
			11	If the user set these bits to "11", the user is allowing the XRT94L33 to be configured as a 3 channel ATM/PPP to STS-3 device (See Figure 4).



Figure 1: Functional Block Diagram for 3-channel DS3/E3 ATM UNI/PPP to STS-3 Applications

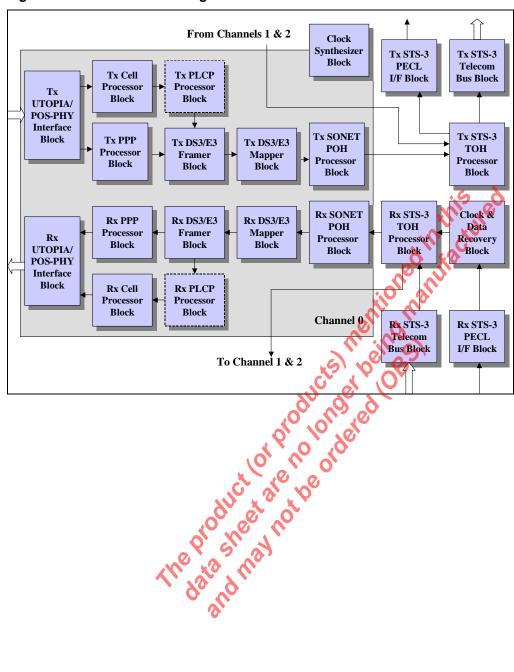


Figure 2: Functional Block Diagram for 3-channel DS3/E3/STS-1 ATM UNI/PPP Applications

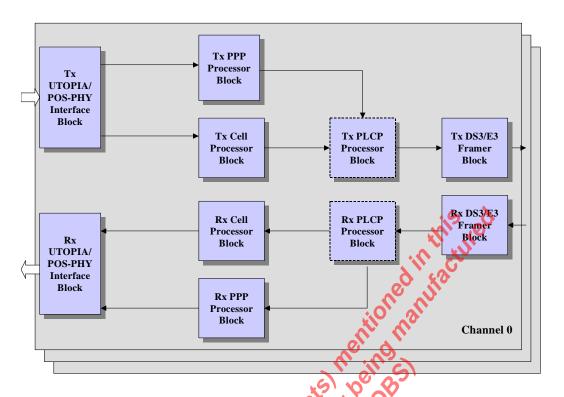


Figure 3: Functional Block Diagram for 3-channel DS3/E3 HDLC/Clear Channel Applications

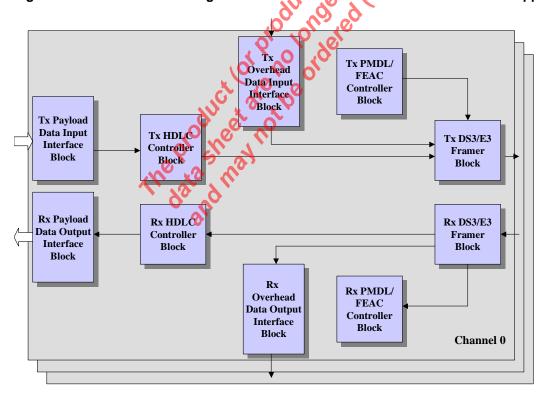


Figure 4: Functional Block Diagram for STS-3 ATM UNI/PPP Applications



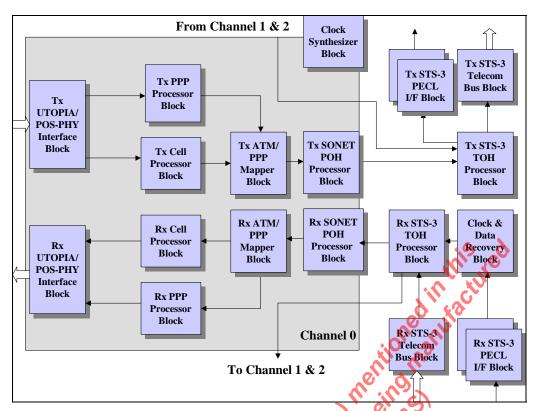


Table 4: Operation Control Register – Byte 2 (Address Location = 0x0101)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3. 🕜	Віт 2	Віт 1	Віт 0
		Unused	10	od longer	Interrupt Write Clear/RUR	Enable Interrupt Clear	Interrupt Enable
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0 0	0	0	0

		di	set not
BIT NUMBER	NAME	TYPE	DESCRIPTION
Bit 7 – Bit 3	Unused	R/O	Please set to "0" for normal operation.
Bit 2	Interrupt Write	R/W	Interrupt – Write to Clear/RUR Select:
	to Clear/RUR	S SIL	This READ/WRITE bit-field permits the user to configure all of the "Source-Level" Interrupt Status bits (within the XRT94L33) to either be "Write to Clear" (WTC) or "Reset-upon-Read" (RUR) bits.
			0 – Configures all "Source-Level" Interrupt Status register bits to function as "Reset-upon-Read" (RUR).
			1 – Configures all "Source-Level" Interrupt Status register bits to function as "Write-to-Clear" (WTC).
Bit 1	Enable Interrupt	R/W	Enable Auto-Clear of Interrupts Select:
	Clear	Clear	This READ/WRITE bit-field permits the user to configure the XRT94L33 to automatically disable all interrupts that are activated.
			0 – Configures the chip to NOT automatically disable any Interrupts following their activation.
			1 – Configures the chip to automatically disable all Interrupts following their

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			activation.
Bit 0	Interrupt Enable	R/W	Interrupt Enable:
			This READ/WRITE bit-field permits the user to configure the XRT94L33 to generate interrupt requests to the Microprocessor.
			0 – Configures the chip to NOT generate interrupt to the Microprocessor. All interrupts are disabled and the Microprocessor must poll the register bits.
			1 – Configures the chip to generate interrupts the Microprocessor.

The product are no ordered (Oss)

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 5: Operation Control Register – Byte 0 (Address Location= 0x0103)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit UTOPIA PLL OFF	Receive UTOPIA PLL OFF				PPP/ATM		SW RESET
R/W	R/W	R/O	R/O	R/O	R/W	R/O	R/W
1	1	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Transmit UTOPIA PLL OFF	R/W	.6 À
6	Receive UTOPIA PLL OFF	R/W	in this wee
5-3	Unused	R/O	89 Ha
2	PPP/ATM	R/W	PPP/ATM UNI Mode Select
			This READ-WRITE bit-field permits the user to configure the XRT94L33 to operate in either the ATM UNI or PPP Mode.
			0 – Configures the OTOPIA/POS-PHY bus to operate in the UTOPIA (ATM) Mode.
			1 - Configures the UTOPIA/POS-PHY Bus to operate in the POS-PHY Mode.
1	Unused	R/O	Please set to "0" for normal operation
Bit 0	SW	R/W	Software Reset - SONET Block:
	Reset	odu	This READ/WRITE bit-field permits the user to command a software reset to the SONET/SDH block. If the user invokes a software reset to the SONET/SDH blocks then all of the internal state machines will be reset to their default conditions; and each of the Receive STS-1/STS-3 TOH Processor blocks will undergo a re-frame operation.
	we.	6, 8	A "0" to "1" transition, within this bit-field commands this Software Reset.
		gand	This Software Reset does not reset the command registers to their default state. This can only be achieved by executing a "Hardware RESET" (e.g., by pulling the RESET_L* input pin "LOW"). This Software Reset does not affect the DS3/E3 Framer blocks. The Software Reset bit-field, for the DS3/E3 Framer block can be found in each of the 3 "DS3/E3 Operating Mode" registers (Address Location= 0xNF00).

Table 6: Operation Status Register – Byte 3 (Address Location= 0x0104)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	Device ID Value								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
1	1	1	0	0	0	1	1		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Device ID Value	R/O	Device ID Value:
			This READ-ONLY bit-field is set to the value "0xE3" and permits the user's software code to uniquely identify this device as being the XRT94L33.

Table 7: Operation Status Register – Byte 2 (Address Location ≥ 0x0105)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			Revision Nu	ımber Value			
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0 0	0	0	1

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Revision Number Value	R/O	Revision NumberValue: This READ-ONLY bit-field is set to the value that corresponds to its revision number. Revision A silicon will be set to the value "0x01". This register permits the user's software code to uniquely identify the revision number of this device.
	The production of the producti	inay in	ot be



Table 8: Operation Interrupt Status Register – Byte 0 (Address Location= 0x010B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			TB Parity Error Interrupt Status				
R/O	R/O	R/O	R/O	R/O	R/O	R/O	RUR/WTC
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
Bit 7 – Bit 1	Unused	R/O	Please set to "0" for normal operation
Bit 0	TB Parity Error Interrupt Status	RUR/ WTC	Telecom Bus Parity Error Interrupt Status: This "RESET-upon-READ" bit-field indicates whether or not the "Detection of 155.52Mbps Telecom Bus — Parity Error" interrupt has occurred since the last read of this register bit. 0 – Indicates that the "Detection of 155.52Mbps Telecom Bus — Parity Error" interrupt has NOT occurred since the last read of this register bit. 1 – Indicates that the "Detection of 155.52Mbps Telecom Bus — Parity Error" interrupt has occurred since the last of this register bit. Note: This register bit is only active if the 155.52Mbps port is configured to operate via the Telecom Bus.

Table 9: Operation Interrupt Enable Register – Byte 0 (Address Location= 0x010F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 1	Віт 0			
			Unused	No lott of		Telecom Bus Parity Error			
				16 7 70		Interrupt Enable			
R/O	R/O	R/O	R/O	R/O R/O	R/O	R/W			
0	0	0	0	00 0	0	0			
	NIC * S. * D.								

		0 0	
BIT NUMBER	NAME	TYPE	DESCRIPTION
Bit 7 – Bit 1	Unused	B)O	Please set to "0" for normal operation
Bit 0	TB Parity Error	R/W	Telecom Bus Parity Error Interrupt Enable:
	Interrupt Enable	and	This "READ/WRITE" bit-field permits the user to either enable or disable the "Detection of 155.52Mbps Telecom Bus – Parity Error" interrupt.
			0 – Disables the "Detection of 155.52Mbps Telecom Bus – Parity Error" interrupt.
			1 – Enables the "Detection of 155.52Mbps Telecom Bus – Parity Error" interrupt.
			Note: This register bit is only active if the 155.52Mbps port is configured to operate via the Telecom Bus.

Table 10: Operation Block Interrupt Status Register – Byte 1 (Address Location= 0x0112)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Op Control Block Interrupt Status	DS3/E3 Mapper Block Interrupt Status	Unused	Rx STS-1 TOH Block Interrupt Status	Rx STS-1 POH Block Interrupt Status	DS3/E3 Framer Block Interrupt Status	Rx Line Interface Block Interrupt Status	Unused
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

Віт	NAME	Түре	DESCRIPTION
NUMBER			.6 \
7	Op Control Block	R/O	Operation Control Block Interrupt Status:
	Interrupt Status		This READ-ONLY bit-field indicates whether or not an Operation Control Block-related Interrupt is awaiting Service.
			0 – No Operation Control Block Interrupts are awaiting service.
			1 – At least one "Operation Control Block" Interrupt is awaiting service.
6	DS3/E3 Mapper Block	R/O	DS3/E3 Mapper Block Interrupt Status:
	Interrupt Status		This READ-ONLY bit-field indicates whether or not a Mapper Block-related Interrupt is awaiting service.
			0 – No Mapper Block interrupt is awaiting service.
			1 – At least one "Mapper Block" Interrupt is awaiting service.
5	Unused	R/O	aro longret
4	Rx STS-1 TOH Block Interrupt Status	R/O	STS-1 Receive Transport Overhead (TOH) Processor Block Interrupt Status:
		John 2	This READ-ONLY bit-field indicates whether or not an "Receive STS-1 TOH Processor" Block Interrupt is awaiting service.
	The biod	reel	No "Receive STS-1 TOH Processor" block interrupt is awaiting service.
	The to	J. Ug	1 – At least one "Receive STS-1 TOH Processor" block interrupt is awaiting service.
	90	0	Note: This bit-field is in-active if the XRT94L33 has been configured to operate in the SDH Mode.
3	Rx STS-1 POH Block Interrupt Status	R/O	Receive STS-1 Path Overhead (POH) Processor Block Interrupt Status:
			This READ-ONLY bit-field indicates whether or not an "Receive STS-1 POH Processor" Block Interrupt is awaiting service.
			0 - No "Receive STS-1 POH Processor" block interrupt is awaiting service.
			1 – At least one "Receive STS-1 POH Processor" block interrupt is awaiting service.
			Note: This bit-field is in-active if the XRT94L33 has been configured to operate in the SDH Mode.
2	DS3/E3 Framer Block	R/O	DS3/E3 Framer Block Interrupt Status
	Interrupt Status		This READ-ONLY bit-field indicates whether or not a "DS3/E3 Framer



Rev 2.0.0

			Block" interrupt is awaiting service. 0 – No "DS3/E3 Framer" block interrupt is awaiting service. 1 – At least one "DS3/E3 Framer" block interrupt is awaiting service.
1	Rx Line Interface Block Interrupt Status	R/O	Receive Line Interface Block Interrupt Status This READ-ONLY bit-field indicates whether or not a "Receive Line Interface Block" interrupt is awaiting service. 0 – No "Receive Line Interface" block interrupt is awaiting service. 1 – At least one "Receive Line Interface" block interrupt is awaiting service.
0	Unused	R/O	Service.

The product are no ordered (OBS)

The product are no ordered (OBS)

Table 11: Operation Block Interrupt Status Register – Byte 0 (Address Location= 0x0113)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Receive ATM Cell Processor Block Interrupt Status	Receive STS-3/ STM-1 TOH Block Interrupt Status	Receive SONET/ VC-3 POH Block Interrupt Status	Receive PPP Processor Block Interrupt Status	Transmit ATM Cell Processor Block Interrupt Status	Unu	sed	Transmit PPP Processor Block Interrupt Status
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7	Receive ATM Cell	R/O	Receive ATM Cell Processor Block Interrupt Status:
	Processor Block Interrupt Status		This READ-ONLY bit-field indicates whether or not a "Receive ATM Cell Processor Block" interrupt is awaiting service.
			0 – No "Receive ATM Cell Processor Block" Interrupt is awaiting service.
			1 – At least one "Receive ATM Cell Processor Block" interrupt is awaiting service.
6	Receive	R/O	Receive STS-3/STM-1 TOH Processor Block Interrupt Status:
	STS-3/ STM-1 TOH Block		This READ-ONLY bit-field indicates whether or not a "Receive STS-3/STM-1 TOH Processor Block" interrupt is awaiting service.
	Interrupt Status		0 – No "Receive STS-3/STM-1 TOH Processor Block" Interrupt is awaiting service.
			1 – At least one "Receive STS-3/STM-1 TOH Processor Block" interrupt is awaiting service.
5	Receive	R/O	Receive SONET/VC-3 POH Processor Block Interrupt Status:
	SONET/ VC-3	the st	This READ-ONLY bit-field indicates whether or not a "Receive SONET/VC-3 POH Processor Block" interrupt is awaiting service.
	POH Block Interrupt Status		0 – No "Receive SONET/VC-3 POH Processor Block" Interrupt is awaiting service.
	Theata	9 Win	1 – At least one "Receive SONET/VC-3 POH Processor Block" Interrupt is awaiting service.
4	Receive PPP	R/O	Receive PPP Processor Block Interrupt Status:
	Processor Block Interrupt Status		This READ-ONLY bit-field indicates whether or not a "Receive PPP Processor Block" interrupt is awaiting service.
			0 – No "Receive PPP Processor Block" Interrupt is awaiting service.
			1 - At least one "Receive PPP Processor Block" interrupt is awaiting service.
3	Transmit ATM Cell	R/O	Transmit ATM Cell Processor Block Interrupt Status:
	Processor Block Interrupt Status		This READ-ONLY bit-field indicates whether or not a "Transmit ATM Cell Processor Block" interrupt is awaiting service.
			0 – No "Transmit ATM Cell Processor Block" Interrupt is awaiting service.
			1 – At least one "Transmit ATM Cell Processor Block" interrupt is awaiting service.

Rev	2.	n	n
nev	-		

2-1	Unused	R/O	
0	Transmit PPP R/O Processor Block Interrupt Status	Transmit PPP Processor Block Interrupt Status:	
			This READ-ONLY bit-field indicates whether or not a "Transmit PPP Processor Block" interrupt is awaiting service.
			0 – No "Transmit PPP Processor Block" Interrupt is awaiting service.
		1 - At least one "Transmit PPP Processor Block" Interrupt is awaiting service.	

The product are no ordered (Oss) in the product are no ordered (Oss) in the product are no ordered (Oss).

Table 12: Operation Block Interrupt Enable Register – Byte 1 (Address Location= 0x0116)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Op Control Block Interrupt Enable	DS3/E3 Mapper Block Interrupt Enable	Unused	Rx STS-1 TOH Block Interrupt Enable	Rx STS-1 POH Block Interrupt Enable	DS3/E3 Framer Block Interrupt Enable	Rx Line Interface Block Interrupt Enable	Unused
R/W	R/W	R/O	R/W	R/W	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Op Control Block Interrupt Enable	R/W	Operation Control Block Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the Operation Control Block for interrupt generation. If the user writes a "0" to this register bit and disables the "Operation Control Block" (for interrupt generation), then all "Operation Control Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "Operation Control Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 – Disable all "Operation Control Block" interrupts within the device. 1 – Enables the "Operation Control Block" at the "Block-Level" for interrupt generation
6	DS3/E3 Mapper Block Interrupt Enable	R/W	DS3/E3 Mapper Block Interrupt Enable: This READ/WRITE bit permits the user to either enable or disable the Mapper Block for interrupt generation. If the user writes a "0" to this register bit and disables the "Mapper Block" (for interrupt generation), then all "Mapper Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "Mapper Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 - Disable all "Mapper Block" interrupts within the device.
5	Unused	R/O	3
4	Rx STS-1,TQH Block Interrupt Enable	A BAN A	Receive STS-1 TOH (Transport Overhead) Processor Block Interrupt Enable: This READ/WRITE bit permits the user to either enable or disable the Receive STS-1 TOH Processor Block for interrupt generation. If the user writes a "0" to this register bit and disables the "Receive STS-1 TOH Processor Block" (for interrupt generation), then all "Receive STS-1 TOH Processor Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "Receive STS-1 TOH Processor Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 – Disable all "Receive STS-1 TOH Processor Block" interrupts within the device. 1 – Enables the "Receive STS-1 TOH Processor Block" at the "Block-Level". Note: This bit-field is inactive if the XRT94L33 has been configured to operate in the SDH Mode.
3	Rx STS-1 POH Block Interrupt	R/W	Receive STS-1 POH (Path Overhead) Processor Block Interrupt Enable: This READ/WRITE bit permits the user to either enable or disable the Receive

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

	Enable		STS-1 POH Processor Block for interrupt generation. If the user writes a "0" to this register bit and disables the "Receive STS-1 POH Processor Block" (for interrupt generation), then all "Receive STS-1 POH Processor Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "Receive STS-1 POH Processor Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 – Disable all "Receive STS-1 POH Processor Block" interrupts within the device. 1 – Enables the "Receive STS-1 POH Processor Block" at the "Block-Level". Note: This bit-field is inactive if the XRT94L33 has been configured to operate in the SDH Mode.
2	DS3/E3	R/W	DS3/E3 Framer Block Interrupt Enable:
	Framer Block Interrupt Enable		This READ/WRITE bit permits the user to either enable or disable the DS3/E3 Framer Block for interrupt generation. If the user writes a "0" to this register bit and disables the "DS3/E3 Framer Block" (for interrupt generation), then all "DS3/E3 Framer Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "DS3/E3 Framer Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 – Disable all "DS3/E3 Framer Block" interrupts within the device.
			1 – Enables the "DS3/E3 Framer Block" at the "Block-Level".
1	Rx Line Interface Block Interrupt Enable	R/W	Receive Line Interface Block Interrupt Enable: This READ/WRITE bit permits the user to either enable or disable the Receive Line Interface Block for interrupt generation. If the user writes a "0" to this register bit and disables the "Receive Line Interface Block" (for interrupt generation), then all "Receive Line Interface Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "Receive Line Interface Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 — Disable all "Receive Line Interface Block" interrupts within the device. 1 — Enables the "Receive Line Interface Block" at the "Block-Level".
0	Unused	R/0	
	*	legia	That is the interest of the interest of the block-level.

Table 13: Operation Block Interrupt Enable Register – Byte 0 (Address Location= 0x0117)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Receive ATM Cell Processor Block Interrupt Enable	Receive STS-3/ STM-1 TOH Block Interrupt Enable	Receive SONET/ VC-3 POH Block Interrupt Enable	Receive PPP Processor Block Interrupt Enable	Transmit ATM Cell Processor Block Interrupt Enable	Unu	sed	Transmit PPP Processor Block Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7	Receive ATM Cell Processor Block Interrupt Enable	R/W	Receive ATM Cell Processor Block Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Receive ATM Cell Processor Block" for interrupt generation. If the user writes a "0" to this register bit and disables the "Receive ATM Cell Processor Block" (for interrupt generation), then all "Receive ATM Cell Processor Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "Receive ATM Cell Processor Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 – Disables all "Receive ATM Cell Processor Block" interrupts within the device. 1 – Enables the "Receive ATM Cell Processor Block at the "Block Level" for interrupt generation.
6	Receive STS-3/STM-1 TOH Block Interrupt Enable	R/W Jick of Jick of Ji	Receive STS-3/STM-1 TOH Processor Block Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Receive STS-3/STM-1 TOH Processor Block" for interrupt generation. If the user writes a "0" to this register bit and disables the "Receive STS-3/STM-1 TOH Processor Block" (for interrupt generation), then all "Receive STS-3/STM-1 TOH Processor Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "Receive STS-3/STM-1 TOH Processor Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 – Disables all "Receive STS-3/STM-1 TOH Processor Block" interrupts within the device. 1 – Enables the "Receive STS-3/STM-1 TOH Processor Block" at the "Block Level" for interrupt generation.
5	Receive SONET/ VC-3 POH Block Interrupt Enable	R/W	Receive SONET/VC-3 POH Processor Block Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Receive SONET/VC-3 POH Processor Block" for interrupt generation. If the user writes a "0" into this register bit and disables the "Receive SONET/VC-3 POH Processor Block" (for interrupt generation), then all "Receive SONET/VC-3 Processor Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, then he/she will still need to enable the individual "Receive SONET/VC-3 POH Processor Block" Interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 – Disables all "Receive SONET/VC-3 POH Processor Block" Interrupts

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			within the device.
			1 – Enables the "Receive SONET/VC-3 POH Processor Block" at the "Block Level" for interrupt generation.
4	Receive PPP	R/W	Receive PPP Processor Block Interrupt Enable:
	Processor Block Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Receive PPP Processor Block" for interrupt generation. If the user writes a "0" to this register bit and disables the "Receive PPP Processor Block" (for interrupt generation), then all "Receive PPP Processor Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "Receive PPP Processor Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt.
			 0 – Disables all "Receive PPP Processor Block" interrupts within the device. 1 – Enables the "Receive PPP Processor Block" at the "Block Level" for interrupt generation.
3	Transmit ATM Cell	R/W	Transmit ATM Cell Processor Block Interrupt Enable:
	Processor Block Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Transmit ATM Cell Processor Block" for interrupt generation. If the user writes a "0" to this register bit and disables the "Transmit ATM Cell Processor Block" (for interrupt generation), then all "Transmit ATM Cell Processor Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "Transmit ATM Cell Processor Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 – Disables all "Transmit ATM Cell Processor Block" interrupts within the device. 1 – Enables the "Transmit ATM Cell Processor Block" at the "Block Level" for interrupt generation.
2 –1	Unused	R/O	of the off
0	Transmit PPP Processor Block Interrupt Enable	RAN ARAN ARAN ARAN ARAN ARAN ARAN ARAN	Transmit PPP Processor Block Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Transmit PPP Processor Block" for interrupt generation. If the user writes a "0" to this register bit and disables the "Transmit PPP Processor Block" (for interrupt generation), then all "Transmit PPP Processor Block" interrupts will be disabled for interrupt generation. If the user writes a "1" to this register bit, he/she will still need to enable the individual "Transmit PPP Processor Block" interrupt(s) at the "Source Level" in order to enable that particular interrupt. 0 — Disables all "Transmit PPP Processor Block" interrupts within the device. 1 — Enables the "Transmit PPP Processor Block" at the "Block Level" for interrupt generation.
			interrupt generation.

Table 14: Mode Control Register – Byte 0 (Address Location= 0x011B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Disable Jitter Attenuator Fast Lock	TBUS0_IS _SDH	V1_PULS E_EN	TBUS0_ MASTER		Reserved		AU-3/TUG-3* Mapping Select
R/W	R/W	R/W	R/W	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7	DISFASTLOCK	R/W	Disable Jitter Attenuator Fast lock:
			This READ/WRITE bit field is used to disable the fast lock feature for the Jitter Attenuator block
			0 – Fast Lock feature is enabled
			1 – Fast Lock feature is disabled
			Note: To configure the XRT94L33 such that it will comply with the Telcordia GR-253-CORE APS Recovery time requirements of 50ms, then the "Fast Lock" feaure MUST be enabled within the Jitter Attenuator block, by setting this bit-field to "0"
6	TBUS0_IS_SDH	R/W	Telecom Bus Coperating in SDH Mode
			This bit is used to qualify and process a Highrate SDH signal for Subrate Telecom Bus 0 operation.
			O- Clearing this bit will disable SDH format signal validation on Telecom Bus O. Subrate Telecom Bus 0 RxD[7:0] data bus ouput will be disabled.
		(0	1 Setting this bit will enable SDH format signal validation on Telecom Bus 0. It enables RxD[7:0] data bus output upon reception of a valid SDH signal format structure.
		duct	Note: This bit must be enabled in SDH mode for Subrate Telecom Bus 0 operation. This bit is ignored and does not apply in SONET mode of operation.
5	V1_PULSE_EN	R/W	V1 Pulse Enable
	The	and ma	This bit provides the option of using an additional pulse on the Telecom Drop Bus RxD_C1J1 output pin and Telecom Add Bus TxA_C1J1 pin to denote the location or onset of V1 Byte within the Synchronous Payload Envelope/Virtual Container of the SONET/SDH frame whenever the Telecom Bus is processing the Virtual Tributary Group/Virtual Container multi-frame boundary
			0 - Telecom Bus 0 in STS-3/STM-1 mode will not indicate a V1 pulse on RxD_CIJ1V1 output pin and TxA_C1J1V1 pin to indicate VT/VC multi-frame boundary.
			1 - Telecom Bus 0 in STS-3/STM-1 mode has V1 pulse added on RxD_CIJ1V1 output pin and TxA_C1J1V1 pin to indicate VT/VC multi-frame boundary
4	TBUS0_MASTER	R/W	Select Phase Timing Reference
			This bit selects TxA_C1J1V1 and TxA_PL phase timing reference when operating the Subrate Add Telecom Bus 0 in Rephase OFF mode.
			0 - Add Telecom Bus 0 timing in Slave Mode. TxA_C1J1V1 and TxA_PL pins are inputs.

			1 - Add Telecom Bus 0 timing in Master Mode. TxA_C1J1V1 and TxA_PL pins are outputs.
3 - 1	Unused	R/O	Reserved
0	AU-3/TUG-3*	R/W	AU-3/TUG-3 Mapping Select:
			This READ/WRITE bit-field is used to to specify how the DS3/E3 data, associated with Channels 0, 1 and 2 are mapped into an SDH signal, as indicated below.
			0 - DS3/E3 Channels are mapped into a VC-3, a TU-3, and then finally a TUG-3 structure, when being mapped into an STM-1 signal.
			1 – DS3/E3 Channels are mapped into a VC-3 and then an AU-3 when being mapped into an STM-1 signal.
			Note: This register bit is only active if the XRT94L33 has been configured to operate in the SDH Mode.
		datand	Note: This register bit is only active if the XRT94L33 has been configured to operate in the SDH Mode: The SDH Mode of the SDH

Table 15: Loop-back Control Register – Byte 0 (Address Location= 0x011F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Unu	sed		Loop-back[3:0]				
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре		DESCRIPTION
7 - 4	Unused	R/O		
3 - 0	Loop-back[3:0]	R/W	Loop-back Mode[3:	0]
				VRITE bits-fields permit the user to configure the te in a variety of loop-back modes, as is tabulated
			Loop-back[3:0]	Resulting Loop-back Mode
			0000	Normal Mode (e.g., No Loop-back Mode)
			0001	Remote Line Loop-back:
			Menth	In this mode, all data that is received by the "Receive STS-3/STM-1 PECL Interface" block will be routed to the "Transmit STS-3/STM-1 PECL Interface" block.
		তে	roducts ment	Note: If the user invokes this loop-back, then he/she must configure the Transmit STS-3/STM-1 PECL Interface to operate in the Loop-timing mode by setting Bit 6 within the Receive Line Interface Control Register – Byte 1, to "1" (Address Location: 0x0302).
		C.V.	0010	Local Transport Loop-back:
	Thedata	heet?	ot	In this mode, all data that is being output via the "Transmit STS-3 TOH Processor" block will also be routed to the "Receive STS-3 TOH Processor" block.
	Theoris	111	0011	Local Path Loop-back:
	, 90	O		In this mode, all data that is output by the Transmit SONET POH Processor block (e.g., towards the "Transmit STS-3 TOH Processor" block) will be routed to the "Receive SONET POH Processor" block.
				Note: This mode effect all 3 Transmit SONET POH Processor and Receive SONET POH Processor blocks.
			0100 - 1111	Reserved – Do Not Use

EXAR

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 16: Channel Interrupt Indicator – Receive SONET POH Processor Block (Address Location= 0x0120)

Віт 7	Віт 6	Віт 5	Віт 4 Віт 3		Віт 2	Віт 1	Віт 0
Unused			Rx STS-3c Rx SDH POH Block Interrupt		Rx SONET POH Block Interrupt Ch 2	Rx SONET POH Block Interrupt Ch 1	Rx SONET POH Block Interrupt Ch 0
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7-5	Unused		"his red
4	Rx STS-3c POH	R/O	Receive STS-3c POH Processor Block Interrupt:
	Block Interrupt		This READ/ONLY bit-field indicates whether or not the "Receive STS-3c POH Processor" block, associated with Channel 0 is declaring an Interrupt, as described below.
			0 – The Receive STS-3c POH Processor block, associated with Channel 0 is NOT declaring an Interrupt.
			1 – The Receive STS-3c POH Processor block, associated with Channel 0 is currently declaring an Interrupt
			Note: This register bit is only active if the XRT94L33 has been configured to support an STS-3c signal via Channel 0.
3	Rx SDH POH	R/O	Receive SDH POH Processor Block Interrupt:
	Block Interrupt		This READ/ONLY bit-field indicates whether or not the "Receive SDH POH Processor" block, associated with Channel 3 is declaring an Interrupt, as described below
		10	0 – The Receive SDH POH Processor block, associated with Channel 3 is NOT declaring an Interrupt.
		orock	14 The Receive SDH POH Processor block, associated with Channel 3 is currently declaring an interrupt.
2	Rx SONET POH	R/O	Receive SONET POH Processor Block Interrupt – Channel 2:
	Block Interrupt Channel 2	datand	This READ/ONLY bit-field indicates whether or not the "Receive SONET POH Processor" block, associated with Channel 2 is declaring an Interrupt, as described below.
			0 – The Receive SONET POH Processor block, associated with Channel 2 is NOT declaring an Interrupt.
			1 – The Receive SONET POH Processor block, associated with Channel 2 is currently declaring an interrupt.
1	Rx SONET POH	R/O	Receive SONET POH Processor Block Interrupt – Channel 1:
	Block Interrupt Channel 1		This READ/ONLY bit-field indicates whether or not the "Receive SONET POH Processor" block, associated with Channel 1 is declaring an Interrupt, as described below.
			0 – The Receive SONET POH Processor block, associated with Channel 9 is NOT declaring an Interrupt.
			1 – The Receive SONET POH Processor block, associated with Channel 9 is currently declaring an interrupt.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

0	Rx SONET POH	R/O	Receive SONET POH Processor Block Interrupt :
	Block Interrupt Channel 0	•	This READ/ONLY bit-field indicates whether or not the "Receive SONET POH Processor" block, associated with Channel 0 is declaring an Interrupt, as described below.
			0 – The Receive SONET POH Processor block, associated with Channel 0 is NOT declaring an Interrupt.
		1 – The Receive SONET POH Processor block, associated with Channel 0 is currently declaring an interrupt.	

The product of products mentioned in this are no ordered (OBS)

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 17: Channel Interrupt Indicator – DS3/E3 Framer Block (Address Location= 0x0122)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Unused	DS3/E3 Framer Block Interrupt Ch 2	DS3/E3 Framer Block Interrupt Ch 1	DS3/E3 Framer Block Interrupt Ch 0		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 –3	Unused	R/O	
2	DS3/E3 Framer Block Interrupt Ch 2	R/O	DS3/E3 Framer Block Interrupt – Channel 2: This READ/ONLY bit-field indicates whether or not the "DS3/E3 Framer" block, associated with Channel 2 is declaring an Interrupt, as described below. 0 – The DS3/E3 Framer block, associated with Channel 2 is NOT declaring an Interrupt. 1 – The DS3/E3 Framer block, associated with Channel 2 is currently declaring an interrupt.
1	DS3/E3 Framer Block Interrupt Ch 1	R/O	DS3/E3 Framer Block Interrupt – Channel 1: This READ/ONLY bit-field indicates whether or not the "DS3/E3 Framer" block, associated with Channel 1 is declaring an Interrupt, as described below. 0 – The DS3/E3 Framer block, associated with Channel 1 is NOT declaring an Interrupt. 1 – The DS3/E3 Framer block, associated with Channel 1 is currently declaring an interrupt.
0	DS3/E3 Framer Block Interrupt Ch 0	R/O Production	DS3/E3 Framer Block Interrupt – Channel 0: This READ/ONLY bit-field indicates whether or not the "DS3/E3 Framer" block, associated with Channel 0 is declaring an Interrupt, as described below. 0.2 The DS3/E3 Framer block, associated with Channel 0 is NOT declaring an Interrupt. 1 – The DS3/E3 Framer block, associated with Channel 0 is currently declaring an interrupt.

Table 18: Channel Interrupt Indicator – Receive STS-1 POH Processor Block (Address Location= 0x0123)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Unused	Rx STS-1 POH Block Interrupt Ch 2	Rx STS-1 POH Block Interrupt Ch 1	Rx STS-1 POH Block Interrupt Ch 0		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 3	Unused	R/O	
2	Rx STS-1 POH Block Interrupt Channel 2	R/O	Receive STS-1 POH Processor Block Interrupt – Channel 2: This READ/ONLY bit-field indicates whether or not the "Receive STS-1 POH Processor" block, associated with Channel 2 is declaring an Interrupt, as described below. 0 – The Receive STS-1 POH Processor block, associated with Channel 2 is NOT declaring an Interrupt. 1 – The Receive STS-1 POH Processor block, associated with Channel 2 is currently declaring an interrupt.
1	Rx STS-1 POH Block Interrupt Channel 1	R/O	Receive STS-1 POH Processor Block Interrupt – Channel 1: This READ/ONLY bit-field indicates whether or not the "Receive STS-1 POH Processor" block, associated with Channel 1 is declaring an Interrupt, as described below. 0 – The Receive STS-1 POH Processor block, associated with Channel 1 is NOT declaring an Interrupt. 1 – The Receive STS-1 POH Processor block, associated with Channel 1 is currently declaring an interrupt.
0	Rx STS-1 POH Block Interrupt Channel 0	d Root	Receive STS-1 POH Processor Block Interrupt – Channel 0: This READ/ONLY bit-field indicates whether or not the "Receive STS-1 POH Processor" block, associated with Channel 0 is declaring an Interrupt, as described below. 0 – The Receive STS-1 POH Processor block, associated with Channel 0 is NOT declaring an Interrupt. 1 – The Receive STS-1 POH Processor block, associated with Channel 0 is currently declaring an interrupt.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 19: Channel Interrupt Indicator – Receive STS-1 TOH Processor Block (Address Location= 0x0124)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Unused		Rx STS-1 TOH Block Interrupt Ch 2	Rx STS-1 TOH Block Interrupt Ch 1	Rx STS-1 TOH Block Interrupt Ch 0	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 3	Unused	R/O	
2	Rx STS-1 TOH Block Interrupt Channel 2	R/O	Receive STS-1 TOH Processor Block Interrupt – Channel 2: This READ/ONLY bit-field indicates whether or not the "Receive STS-1 TOH Processor" block, associated with Channel 2 is declaring an Interrupt, as described below. 0 – The Receive STS-1 TOH Processor block, associated with Channel 2 is NOT declaring an Interrupt 1 – The Receive STS-1 TOH Processor block, associated with Channel 2 is currently declaring an interrupt.
1	Rx STS-1 TOH Block Interrupt Channel 1	R/O	Receive STS-1 TOH Processor Block Interrupt – Channel 1: This READ/ONLY bit-field indicates whether or not the "Receive STS-1 TOH Processor" block, associated with Channel 1 is declaring an Interrupt, as described below. 0 – The Receive STS-1 TOH Processor block, associated with Channel 1 is NOT declaring an Interrupt. 1 – The Receive STS-1 TOH Processor block, associated with Channel 1 is currently declaring an interrupt.
0	Rx STS-1 TOH Block Interrupt Channel 0	R/Q1)	Receive STS-1 TOH Processor Block Interrupt – Channel 0: This READ/ONLY bit-field indicates whether or not the "Receive STS-1 TOH Processor" block, associated with Channel 0 is declaring an Interrupt, as described below. 0 – The Receive STS-1 TOH Processor block, associated with Channel 0 is NOT declaring an Interrupt. 1 – The Receive STS-1 TOH Processor block, associated with Channel 0 is currently declaring an interrupt.

Table 20: Channel Interrupt Indicator -DS3/E3 Mapper Block (Address Location= 0x0126)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused					DS3/E3	DS3/E3
						Mapper Block Interrupt Ch 1	Mapper Block Interrupt Ch 0
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 3	Unused	R/O	
2	DS3/E3 Mapper Block Interrupt Channel 2	R/O	DS3/E3 Mapper Block Interrupt – Channel 2: This READ/ONLY bit-field indicates whether or not the "DS3/E3 Mapper" block, associated with Channel 2 is declaring an Interrupt, as described below. 0 – The DS3/E3 Mapper block, associated with Channel 2 is NOT declaring an Interrupt. 1 – The DS3/E3 Mapper block, associated with Channel 2 is currently
1	DS3/E3 Mapper Block Interrupt Channel 1	R/O	DS3/E3 Mapper Block Interrupt – Channel 1: This READ/ONLY bit-field indicates whether or not the "DS3/E3 Mapper" block, associated with Channel 1 is declaring an Interrupt, as described below. 0 – The DS3/E3 Mapper block, associated with Channel 1 is NOT declaring an Interrupt. 1 – The DS3/E3 Mapper block, associated with Channel 1 is currently declaring an interrupt.
0	DS3/E3 Mapper Block Interrupt Channel 0	ROSHR	DS3/E3 Mapper Block Interrupt – Channel 0: This READ/ONLY bit-field indicates whether or not the "DS3/E3 Mapper" block, associated with Channel 0 is declaring an Interrupt, as described below. 0 – The DS3/E3 Mapper block, associated with Channel 0 is NOT declaring an Interrupt. 1 – The DS3/E3 Mapper block, associated with Channel 0 is currently declaring an interrupt.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 21: Channel Interrupt Indicator –Transmit ATM Cell Processor Block (Address Location= 0x0127)

Віт 7	Віт 6	Віт 5 Віт 4 Віт 3		Віт 2	Віт 1	Віт 0	
Unused				Transmit ATM Cell Processor Block Interrupt Ch 2	Transmit ATM Cell Processor Block Interrupt Ch 1	Transmit ATM Cell Processor Block Interrupt Ch 0	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 3	Unused	R/O	,s &
2	Transmit ATM Cell Processor Block Interrupt Channel 2	R/O	Transmit ATM Cell Processor Block Interrupt – Channel 2: This READ/ONLY bit-field indicates whether or not the "Transmit ATM Cell Processor Block", associated with Channel 2 is declaring an Interrupt, as described below. 0 – The transmit ATM Cell Processor Block, associated with Channel 2 is NOT declaring an Interrupt. 1 – The transmit ATM Cell Processor Block, associated with Channel 2 is currently declaring an interrupt.
1	Transmit ATM Cell Processor Block Interrupt Channel 1	R/O	Transmit ATM Cell Processor Block Interrupt – Channel 1: This READ/ONLY bit-field indicates whether or not the "Transmit ATM Cell Processor Block", associated with Channel 1 is declaring an Interrupt, as described below. 0 – The transmit ATM Cell Processor Block, associated with Channel 1 is NOT declaring an Interrupt. 1 – The transmit ATM Cell Processor Block, associated with Channel 1 is currently declaring an interrupt.
0	Transmit ATM Cell Processor Block Interrupt Channel 0	R/ON Atand	Transmit ATM Cell Processor Block Interrupt – Channel 0: This READ/ONLY bit-field indicates whether or not the "Transmit ATM Cell Processor Block" associated with Channel 0 is declaring an Interrupt, as described below. 0 – The transmit ATM Cell Processor Block, associated with Channel 0 is NOT declaring an Interrupt. 1 – The transmit ATM Cell Processor Block, associated with Channel 0 is currently declaring an interrupt.

Table 22: Channel Interrupt Indicator – Receive ATM Cell Processor Block (Address Location= 0x0128)

Віт 7	Віт 6	Віт 5 Віт 4 Віт 3		Віт 2	Віт 1	Віт 0	
	Unused				Receive ATM Cell Processor Block Interrupt Ch 2	Receive ATM Cell Processor Block Interrupt Ch 1	Receive ATM Cell Processor Block Interrupt Ch 0
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 3	Unused	R/O	
2	Receive ATM Cell Processor Block Interrupt Channel 2	R/O	Receive ATM Cell Processor Block Interrupt – Channel 2: This READ/ONLY bit-field indicates whether or not the "Receive ATM Cell Processor Block", associated with Channel 2 is declaring an Interrupt, as described below. 0 – The Receive ATM Cell Processor Block, associated with Channel 2 is NOT declaring an Interrupt. 1 – The Receive ATM Cell Processor Block, associated with Channel 2 is currently declaring an interrupt.
1	Receive ATM Cell Processor Block Interrupt Channel 1	R/O	Receive ATM Cell Processor Block Interrupt – Channel 1: This READ/ONLY bit-field indicates whether or not the "Receive ATM Cell Processor Block", associated with Channel 1 is declaring an Interrupt, as described below. 0 – The Receive ATM Cell Processor Block, associated with Channel 1 is NOT declaring an Interrupt. 1 – The Receive ATM Cell Processor Block, associated with Channel 1 is currently declaring an interrupt.
0	Receive ATM Cell Processor Block Interrupt Channel 0	d die	This READ/ONLY bit-field indicates whether or not the "Receive ATM Cell Processor Block" associated with Channel 0 is declaring an Interrupt, as described below. 0 – The Receive ATM Cell Processor Block, associated with Channel 0 is NOT declaring an Interrupt. 1 – The Receive ATM Cell Processor Block, associated with Channel 0 is currently declaring an interrupt.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 23: Channel Interrupt Indicator – Transmit PPP Processor Block (Address Location= 0x0129)

Віт 7	Віт 6	Віт 5 Віт 4 Віт 3		Віт 2	Віт 1	Віт 0	
Unused				Transmit PPP Processor Block Interrupt Ch 2	Transmit PPP Processor Block Interrupt Ch 1	Transmit PPP Processor Block Interrupt Ch 0	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 3	Unused	R/O	
2	Transmit PPP Processor Block Interrupt Channel 2	R/O	Transmit PPP Processor Block Interrupt – Channel 2: This READ/ONLY bit-field indicates whether or not the "Transmit PPP Processor Block", associated with Channel 2 is declaring an Interrupt, as described below. 0 – The Transmit PPP Processor Block, associated with Channel 2 is NOT declaring an Interrupt. 1 – The Transmit PPP Processor Block, associated with Channel 2 is currently declaring an interrupt.
1	Transmit PPP Processor Block Interrupt Channel 1	R/O	Transmit PPP Processor Block Interrupt – Channel 1: This READ/ONLY bit field indicates whether or not the "Transmit PPP Processor Block", associated with Channel 1 is declaring an Interrupt, as described below. 0 – The Transmit PPP Processor Block, associated with Channel 1 is NOT declaring an Interrupt. 1 The Transmit PPP Processor Block, associated with Channel 1 is currently declaring an interrupt.
0	Transmit PPP Processor Block Interrupt Channel 0	R/OU	Transmit PPP Processor Block Interrupt – Channel 0: This READ/ONLY bit-field indicates whether or not the "Transmit PPP Processor Block" associated with Channel 0 is declaring an Interrupt, as described below. O – The Transmit PPP Processor Block, associated with Channel 0 is NOT declaring an Interrupt. 1 – The Transmit PPP Processor Block, associated with Channel 0 is currently declaring an interrupt.

Table 24: Channel Interrupt Indicator –Receive PPP Processor Block (Address Location= 0x012A)

Віт 7	Віт 6	Віт 5 Віт 4 Віт 3		Віт 2	Віт 1	Віт 0	
	Unused				Receive PPP Processor Block Interrupt Ch 2	Receive PPP Processor Block Interrupt Ch 1	Receive PPP Processor Block Interrupt Ch 0
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 3	Unused	R/O	
2	Receive PPP Processor Block Interrupt Channel 2	R/O	Receive PPP Processor Block Interrupt — Channel 2: This READ/ONLY bit-field indicates whether or not the "Receive PPP Processor Block", associated with Channel 2 is declaring an Interrupt, as described below. 0 — The Receive PPP Processor Block, associated with Channel 2 is NOT declaring an Interrupt. 1 — The Receive PPP Processor Block, associated with Channel 2 is currently declaring an interrupt.
1	Receive PPP Processor Block Interrupt Channel 1	R/O	Receive PPP Processor Block Interrupt – Channel 1: This READ/ONLY bit-field indicates whether or not the "Receive PPP Processor Block", associated with Channel 1 is declaring an Interrupt, as described below. 0 – The Receive PPP Processor Block, associated with Channel 1 is NOT declaring an Interrupt. 1 – The Receive PPP Processor Block, associated with Channel 1 is currently declaring an interrupt.
0	Receive PPP Processor Block Interrupt Channel 0	d die	Receive PPP Processor Block Interrupt – Channel 0: This READ/ONLY bit-field indicates whether or not the "Receive PPP Processor Block" associated with Channel 0 is declaring an Interrupt, as described below. 0 – The Receive PPP Processor Block, associated with Channel 0 is NOT declaring an Interrupt. 1 – The Receive PPP Processor Block, associated with Channel 0 is currently declaring an interrupt.

EXAR

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 25: Interface Control Register – Byte 1 (Address Location= 0x0132)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unu	ısed	Receive STS-3/STM-1 Line Select[1:0]		Unused		Transmit STS Selec	-3/STM-1 Line ct[1:0]
R/O	R/O	R/W	R/W	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 6	Unused	R/O	
5 – 4	Receive STS- 3/STM-1 Line Select[1:0]	R/W	Receive STS-3/STM-1 Line Select[1:0]: These two READ/WRITE bit-fields permit the user to configure the Receive STS-3 TOH Processor block to either accept its STS-3/STM-1 data from the Receive STS-3/STM-1 Telecom Bus Interface, or from the Receive STS-3/STM-1 PECL Interface. 0, 0 – Configures the Receive STS-3 TOH Processor block to accept the incoming STS-3/STM-1 data via the Receive STS-3/STM-1 PECL Interface block 0, 1 – Configures the Receive STS-3 TOH Processor block to accept the incoming STS-3/STM-1 data via the Receive STS-3/STM-1 Telecom Bus Interface block 1, 0 and 1, 1 – Do not use
3 – 2	Unused	R/O	ucier O
1 – 0	Transmit STS- 3/STM-1 Line Select[1:0]	P/W	Transmit STS-3/STM-1 Line Select[1:0]: These two READ/WRITE bit-fields permit the user to configure the Transmit STS-3 TOH Processor block to output its outbound STS-3/STM-1 data to either the Transmit STS-3/STM-1 Telecom Bus Interface, or to the Transmit STS-3/STM-1 PECL Interface. 0, 0 - Configures the Transmit STS-3 TOH Processor block to output the outbound STS-3/STM-1 data via the Transmit STS-3/STM-1 PECL Interface block 0, 1 - Configures the Transmit STS-3 TOH Processor block to output the outbound STS-3/STM-1 data via the Transmit STS-3/STM-1 Telecom Bus Interface block 1, 0 and 1, 1 - Do not use.

Table 26: Interface Control Register – Byte 0 (Address Location= 0x0133)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SBSYNC_Delay[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION			
7 – 0	SBSYNC_Delay[7:0]	R/W	STS-1 Telecom Bus – Sync Delay:			
			The Transmit STS-1 Telecom Bus is aligned to the "TxSBFP_in" input pin.			
			The user is expected to apply a pulse (with the period of a 6.48MHz clock signal) at a rate of 8kHz to the "TxSBFP in input (pin number G4). Each Transmit STS-1 Telecom Bus will align its transmission of the very first byte of a new STS-1 frame, with a pulse at this input pin.			
			These READ/WRITE bit-fields permit the user to specify the amount of delay (in terms of 6.48MHz clock periods) that will exist between the rising edge of "TxSBFP_in" and the transmission of the very first byte, within a given STS-1 via the Transmit STS-1 Telecom Bus.			
			Setting this register to "0x00" configures each of the Transmit STS-1 Telecom Bus Interfaces to transmit the very first byte of a new STS-1 frame, upon detection of the rising edge of the "TxSBFP_in".			
			Setting this register to "0x01" configures each of the Transmit STS-1 Telecom Bus Interfaces to delay its transmission of the very first byte of a new STS-1 frame, by one 6.48MHz clock period, and so on.			
			Note: This register is only active if at least one of the three STS-1 Telecom Bus Interfaces are enabled.			
	Note: This register is only active if at least one of the three S					

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 27: STS-3/STM-1 Telecom Bus Control Register – Byte 3 (Address Location= 0x0134)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
HRSYNC_Delay[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	HRSYNC_Delay[15:8]	R/W	STS-3 Telecom Bus – Sync Delay – Upper Byte:
			The Transmit STS-3 Telecom Bus is aligned to the "TxSBFP_in" input pin.
			The user is expected to apply a pulse (with the period of a 6.48MHz clock signal) at a rate of 8kHz to the "TxSBFP_in input (pin number G4). The Transmit STS-3/STM-1 Telecom Bus will align its transmission of the very first byte of a new STS-3/STM-1 frame, with a pulse at this input pin.
			These READ/WRITE bit-fields permit the user to specify the amount of delay (in terms of 19.44MHz clock periods) that will exist between the rising edge of "TxSBFP_in" and the transmission of the very first byte, within a given STS-3 via the Transmit STS-3/STM-1 Telecom Bus.
			Setting these two registers to "0x0000" configures each of the Transmit STS-3/STM-1 Telecom Bus Interfaces to transmit the very first byte of a new STS-3 frame, upon detection of the rising edge of the "TxSBFP_in".
			Setting these register to "0x0001" configures each of the Transmit STS-3 Telecom Bus Interfaces to delay its transmission of the very first byte of a new STS-3 frame, by one 19.44MHz clock period, and so on.
		(Note: This register is only active if the STS-3/STM-1 Telecom Bus Interfaces is enabled.
	The day	aduct and man	Note: This register is only active if the STS-3/STM-1 Telecom Bus Interfaces is enabled.

Table 28: STS-3/STM-1 Telecom Bus Control Register – Byte 2 (Address Location= 0x0135)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
HRSYNC_Delay[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	HRSYNC_Delay[7:0]	R/W	STS-3 Telecom Bus – Sync Delay – Lower Byte:
			The Transmit STS-3 Telecom Bus is aligned to the "TxSBFP_in" input pin.
			The user is expected to apply a pulse (with the period of a 6.48MHz clock signal) at a rate of 8kHz to the "TxSBFP_in input (pin number G4). The Transmit STS 3/STM-1 Telecom Bus will align its transmission of the very first byte of a new STS-3/STM-1 frame, with a pulse at this input pin.
			These READ/WRITE bit-fields (along with that within the "Interface Control Register – Byte 3) permit the user to specify the amount of delay (in terms of 19.44MHz clock periods) that will exist between the rising edge of "TxSBFP_in" and the transmission of the very first byte, within a given STS-3 via the Transmit STS-3/STM-1 Telecom Bus.
			Setting this register to "0x0000" configures each of the Transmit STS-3/STM-1 Telecom Bus Interfaces to transmit the very first byte of a new STS-3 frame, upon detection of the rising edge of the "TxSBFP_in".
			Setting this register to "0x0001" configures each of the Transmit STS-3 Telecom Bus Interfaces to delay its transmission of the very first byte of a new STS-3 frame, by one 19.44MHz clock period, and so on.
		lot	Note: This register is only active if the STS-3/STM-1 Telecom Bus Interfaces is enabled.
	The produ	inay n	othe



Table 29: STS-3/STM-1 Telecom Bus Control Register – Byte 0 (Address Location= 0x0137)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Telecom Bus ON	Telecom Bus Disable	Is STS-3 Payload	Telecom Bus Parity Type	Telecom Bus J1 Only	Telecom Bus Parity Odd	Telecom Bus Parity Disable	STS-3 Rephase OFF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
Bit 7	Telecom Bus ON	R/W	Telecom Bus Enable:
			This READ/WRITE permits the user to either enable or disable the 155.52Mbps Telecom Bus Interface.
			0 – Telecom Bus Interface is Disabled:
			STS-3/STM-1 data will output via "Interleave/De-Interleave" or "Clock/Data" Interface.
			1 – Telecom Bus Interface is Enabled:
			In this selection, the STS-3/STM-1 Transmit and Receive Telecom Bus Interface will be enabled.
Bit 6	Telecom Bus Tri-	R/W	Telecom Bus Tri-state.
	State		This READ/WRITE bit-field permits the user to "tri-state" the Telecom Bus Interface.
			0 – Telecom Bus Interface is NOT tri-stated.
			1 – Telecom Bus Interface is tri-stated.
			Note: This READ/WRITE bit-field is ignored if the STS-3/STM-1 Transmit and Receive Telecom Bus Interface is disabled.
Bit 5	Is STS-3 Payload	R/W	Is STS-3 Payload:
		odu	This READ/WRITE bit-field permits the user to enable Telecom bus 0 to handle complete STS-3 payload
		1 3/1	0+ All three buses are enabled
	The	10	T – Telecom Bus 0 is enabled to handle complete STS-3 payload, the other two buses are not used.
Bit 4	Telecom Bus	R/W	Telecom Bus Parity Type:
	Parity Type		This READ/WRITE bit-field permits the user to define the parameters, over which "Telecom Bus" parity will be computed.
			0 - Parity is computed/verified over the STS-3/STM-1 Transmit and Receive Telecom Bus - data bus pins (e.g., TXA_D[7:0] and RXD_D[7:0]).
			If the user implements this selection, then the following will happen.
			a. The STS-3/STM-1 Transmit Telecom Bus Interface will compute and output parity (via the "TXA_DP" output pin) based upon and coincident with the data being output via the "TXA_D[7:0]" output pins.
			b. The STS-3/STM-1 Receive Telecom Bus Interface will compute and verify the parity data (which is input via the "RXD_DP" input pin) based upon the data which is being input (and latched) via

		1		the "RXD_D[7:0]" input pins.
			Receive	ity is computed/verified over the STS-3/STM-1 Transmit and Telecom Bus – data bus pins (e.g., TXA_D[7:0] and 7:0]); the C1J1 and PL input/output pins.
			If the use	er implements this selection, then the following will happen.
				The STS-3/STM-1 Transmit Telecom Bus Interface will compute and output parity (via the "TXA_DP" output) based upon and coincident with (1) the data being output via the "TXA_D[7:0]" output pins, (2) the state of the "TXA_PL" output pin, and (3) the state of the "TXA_C1J1" output pin.
				The STS-3/STM-1 Transmit Telecom Bus Interface will compute and verify the parity data (which is input via the "RXD_DP" input pin) based upon (1) the data which is being input (and latched) via the "RXD_D[7:0]" input pins, (2) the state of the "RXD_PL" input pin, and (3) the state of the "RXD_C1J1" input pin.
			Note:	This bit-field is disabled if the STS-3/STM-1 Telecom Bus is disabled. The user can configure the STS-3/STM-1 Telecom Bus to compute with either even or odd parity, by writing the appropriate data into Bit 2 (Telecom Bus Parity – Odd), within this register.
Bit 3	Telecom Bus J1	R/W	Telecom	Bus - J1 Indicator Only:
	Only		3/STM-1 "TXA_C1	AD/WRITE bit-field permits the user to configure how the STS- Transmit and Receive Telecom Bus interface handles the J1" and RXD_C1J1" signals, as described below.
			0 - C1 at	nd J1 Bytes
			This sele	ction configures the following.
		4	4, 10	The STS-3/STM-1 Transmit Telecom Bus to pulse the "TXA_C1J1" output coincident to whenever the C1 and J1 bytes are being output via the "TXA_D[7:0]" output pins.
		10, 5	ie be	The STS-3/STM-1 Receive Telecom Bus will expect the "RXD_C1J1" input to pulse "high" coincident to whenever the C1 and J1 bytes are being sampled via the "RXD_D[7:0]" input pins.
	6	0	15 J1 By	ytes Only
	de	100	This sele	ction configures the following.
	Thelata	qua		The STS-3/STM-1 Transmit Telecom Bus Interface to only pulse the "TXA_C1J1" output pin coincident to whenever the J1 byte is being output via the "TXA_D[7:0]" output pins.
	8		Note:	The "TXA_C1J1" output pin will NOT be pulsed "high" whenever the C1 byte is being output via the "TXA_D[7:0]" output pins
				The STS-3/STM-1 Receive Telecom Bus Interface will expect the "RXD_C1J1" input to only pulse "high" coincident to whenever the J1 byte is being sampled via the "RXD_D[7:0]" input pins.
			Note:	The "RXD_C1J1" input pin will NOT be pulsed "high" whenever the C1 byte is being input via the "RXD_D[7:0]" input pins
Bit 2	Telecom Bus	R/W	Telecom	Bus Parity – ODD Parity Select:
	Parity Odd			AD/WRITE bit-field permits the user to configure the STS-3/STMm Bus Interface to do the following.
			In the Tr	ansmit (Drop) Direction
				S-3/STM-1 Telecom Bus to compute either the EVEN or ODD ver the contents of the (1) TxD_D[7:0] output pins, or (2)

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			TxD_D[7:0] output pins, the states of the TxD_PL and TxD_C1J1 output pins (depending upon user setting for Bit 3).
			In the Receive (Add) Direction
			Receive STS-3/STM-1 Telecom Bus to compute and verify the EVEN or ODD parity over the contents of the (1) RxA_D[7:0] input pins, or (2) RxA_D[7:0] input pins, the states of the RxA_PL and RxA_C1J1 input pins (depending upon user setting for Bit 3).
			0 – Configures Transmit (Drop) Telecom Bus to compute EVEN parity and configures the Receive (Add) Telecom Bus to verify EVEN parity.
			1 – Configures Transmit (Drop) Telecom Bus to compute ODD parity and configures the Receive (Add) Telecom Bus to verify ODD parity.
Bit 1	Telecom Bus	R/W	Telecom Bus Parity Disable:
	Parity Disable		This READ/WRITE bit-field permits the user to either enable or disable parity calculation and placement via the "TxA_DP" output pin. This bit field also permits the user to enable or disable parity verification by the Receive Telecom Bus.
			0 - Enables Parity Calculation (on the Transmit Telecom Bus) and Disables Parity Verification (on the Receive Telecom Bus.
			1 – Disables Parity Calculation and Verification
Bit 0	Rephase OFF Only	R/W	Telecom Bus – Rephase Disable: This READ/WRITE bit-field permits the user to configure the Receive STS-3/STM-1 Telecom Bus to internally compute the Pointer Bytes, based upon the data that if receives via the "RxD_D[7:0] input pins. Note: If the Receive STS-3/STM-1 Telecom Bus is being provided with pulses denoting the C1 and J1 bytes (via the "RxD_C1J1" input pin), then this feature is unnecessary. 1 – Disables Rephase
	The	ato she	1 – Disables Rephase 0 – Enables Rephase

Table 30: Interface Control Register - Byte 2 - STS-1/STM-0 Telecom Bus 2 (Address Location= 0x0139)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
STS-1 Telecom Bus ON # 2	STS-1 Telecom Bus Tri- State # 2	Unused	STS-1 Telecom Bus Parity Type # 2	STS-1 Telecom Bus J1 ONLY	STS-1 Telecom Bus Parity Odd	STS-1 Telecom Bus Parity Disable	STS-1 REPHASE OFF
R/W	R/W	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
Bit 7	STS-1	R/W	STS-1 Telecom Bus ON – Channel 25
	Telecom Bus ON # 2		This READ/WRITE bit-field permits the user to either enable or disable the Telecom Bus associated with STS-1 Telecom Bus # 2. If the STS-1 Telecom Bus is enabled, then an STS-1 signal will be mapped into (demapped) from the STS-3 signal. If STS-1 Telecom Bus Interface – Channel 2 is disabled, then Channel 2 will support the mapping of DS3, E3 or STS-1 into the STS-3 signal.
			0 – STS-1 Telecom Bus # 2 is disabled.
			In this mode, DS3/E3/STS1 Channel 2 will now be enabled. Depending upon user's selection, the following functional blocks (within Channel 2) will now be enabled.
			If DS3/E3 Framing is support
			DS3/E3 Framer Block
			DS3/E3 Mapper Block
			DS3/E3 Jitter Attenuator/De-Sync Block
		k	If STS-1 Framing is supported
			Receive STS-1 TOH Processor Block
		90	Receive STS-1 POH Processor Block
	o	100	Transmit STS-1 POH Processor Block
	(O)	\$ \$	Transmit STS-1 TOH Processor Block
	1, 20		1 – STS-1 Telecom Bus # 2 is enabled.
	0	all	In this mode, all DS3/E3 Framer block and STS-1 circuitry associated with Channel 2 will be disabled.
Bit 6	STS-1	R/W	STS-1 Telecom Bus Tri-state – Channel 2:
	Telecom Bus Tri-State # 2		This READ/WRITE bit-field permits the user to "tri-state" the Telecom Bus Interface.
			0 - Telecom Bus Interface is NOT tri-stated.
			1 – Telecom Bus Interface is tri-stated.
			Note: This READ/WRITE bit-field is ignored if the STS-1 Transmit and Receive Telecom Bus Interface is disabled.
Bit 5	Unused	R/W	
Bit 4	STS-1	R/W	STS-1 Telecom Bus Parity Type – Channel 2:
	Telecom Bus Parity Type #		This READ/WRITE bit-field permits the user to define the parameters, over

	2		which "Telecom Bus" parity will be computed.
			0 – Parity is computed/verified over the STS-1 Transmit and Receive Telecom Bus – data bus pins (e.g., STS1TXA_D_2[7:0] and STS1RXD_D_2[7:0]).
			If the user implements this selection, then the following will happen.
			g. The STS-1 Receive Telecom Bus Interface will compute and output parity (via the "STS1RXD_DP_2" output pin) based upon and coincident with the data being output via the "STS1RXD_D_2[7:0]" output pins.
			h. The STS-1 Transmit Telecom Bus Interface will compute and verify the parity data (which is input via the "STS1TXA_DP_2" input pin) based upon the data which is being input (and latched) via the "STS1TXA_D_2[7:0]" input pins.
			1 – Parity is computed/verified over the STS-1 Transmit and Receive Telecom Bus – data bus pins (e.g., STS1TXA_D_2[7:0] and STS1RXD_D_3[7:0]); the STS1TXA_C1J1_2, STS1RXD_C1J1_2, STS1TXA_PL_2 and STS1RXD_PL_2 input/output pins.
			If the user implements this selection, then the following will happen.
			The STS-1 Receive Telecom Bus Interface will compute and output parity (via the "RXD_DP_2" output) based upon and coincident with (1) the data being output via the "STS1RXD_D_2[7:0]" output pins, (2) the state of the "STS1RXD_PL_2" output pin, and (3) the state of the "STS1RXD_C1J1_2" output pin.
			The STS-1 Transmit Telecom Bus Interface will compute and verify the parity data (which is input via the "STS1TXA_DP_2" input pin) based upon (1) the data which is being input (and latched) via the "STS1TXA_D_2[7:0]" input pins, (2) the state of the "STS1TXA_PL_2" input pin, and (3) the state of the "STS1TXA_C1J1_2" input pin.
			Note: This bit-field is disabled if the STS-1 Telecom Bus is disabled. The user can configure the STS-1 Telecom Bus to compute with either even or odd parity, by writing the appropriate data into Bit 2 (Telecom Bus Parity – Odd), within this register.
Bit 3	STS-1	R/W	Telecom Bus – J1 Indicator Only – Channel 2:
	Telecom Bus J1 ONLY	POTO	This READ/WRITE bit-field permits the user to configure how the STS-1 Transmit and Receive Telecom Bus interface handles the "STS1TXA_C1J1_2" and STS1RXD_C1J1_2" signals, as described below.
		131	0 C1 and J1 Bytes
		S	This selection configures the following.
			 a. The STS-1 Receive Telecom Bus to pulse the "STS1RXD_C1J1_2" output coincident to whenever the C1 and J1 bytes are being output via the "STS1RXD_D_2[7:0]" output pins.
			b. The STS-1 Transmit Telecom Bus will expect the "STS1TXA_C1J1_2" input to pulse "high" coincident to whenever the C1 and J1 bytes are being sampled via the "STS1TXA_D_2[7:0]" input pins.
			1 – J1 Bytes Only
			This selection configures the following.
			a. The STS-1 Receive Telecom Bus Interface to only pulse the "STS1RXD_C1J1_2" output pin coincident to whenever the J1 byte is being output via the "STSRXD_D_2[7:0]" output pins.
			Note: The "STS1RXD_C1J1_2" output pin will NOT be pulsed "high" whenever the C1 byte is being output via the "STS1RXD_D_2[7:0]"

			output pins
			b. The STS-1 Transmit Telecom Bus Interface will expect the "STS1TXA_C1J1_2" input to only pulse "high" coincident to whenever the J1 byte is being sampled via the "STS1TXA_D_2[7:0]" input pins.
			Note: The "STS1TXA_C1J1_2" input pin will NOT be pulsed "high" whenever the C1 byte is being input via the "STS1TXA_D_2[7:0]" input pins
Bit 2	STS-1	R/W	Telecom Bus Parity – ODD Parity Select – Channel 2:
	Telecom Bus Parity Odd		This READ/WRITE bit-field permits the user to configure the STS-1 Telecom Bus Interface, associated with Channel 2 to do the following.
			In the Receive (Drop) Direction
			Receive STS-1 Telecom Bus to compute either the EVEN or ODD parity over the contents of the (1) STS1RxD_D_2[7:0] output pins, or (2) STS1RxD_D_2[7:0] output pins, the states of the STS1RxD_PL_2 and STS1RxD_C1J1_2 output pins (depending upon user setting for Bit 3).
			In the Transmit (Add) Direction
			Transmit STS-1 Telecom Bus to compute and verify the EVEN or ODD parity over the contents of the (1) STS1TxA_D_2[7:0] input pins, or (2) STS1TxA_D_2[7:0] input pins, the states of the STS1TxA_PL_2 and STS1TxA_C1J1_2 input pins (depending upon user setting for Bit 3).
			0 – Configures Receive (Drop) Telecom Bus to compute EVEN parity and configures the Transmit (Add) Telecom Bus to verify EVEN parity.
			1 – Configures Receive (Drop) Telecom Bus to compute ODD parity and configures the Transmit (Add) Telecom Bus to verify ODD parity.
Bit 1	STS-1	R/W	STS-1 Telecom Bus Parity Disable – Channel 2:
	Telecom Bus Parity Disable		This READ/WRITE bit-field permits the user to either enable or disable parity calculation and placement via the "STSRxD_DP_2" output pin. Further, this bit-field also permits the user to enable or disable parity verification via the "STS1TxA_DP_2" input pin by the Transmit Telecom Bus.
		AUC	1 Disables Parity Calculation (on the Receive Telecom Bus) and Disables Parity Verification (on the Transmit Telecom Bus.
	4	0,6	0 – Enables Parity Calculation and Verification
Bit 0	STS-1	R/W	STS-1 Telecom Bus – Rephase Disable – Channel 2:
	REPHASE OFF	Sold	This READ/WRITE bit-field permits the user to configure the Receive STS-1 Telecom Bus to internally compute the Pointer Bytes, based upon the data that it receives via the "RxD_D[7:0] input pins.
		' O'	Note: If the Receive STS-1 Telecom Bus is being provided with pulses denoting the C1 and J1 bytes (via the "RxD_C1J1" input pin), then this feature is unnecessary.
			1 – Disable Rephase
			0 – Enable Rephase
	•		

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 31: Interface Control Register - Byte 1 - STS-1/STM-0 Telecom Bus 1 (Address Location= 0x013A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
STS-1 Telecom Bus ON # 1	STS-1 Telecom Bus Tri- State # 1	Unused	STS-1 Telecom Bus Parity Type # 1	STS-1 Telecom Bus J1 ONLY	STS-1 Telecom Bus Parity ODD	STS-1 Telecom Bus Parity Disable	STS-1 REPHASE OFF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
Bit 7	STS-1	R/W	STS-1 Telecom Bus ON – Channel 1:
	Telecom Bus ON # 1		This READ/WRITE bit-field permits the user to either enable or disable the Telecom Bus associated with STS-1 Telecom Bus # 1. If the STS-1 Telecom Bus is enabled, then an STS-1 signal will be mapped into (demapped from) the STS-3 signal. If STS-1 Telecom Bus Interface — Channel 1 is disabled, then Channel 1 will support the mapping of DS3, E3 or STS-1 into the STS-3 signal.
			0 – STS-1 Telecom Bus # 1 is disabled.
			In this mode, DS3/E3/ST3-1 Channel 1 will now be enabled. Depending upon user's selection, the following functional blocks (within Channel 1) will now be enabled.
			If DS3/E3 Framing is supported
			DS3/E3 Framer Block
			DS3/E3 Mapper Block
			DS3/E3 Jitter Attenuator/De-Sync Block
			If STS-1 Framing is supported
			Receive STS-1 TOH Processor Block
		00	Receive STS-1 POH Processor Block
		ol	Transmit STS-1 POH Processor Block
	N	0	Transmit STS-1 TOH Processor Block
		10	STS-1 Telecom Bus # 1 is enabled.
		8	In this mode, all DS3/E3 Framer block and STS-1 circuitry associated with Channel 1 will be disabled.
Bit 6	STS-1	R/W	STS-1 Telecom Bus Tri-state – Channel 1:
	Telecom Bus Tri- State # 1		This READ/WRITE bit-field permits the user to "tri-state" the Telecom Bus Interface.
			0 - Telecom Bus Interface is NOT tri-stated.
			1 – Telecom Bus Interface is tri-stated.
			Note: This READ/WRITE bit-field is ignored if the STS-1 Transmit and Receive Telecom Bus Interface is disabled.
Bit 5	Unused	R/O	
Bit 4	STS-1	R/W	STS-1 Telecom Bus Parity Type – Channel 1:
	Telecom Bus Parity		This READ/WRITE bit-field permits the user to define the parameters, over

	Type # 1		which "Telecom Bus" parity will be computed.
			0 – Parity is computed/verified over the STS-1 Transmit and Receive Telecom Bus – data bus pins (e.g., STS1TXA_D_1[7:0] and STS1RXD_D_1[7:0]).
			If the user implements this selection, then the following will happen.
			a. The STS-1 Receive Telecom Bus Interface will compute and output parity (via the "STS1RXD_DP_1" output pin) based upon and coincident with the data being output via the "STS1RXD_D_1[7:0]" output pins.
			b. The STS-1 Transmit Telecom Bus Interface will compute and verify the parity data (which is input via the "STS1TXA_DP_1" input pin) based upon the data which is being input (and latched) via the "STS1TXA_D_1[7:0]" input pins.
			1 – Parity is computed/verified over the STS-1 Transmit and Receive Telecom Bus – data bus pins (e.g., STS1TXA_D_1[7:0] and STS1RXD_D_1[7:0]); the STS1TXA_C1J1_1, STS1RXD_C1J1_4, STS1TXA_PL_1 and STS1RXD_PL_1 input/output pins.
			If the user implements this selection, then the following will happen.
			a. The STS-1 Receive Telecom Bus Interface will compute and output parity (via the "ST\$1RXD_DP_1" output) based upon and coincident with (1) the data being output via the "ST\$1RXD_D_1[7:0]" output pins, (2) the state of the "ST\$1RXD_PL_1" output pin, and (3) the state of the "ST\$1RXD_C1J1_1" output pin.
			b. The STS-1 Transmit Telecom Bus Interface will compute and verify the parity data (which is input via the "STS1TXA_DP_1" input pin) based upon (1) the data which is being input (and latched) via the "STS1TXA_D_1[7:0]" input pins, (2) the state of the "STS1TXA_PL_1" input pin, and (3) the state of the "STS1TXA_C1J1_1" input pin.
		X	Note This bit-field is disabled if the STS-1 Telecom Bus is disabled. The user can configure the STS-1 Telecom Bus to compute/verify with either even or odd parity, by writing the appropriate data into Bit 2 (Telecom Bus Parity – Odd), within this register.
Bit 3	STS-1 Telecom	R/W	Telecom Bus – J1 Indicator Only – Channel 1:
	Bus J1 ONLY	oche	This READ/WRITE bit-field permits the user to configure how the STS-1 Transmit and Receive Telecom Bus interface handles the "STS1TXA_C1J1_1" and STS1RXD_C1J1_1" signals, as described below. 0 – C1 and J1 Bytes
		0,70	This selection configures the following.
	0	and	a. The STS-1 Receive Telecom Bus to pulse the "STS1RXD_C1J1_1"
		0	output coincident to whenever the C1 and J1 bytes are being output via the "STS1RXD_D_1[7:0]" output pins.
			b. The STS-1 Transmit Telecom Bus will expect the "STS1TXA_C1J1_1" input to pulse "high" coincident to whenever the C1 and J1 bytes are being sampled via the "STS1TXA_D_1[7:0]" input pins.
			1 – J1 Bytes Only
			This selection configures the following.
			i. The STS-1 Receive Telecom Bus Interface to only pulse the "STS1RXD_C1J1_1" output pin coincident to whenever the J1 byte is being output via the "STS1RXD_D_1[7:0]" output pins.
			Note: The "STS1RXD_C1J1_1" output pin will NOT be pulsed "high" whenever the C1 byte is being output via the "STS1RXD_D_1[7:0]"

			output pins).
			j. The STS-1 Transmit Telecom Bus Interface will expect the "STS1TXA_C1J1_1" input to only pulse "high" coincident to whenever the J1 byte is being sampled via the "STS1TXA_D_1[7:0]" input pins.
			Note: The "STS1TXA_C1J1_1" input pin will NOT be pulsed "high" whenever the C1 byte is being input via the "STS1TXA_D_1[7:0]" input pins).
Bit 2	STS-1	R/W	Telecom Bus Parity – ODD Parity Select – Channel 1:
	Telecom Bus Parity Odd		This READ/WRITE bit-field permits the user to configure the STS-1 Telecom Bus Interface, associated with Channel 1 to do the following.
			In the Receive (Drop) Direction
			Receive STS-1 Telecom Bus to compute either the EVEN or ODD parity over the contents of the (1) STS1RxD_D_1[7:0] output pins, or (2) STS1RxD_D_1[7:0] output pins, the states of the STS1RxD_PL_1 and "STS1RxD_C1J1_1 output pins (depending upon user setting for Bit 3).
			In the Transmit (Add) Direction
			Transmit STS-1 Telecom Bus to compute and verify the EVEN or ODD parity over the contents of the (1) STS1TxA_D_1[7:0] input pins, or (2) STS1TxA_D_1[7:0] input pins, the states of the STS1TxA_PL_1 and STS1TxA_C1J1_1 input pins (depending upon user setting for Bit 3).
			0 - Configures Receive (Drop) Telecom Bus to compute EVEN parity and configures the Transmit (Add) Telecom Bus to verify EVEN parity
			1 - Configures Receive (Drop) Telecom Bus to compute ODD parity and configures the Transmit (Add) Telecom Bus to verify ODD parity.
Bit 1	STS-1	R/W	STS-1 Telecom Bus Parity Disable – Channel 1:
	Telecom Bus Parity Disable		This READAWRITE bit-field permits the user to either enable or disable parity calculation and placement via the "STSRxD_DP_1" output pin. Further, this bit field also permits the user to enable or disable parity verification via the "STS1TxA_DP_1" input pin by the Transmit Telecom Bus.
		X	1 Disables Parity Calculation (on the Receive Telecom Bus) and Disables Parity Verification (on the Transmit Telecom Bus.
		400	0
Bit 0	STS-1	R/W	STS-1 Telecom Bus – Rephase Disable – Channel 1:
	OFF OFF	data	This READ/WRITE bit-field permits the user to configure the Receive STS-1 Telecom Bus to internally compute the Pointer Bytes, based upon the data that it receives via the "RxD_D[7:0] input pins.
		*	Note: If the Receive STS-1 Telecom Bus is being provided with pulses denoting the C1 and J1 bytes (via the "RxD_C1J1" input pin), then this feature is unnecessary.
			1 – Disables Rephase
			0 – Enables Rephase

Table 32: Interface Control Register – Byte 0 – STS-1/STM-0 Telecom Bus 0 (Address Location= 0x013B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
STS-1 Telecom Bus ON # 0	STS-1 Telecom Bus Tri- State # 0	STS-3c REPHASE OFF	STS-1 Telecom Bus Parity Type # 0	STS-1 Telecom Bus J1 ONLY	STS-1 Telecom Bus Parity Odd	STS-1 Telecom Bus Parity Disable	STS-1 REPHASE OFF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
Bit 7	STS-1	R/W	STS-1 Telecom Bus ON – Channel 0:
	Telecom Bus ON # 0		This READ/WRITE bit-field permits the user to either enable or disable the Telecom Bus associated with STS-1 Telecom Bus # 0. If the STS-1 Telecom Bus is enabled, then an STS-1 signal will be mapped into (demapped from) the STS-3 signal. If STS-1 Telecom Bus Interface – Channel 3 is disabled, then Channel 0 will support the mapping of DS3, E3 or STS-1 into the STS-3 signal.
			0 – STS-1 Telecom Bus # 0 is disabled.
			In this mode, DS3/E3/STS-1 Channel 0 will now be enabled. Depending upon user's selection, the following functional blocks (within Channel 0) will now be enabled.
			If DS3/E3 Framing is supported
			DS3/E3 Framer Block
			DS3/E3 Mapper Block
			DS3/E3 Jitter Attenuator/De-Sync Block
			If STS-1 Framing is supported
		"10"	Receive STS-1 TOH Processor Block
	.0	0 0	Receive STS-1 POH Processor Block
	of	No	 Transmit STS-1 POH Processor Block
	No.	9 N	Transmit STS-1 TOH Processor Block
	7, 79,	6	1 – STS-1 Telecom Bus # 0 is enabled.
		dill	In this mode, all DS3/E3 Framer block and STS-1 circuitry associated with Channel 0 will be disabled.
Bit 6	STS-1	R/W	STS-1 Telecom Bus Tri-state – Channel 0:
	Telecom Bus Tri-State # 0		This READ/WRITE bit-field permits the user to "tri-state" the Telecom Bus Interface.
			0 – Telecom Bus Interface is NOT tri-stated.
			1 – Telecom Bus Interface is tri-stated.
			Note: This READ/WRITE bit-field is ignored if the STS-1 Transmit and Receive Telecom Bus Interface is disabled.
Bit 5	STS-3c	R/O	STS-3c While Rephase Off:
	REPHASE OFF		This READ/WRITE bit-field permits the user to configure the STS-1 Telecom Bus # 0 to process STS-3c data while the "Rephase" feature is disabled.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			0 – STS-1 Telecom Bus # 0 is processing STS-3 data.
			1 – STS-1 Telecom Bus # 0 is processing STS-3c data.
			Note: This bit-field is ignored if STS-1 Telecom Bus Interface # 0 has been configured to operate in the "Rephase" Mode.
Bit 4	STS-1	R/W	STS-1 Telecom Bus Parity Type – Channel 0:
	Telecom Bus Parity Type # 0		This READ/WRITE bit-field permits the user to define the parameters, over which "Telecom Bus" parity will be computed.
			0 - Parity is computed/verified over the STS-1 Transmit and Receive Telecom Bus - data bus pins (e.g., STS1TXA_D_0[7:0] and STS1RXD_D_0[7:0]).
			If the user implements this selection, then the following will happen.
			a. The STS-1 Receive Telecom Bus Interface will compute and output parity (via the "STS1RXD_DP_0" output pin) based upon and coincident with the data being output via the "STS1RXD_D_0[7:0]" output pins.
			b. The STS-1 Transmit Telecom Bus Interface will compute and verify the parity data (which is input via the "STS1TXA_DP_0" input pin) based upon the data which is being input (and latched) via the "STS1TXA_D_0[7:0]" input pins.
			1 - Parity is computed/verified over the STS-1 Transmit and Receive Telecom Bus - data bus pins (e.g., STS1TXA_D_0[7:0] and STS1RXD_D_0[7:0]); the STS1TXA_C1J1_0, STS1RXD_C1J1_0, STS1TXA_PL_0 and STS1RXD_PL_0 input/output pins.
			If the user implements this selection, then the following will happen.
			a. The STS-1 Receive Telecom Bus Interface will compute and output parity (via the "STS1RXD_DP_0" output) based upon and coincident with (1) the data being output via the "STS1RXD_D_0[7:0]" output pins, (2) the state of the "STS1RXD_PL_0" output pin, and (3) the state of the "STS1RXD_C1J1_0" output pin.
		Produ	The STS-1 Transmit Telecom Bus Interface will compute and verify the parity data (which is input via the "STS1TXA_DP_0" input pin) based upon (1) the data which is being input (and latched) via the "STS1TXA_D_0[7:0]" input pins, (2) the state of the "STS1TXA_PL_0" input pin, and (3) the state of the "STS1TXA_C1J1_0" input pin.
	4/4	datand	Wote: This bit-field is disabled if the STS-1 Telecom Bus is disabled. The user can configure the STS-1 Telecom Bus to compute/verify with either even or odd parity, by writing the appropriate data into Bit 2 (Telecom Bus Parity – Odd), within this register.
Bit 3	STS-1	R/W	Telecom Bus – J1 Indicator Only – Channel 0:
	Telecom Bus J1 ONLY		This READ/WRITE bit-field permits the user to configure how the STS-1 Transmit and Receive Telecom Bus interface handles the "STS1TXA_C1J1_0" and STS1RXD_C1J1_0" signals, as described below.
			0 – C1 and J1 Bytes
			This selection configures the following.
			a. The STS-1 Receive Telecom Bus to pulse the "STS1RXD_C1J1_0" output coincident to whenever the C1 and J1 bytes are being output via the "STS1RXD_D_0[7:0]" output pins.
			 b. The STS-1 Transmit Telecom Bus will expect the "STS1TXA_C1J1_0" input to pulse "high" coincident to whenever the C1 and J1 bytes are being sampled via the

1 – J1 Bytes Only This selection configures the following. a. The STS-1 Receive Telecom Bus Interface to only pulse the "STS1RXD_C11J" of output pin coincident to whenever the J1 byte is being output via the "STS1RXD_D17.0" output pins. Whenever the J1 byte is being output via the "STS1RXD_C1J1,0" output pins. Whenever the C1 byte is being output via the "STS1RXD_C1J1,0" output pins. b. The STS-1 Transmit Telecom Bus Interface will expect the "STS1RXD_C1J1,0" input to only pulse "high" coincident to whenever the J1 byte is being sampled via the "STS1TXA_C1J1,0" input pins. Note: The "STS1TXA_C1J1,0" opput gin will NOT be pulsed "high" whenever the J1 byte is being sampled via the "STS1TXA_CJJ1,0" input pins. Note: The "STS1TXA_CJJ1,0" opput gin will NOT be pulsed "high" whenever the C1 byte is being sampled via the "STS1TXA_D_Q17.0" input pins. Note: The "STS1TXA_CJJ1,0" opput gin will NOT be pulsed "high" whenever the C1 byte is being sampled via the "STS1TXA_D_Q17.0" input pins. Note: The "STS1TXA_CJJ1,0" opput gin will NOT be pulsed "high" whenever the C1 byte is being sampled via the "STS1TXA_D_Q17.0" input pins. Note: The "STS1TXA_CJJ1,0" opput gin will NOT be pulsed "high" whenever the C1 byte is being sampled via the "STS1TXA_D_Q17.0" output pins. or (2) STS1TXA_D_Q17.0" input pins. or (2) STS1TXA_D_Q17.0" output pins. Or (2) STS1TXA_D_Q17.0" output pins. Or (2) STS1TXA_D_Q17.0" output pins				"STS1TXA_D_0[7:0]" input pins.
This selection configures the following. a. The STS-1 Receive Telecom Bus Interface to only pulse the "STS1RXD C1J1_0" output pin coincident to whenever the J1 byte is being output via the "STS1RXD_D[7:0]" output pins. **Note: The "STS1RXD_D_0[7:0]" output pins will NOT be pulsed "high" whenever the C1 byte is being output via the "STS1RXD_D_0[7:0]" output pins. **DITESTS-1 Transmit Telecom Bus Interface will expect the "STS1TXA_C1J1_0" input to only pulse "high" coincident to whenever the J1 byte is being sampled via the "STS1TXA_D_0[7:0]" input pins. **Note: The "STS1TXA_C1J1_0" input ion will NOT be pulsed "high" whenever the C1 byte is being sampled via the "STS1TXA_D_0[7:0]" input pins. **Note: The "STS1TXA_C1J1_0" input ion will NOT be pulsed "high" whenever the C1 byte is being sampled via the "STS1TXA_D_0[7:0]" input pins. **Note: The "STS1TXA_C1J1_0" input ion will NOT be pulsed "high" whenever the C1 byte is being sampled via the "STS1TXA_D_0[7:0]" input pins. **Parity Odd** **Telecom Bus Parity - QDP Parity Select - Channel 0: This READ/WRITE bit-feld parmits the user to configure the STS-1 Telecom Bus Interface associated with Channel 0 to do the following. In the Receive (Drop) Direction **Receive STS-1-Telecom Bus to compute either the EVEN or ODD parity over the contents of the (1) STS1RXD_D_0_017:0] upput pins, or (2) STS1RXD_D_017:0] upput pins, the states of the STS1RXD_PL_0 and "STS1RXD_C1J1" output pins, or (2) STS1RXD_D_017:0] upput pins, the states of the STS1RXD_PL_0 and STS1RXD_D_017:0] upput pins, the states of the STS1RXD_PL_0 and STS1RXD_D_017:0] upput pins, the states of the STS1RXD_PL_0 and STS1RXD_D_017:0] upput pins, the states of the STS1RXD_PL_0 and STS1RXD_D_017:0] upput pins, the states of the STS1RXD_D_017:0] upput pins, over the STS1RXD_D_017:0 upp				
a. The STS-1 Receive Telecom Bus Interface to only pulse the "STS1RXD_CJJ1_0" output pin coincident to whenever the J1 byte is being output via the "STS1RXD_CJJ1_0" output pin will NOT be pulsed "high" whenever the C1 byte is being output via the "STS1RXD_D_O[7:0]" output pins. Note: The "STS1RXD_CJJ1_0" output pins will NOT be pulsed "high" whenever the C1 byte is being output via the "STS1RXA_CJJ_O" input ton only pulse "high" coincident to whenever the J1 byte is being sampled via the "STS1RXA_CJJ1_O" input pins will NOT be pulsed "high" whenever the C1 byte is being sampled via the "STS1RXA_D_O[7:0]" input pins. Note: The "STS1RXA_CJJ1_O" onput ion will NOT be pulsed "high" whenever the C1 byte is being sampled via the "STS1RXA_D_O[7:0]" input pins. Note: The "STS1RXA_CJJ1_O" onput ion will NOT be pulsed "high" whenever the C1 byte is being sampled via the "STS1RXA_D_O[7:0]" input pins. Note: The STS1RXA_CJJ1_O" onput ion will NOT be pulsed "high" whenever the C1 byte is being sampled via the "STS1RXA_D_O[7:0]" input pins. Note: The STS1RXA_CJJ1_O" onput ion will NOT be pulsed "high" whenever the C1 byte is being sampled via the "STS1RXA_D_O[7:0]" input pins. In the Receive (Drop) Direction Receive STS-1, felecom Bus to compute either the EVEN or ODD parity over the contents of the C1 STS1RXD_D_O[7:0] input pins, or (2) STS1RXD_D				
whenever the C1 byte is being output via the "STSTRXD_D_QT-0" output pins. b. The STS-1 Transmit Telecom Bus Interface will expect the "STS1TXA_C1J1_0" input to only pulse "high" coincident to whenever the J1 byte is being sampled via the "STS1TXA_D_QT-0" input on will NOT be pulsed "high" whenever the C1 byte is being input via the "STS1TXA_D_QT-0" input pins. Note: The "STS1TXA_C1J1_0" input on will NOT be pulsed "high" whenever the C1 byte is being input via the "STS1TXA_D_QT-0" input pins. R/W Telecom Bus Parity — QOD Parity Select — Channel 0: This READ/WRITE bit-field paritis the user to configure the STS-1 Telecom Bus Interface associated with Channel 0 to do the following. In the Receive (Drop) Direction Receive STS-1 Telecom Bus to compute either the EVEN or ODD parity over the contents of the 11 STS1RxD_D_0[7:0] output pins, or (2) STS1RxD_D_0[7:0] output pins, the states of the STS1RxD_PL_0 and "STS1RxD_C1J1_0" output pins, the states of the STS1RxD_PL_0 and "STS1RxD_C1J1_0" output pins, the states of the STS1RxD_PL_0 and STS1xA_4_J1_0 input pins, the states of the STS1RxD_PL_0 and STS1xA_4_J1_0 input pins, or (2) STS1RxD_D1. Bit 1 STS-10 First READ/WRITE bit-field permits the user to enable or disable parity calculation and placement via the "STS1RxD_DP_0" output pins. Purther, this bit field also permits the user to enable or disable parity calculation and placement via the "STSRxD_DP_0" output pins. Further, this bit field also permits the user to enable or disable parity verification via the "STS1AZ_DP_0" output pin by the Transmit Telecom Bus. 1 — Disables Parity Calculation and Verification Bit 0 STS-1 R/W STS-1 Telecom Bus — Rephase Disable — Channel 0: This READ/WRITE bit-field permits the user to configure the Receive STS-1 Telecom Bus to internally compute the Politore Bytes, based upon the data that it receives via the "RxD_D[7:0] input pins. Note: If the Receive STS-1 Telecom Bus is being provided with pulses denoting the C1 and J1 bytes (via the "RxD_C1J1" input pin), the				a. The STS-1 Receive Telecom Bus Interface to only pulse the "STS1RXD_C1J1_0" output pin coincident to whenever the J1 byte
"STS1TXA_C1J1_0" input to only pulse "high" coincident to whenever the J1 byte is being sampled via the "STS1TXA_D_0[7:0]" input pins. **Note:** The "STS1TXA_C1J1.0" input on will NOT be pulsed "high" whenever the C1 byte is being input via the "STS1TXA_D_0[7:0]" input pins **Bit 2** STS-1** Telecom Bus Parity - ODD Parity Select - Channel 0: This READ/WRITE bit-field parints the user to configure the STS-1 Telecom Bus Interface; associated with Channel 0 to do the following. In the Receive STS-1 Telecom Bus to compute either the EVEN or ODD parity over the contents; of the (1) STS1RXD_D_0[7:0] output pins, or (2) STS1RXD_D_0[7:0] input pins (depending upon user setting for Bit 3). In the Tansmit STS-1 Telecom Bus to compute and verify the EVEN or ODD parity over the contents of the (1) STS1TxA_D_0[7:0] input pins, or (2) STS1TxA_D_0[7:0] input pins, the states of the STS1TxA_P_0 and STS1TxA_D_0[7:0] input pins, the states of the STS1TxA_P_0 and STS1TxA_D_0[7:0] input pins (depending upon user setting for Bit 3). **In the Tansmit (Add) Telecom Bus to compute EVEN parity and configures the Transmit (Add) Telecom Bus to compute DDD parity and configures the Transmit (Add) Telecom Bus to verify ODD parity and configures the Transmit (Add) Telecom Bus to verify ODD parity and configures the Transmit (Add) Telecom Bus to verify ODD parity and configures the Transmit (Add) Telecom Bus to verify ODD parity and configures the Transmit (Add) Telecom Bus to verify ODD parity and configures the Transmit (Add) Telecom Bus to verify ODD parity and configures the Transmit (Add) Telecom Bus to verify ODD parity and configures the Transmit (Add) Telecom Bus to verify ODD parity and configures the Transmit (Add) Telecom Bus to verify ODD parity and configures the Transmit (Add) Telecom Bus to verify ODD parity and configures the Transmit (Add) Telecom Bus to verify ODD parity and configures the Transmit Telecom Bus				whenever the C1 byte is being output via the
Bit 2 STS-1 Telecom Bus Parity Odd R/W Telecom Bus Parity - ODD Parity Select - Channel 0: This READ/WRITE bit-field parmits the user to configure the STS-1 Telecom Bus Interface; associated with Channel 0 to do the following. In the Receive (Drop) Direction Receive (STS-1, Telecom Bus to compute either the EVEN or ODD parity over the contents of the (1) STS1RxD_D_0[7:0] output pins, or (2) STS1RxD_D_0[7:0] output pins, the states of the STS1RxD_PL_0 and "STS1RxD_D_0[7:0] output pins, the states of the STS1RxD_PL_0 and "STS1RxD_D_0[7:0] input pins (depending upon user setting for Bit 3). In the Transmit (Add) Direction Transmit STS-1, Telecom Bus to compute and verify the EVEN or ODD parity over the contents of the (1) STS1TxA_D_0[7:0] input pins, or (2) STS1TxA_D_0[7:0] input pins, the states of the STS1TxA_PL_0 and STS1TxA_D_10[7:0] input pins (depending upon user setting for Bit 3). O_Configures Receive (Drop) Telecom Bus to compute EVEN parity and configures the Transmit (Add) Telecom Bus to compute EVEN parity and configures the Transmit (Add) Telecom Bus to compute DDD parity and configures the Transmit (Add) Telecom Bus to terrify EVEN parity STS-1 Telecom Bus Parity Disable - Channel 0: This READ/WRITE bit-field permits the user to either enable or disable parity verification via the "STS1TxA_DP_0" input pin by the Transmit Telecom Bus. 1 - Disables Parity Calculation (on the Receive Telecom Bus) and Disables Parity Verification (on the Transmit Telecom Bus. 0 - Enables Parity Calculation and Verification REPHASE OFF RW STS-1 Telecom Bus - Rephase Disable - Channel 0: This READ/WRITE bit-field permits the user to configure the Receive STS-1 Telecom Bus to internally compute the Pointer Bytes, based upon the data that it receives via the "RxD_D[7:0] input pins. Note: If the Receive STS-1 Telecom Bus is being provided with pulses denoting the C1 and J1 bytes (via the "RxD_C1J1" input pin), then				"STS1TXA_C1J1_0" input to only pulse "high" coincident to whenever the J1 byte is being sampled via the
Telecom Bus Parity Odd This READ/WRITE bit-tiefd permits the user to configure the STS-1 Telecom Bus Interface associated with Channel 0 to do the following. In the Receive (Drop) Direction Receive STS-1, Telecom Bus to compute either the EVEN or ODD parity over the contents of the (1) STS1RxD_D_0[7:0] output pins, or (2) STS1RxD_D_0[7:0] output pins, the states of the STS1RxD_D_C and "STS1RxD_C1J_D output pins (depending upon user setting for Bit 3). In the Transmit (Add) Direction Transmit STS-1, Telecom Bus to compute and verify the EVEN or ODD parity over the contents of the (1) STS1TxA_D_0[7:0] input pins, or (2) STS1TxA_D_0[7:0] input pins, the states of the STS1TxA_PL_0 and STS1TxA_D_0[7:0] input pins, the states of the STS1TxA_PL_0 and STS1TxA_D_0[7:0] input pins, the states of the STS1TxA_PL_0 and STS1TxA_D_0[7:0] input pins, the states of the STS1TxA_PL_0 and STS1TxA_D_0[7:0] input pins, the states of the STS1TxA_PL_0 and STS1TxA_D_0[7:0] input pins, the states of the STS1TxA_PL_0 and STS1TxA_D_0[7:0] input pins, the states of the STS1TxA_PL_0 and STS1TxA_D_0[7:0] input pins, the states of the STS1TxA_PL_0 and STS1TxA_D_0[7:0] input pins, the states of the STS1TxA_PL_0 and STS1TxA_D_0[7:0] input pins, the states of the STS1TxA_PL_0 and STS1TxA_D_0[7:0] input pins, the states of the STS1TxA_D_D_0 and STS1TxA_D_0[7:0] input pins the user to compute CDD parity and configures the Transmit (Add) Telecom Bus to verify ODD parity and configures the Transmit Telecom Bus. 1 - Disables Parity Calculation (on the Receive Telecom Bus) and Disables Parity Verification (in the Transmit Telecom Bus. 2 - Enables Parity Calculation and Verification Bit 0 STS-1 REPMASE_OFF This READ/WRITE bit-field permits the user to configure the Receive STS-1 Telecom Bus to internally compute the Pointer Bytes, based upon the data that it receives via the "RxD_D[7:0] input pins. Note: If the Receive STS-1 Telecom Bus is being provided with pulses denoting the C1 and J1 bytes (via the "RxD_D(7:1)" input pin), then				whenever the C1 byte is being input via the "STS1TXA_D_0[7:0]"
This READ/WRITE bit-field permits the user to configure the STS-1 Telecom Bus Interface associated with Channel 0 to do the following. In the Receive (Drop) Direction Receive STS-1 Telecom Bus to compute either the EVEN or ODD parity over the contents of the (1) STS1RxD_D_0[7:0] output pins, or (2) STS1RxD_D_1_0 10;7:0] bruput pins, the states of the STS1RxD_PL_0 and "STS1RxD_C_1]-1 output pins (depending upon user setting for Bit 3). In the Transmit (Add) Direction Transmit STS-1 Telecom Bus to compute and verify the EVEN or ODD parity over the contents of the (1) STS1TxA_D_0[7:0] input pins, or (2) STS1TyA_D_0[7:0] input pins, the states of the STS1TxA_PL_0 and STS(TxA_C_1]-1_0 input pins, the states of the STS1TxA_PL_0 and STS(TxA_C_1]-1_0 input pins, the states of the STS1TxA_PL_0 and STS(TxA_C_1]-1_0 input pins, the states of the STS1TxA_PL_0 and STS(TxA_C_1]-1_0 input pins, the states of the STS1TxA_PL_0 and STS(TxA_C_1]-1_0 input pins, the states of the STS1TxA_PL_0 and STS(TxA_C_1]-1_0 input pins, the states of the STS1TxA_PL_0 and STS(TxA_C_1]-1_0 input pins, the states of the STS1TxA_PL_0 and STS(TxA_C_1]-1_0 input pins, the states of the STS1TxA_PL_0 and STS(TxA_C_1]-1_0 input pins, the states of the STS1TxA_PL_0 and STS(TxA_C_1]-1_0 input pins the Transmit (Add) Telecom Bus to verify ODD parity and configures the Transmit (Add) Telecom Bus to verify ODD parity. Bit 1 STS-1 Telecon Bus Parity Disable - Channel 0: This READ/WRITE bit-field permits the user to enable or disable parity verification via the "STS1TxA_DP_0" input pin by the Transmit Telecom Bus. 1 - Disables Parity Calculation (on the Receive Telecom Bus) and Disables Parity Verification (on the Transmit Telecom Bus. 2 - Enables Parity Calculation and Verification Bit 0 STS-1 REPHASE OFF This READ/WRITE bit-field permits the user to configure the Receive STS-1 Telecom Bus to internally compute the Pointer Bytes, based upon the data that it receives via the "RxD_D[7:0] input pins. Note: If the Receive STS-1 Telecom Bus is be	Bit 2		R/W	Telecom Bus Parity - ODD Parity Select - Channel 0:
Receive STS-1, Telecom Bus to compute either the EVEN or ODD parity over the contents of the (1) STS1RxD_D_0[7:0] output pins, or (2) STS1RxD_D_0 0[7:0] output pins, the states of the STS1RxD_PL_0 and "STS1RxD_E_01] to output pins (depending upon user setting for Bit 3). In the Transmit (Add) Direction Transmit STS-1 Telecom Bus to compute and verify the EVEN or ODD parity over the contents of the (1) STS1TxA_D_0[7:0] input pins, or (2) STS1TxA_D_D_0[7:0] input pins, or (2) STS1TxA_D_0[7:0] input pins, or (2) STS1TxA_D_D_0[7:0] input pins, or (2) STS1TxA_D_D_0[7:0] input pins, or (2) STS1TxA_D_D_0[7:0] input				
over the contents of the (1) STS1RxD_D_0[7:0] output pins, or (2) STS1RxD_D_0[7:0] output pins, the states of the STS1RxD_PL_0 and "STS1RxD_D_0[7:0] output pins (depending upon user setting for Bit 3). In the Transmit (Add) Direction Transmit STS-1, Telecom Bus to compute and verify the EVEN or ODD parity over the contents of the (1) STS1TxA_D_0[7:0] input pins, or (2) STS1TxA_D_0[7:0] input pins, the states of the STS1TxA_PL_0 and STS[TxA_C1]T_0 input pins (depending upon user setting for Bit 3). 0 Configures Receive (Drop) Telecom Bus to compute EVEN parity and configures the Transmit (Add) Telecom Bus to verify EVEN parity 1 Configures Receive (Drop) Telecom Bus to verify ODD parity and configures the Transmit (Add) Telecom Bus to verify ODD parity. 8 STS-1 Telecom Bus Parity Disable - Channel 0: This READ/WRITE bit-field permits the user to either enable or disable parity calculation and placement via the "STSRXD_DP_0" output pin. Further, this bit field also permits the user to enable or disable parity verification via the "STS1TxA_DP_0" input pin by the Transmit Telecom Bus. 1 - Disables Parity Calculation (on the Receive Telecom Bus) and Disables Parity Verification (on the Transmit Telecom Bus. 0 - Enables Parity Calculation and Verification STS-1 READ/WRITE bit-field permits the user to configure the Receive STS-1 Telecom Bus to internally compute the Pointer Bytes, based upon the data that it receives via the "RxD_D[7:0] input pin, ben denoting the C1 and J1 bytes (via the "RxD_C1J1" input pin), then				In the Receive (Drop) Direction
Transmit STS-1 Telecom Bus to compute and verify the EVEN or ODD parity over the contents of the (1) STS1TxA_D_0[7:0] input pins, or (2) STS1TxA_D_0[7:0] input pins, the states of the STS1TxA_PL_0 and STS1TxA_O_1J1-0 input pins (depending upon user setting for Bit 3). 0 Configures Receive (Drop) Telecom Bus to compute EVEN parity and configures the Transmit (Add) Telecom Bus to verify EVEN parity and configures the Transmit (Add) Telecom Bus to verify DDD parity and configures the Transmit (Add) Telecom Bus to verify DDD parity and configures the Transmit Polecom Bus to verify DDD parity. Bit 1 STS-1 R/W Telecom Bus Parity Disable - Channel 0: This READ/WRITE bit-field permits the user to either enable or disable parity calculation and placement via the "STSRXD_DP_0" output pin. Further, this bit field also permits the user to enable or disable parity verification via the "STS1TxA_DP_0" input pin by the Transmit Telecom Bus. 1 - Disables Parity Calculation (on the Receive Telecom Bus) and Disables Parity Verification (on the Transmit Telecom Bus. 0 - Enables Parity Calculation and Verification STS-1 REPHASE OFF R/W STS-1 Telecom Bus - Rephase Disable - Channel 0: This READ/WRITE bit-field permits the user to configure the Receive STS-1 Telecom Bus to internally compute the Pointer Bytes, based upon the data that it receives via the "RXD_D[7:0] input pins. Note: If the Receive STS-1 Telecom Bus is being provided with pulses denoting the C1 and J1 bytes (via the "RXD_C1J1" input pin), then				over the contents of the (1) STS1RxD_D_0[7:0] output pins, or (2) STS1RxD_D_0[7:0] output pins, the states of the STS1RxD_PL_0 and "STS1RxD_C1J1_0 output pins (depending upon user setting for Bit 3).
Bit 1 STS-1 Telecom Bus Parity Disable Parity Disable Bit 0 STS-1 REPHASE OFF R/W STS-1 Telecom Bus Parity Calculation (on the Receive Telecom Bus) STS-1 READ/WRITE bit-field permits the user to enable or disable parity verification (on the Transmit Telecom Bus) ARW STS-1 Telecom Bus Parity Disable – Channel 0: This READ/WRITE bit-field permits the user to enable or disable parity calculation and placement via the "STSRXD_DP_0" output pin. Further, this bit field also permits the user to enable or disable parity verification via the "STS1TxA_DP_0" input pin by the Transmit Telecom Bus. 1 – Disables Parity Calculation (on the Receive Telecom Bus) and Disables Parity Verification (on the Transmit Telecom Bus. 0 – Enables Parity Calculation and Verification STS-1 REPHASE OFF R/W STS-1 Telecom Bus – Rephase Disable – Channel 0: This READ/WRITE bit-field permits the user to configure the Receive STS-1 Telecom Bus to internally compute the Pointer Bytes, based upon the data that it receives via the "RxD_D[7:0] input pins. Note: If the Receive STS-1 Telecom Bus is being provided with pulses denoting the C1 and J1 bytes (via the "RxD_C1J1" input pin), then			(6	Transmit STS-1 Telecom Bus to compute and verify the EVEN or ODD parity over the contents of the (1) STS1TxA_D_0[7:0] input pins, or (2) STS1TxA_D_0[7:0] input pins, the states of the STS1TxA_PL_0 and
Bit 1 STS-1 Telecom Bus Parity Disable - Channel 0: This READ/WRITE bit-field permits the user to either enable or disable parity calculation and placement via the "STSRxD_DP_0" output pin. Further, this bit field also permits the user to enable or disable parity verification via the "STS1TxA_DP_0" input pin by the Transmit Telecom Bus. 1 - Disables Parity Calculation (on the Receive Telecom Bus) and Disables Parity Verification (on the Transmit Telecom Bus. 0 - Enables Parity Calculation and Verification 8it 0 STS-1 REPHASE OFF R/W STS-1 Telecom Bus - Rephase Disable - Channel 0: This READ/WRITE bit-field permits the user to configure the Receive STS-1 Telecom Bus to internally compute the Pointer Bytes, based upon the data that it receives via the "RxD_D[7:0] input pins. Note: If the Receive STS-1 Telecom Bus is being provided with pulses denoting the C1 and J1 bytes (via the "RxD_C1J1" input pin), then				O Configures Receive (Drop) Telecom Bus to compute EVEN parity and configures the Transmit (Add) Telecom Bus to verify EVEN parity
Telecom Bus Parity Disable This READ/WRITE bit-field permits the user to either enable or disable parity calculation and placement via the "STSRxD_DP_0" output pin. Further, this bit field also permits the user to enable or disable parity verification via the "STS1TxA_DP_0" input pin by the Transmit Telecom Bus. 1 - Disables Parity Calculation (on the Receive Telecom Bus) and Disables Parity Verification (on the Transmit Telecom Bus. 0 - Enables Parity Calculation and Verification 8th 0 STS-1 REPHASE OFF R/W STS-1 Telecom Bus - Rephase Disable - Channel 0: This READ/WRITE bit-field permits the user to configure the Receive STS-1 Telecom Bus to internally compute the Pointer Bytes, based upon the data that it receives via the "RxD_D[7:0] input pins. Note: If the Receive STS-1 Telecom Bus is being provided with pulses denoting the C1 and J1 bytes (via the "RxD_C1J1" input pin), then		A ^C	o ke	
This READ/WRITE bit-field permits the user to either enable or disable parity calculation and placement via the "STSRXD_DP_0" output pin. Further, this bit field also permits the user to enable or disable parity verification via the "STS1TxA_DP_0" input pin by the Transmit Telecom Bus. 1 - Disables Parity Calculation (on the Receive Telecom Bus) and Disables Parity Verification (on the Transmit Telecom Bus. 0 - Enables Parity Calculation and Verification 8th 0 STS-1 RPW STS-1 Telecom Bus - Rephase Disable - Channel 0: This READ/WRITE bit-field permits the user to configure the Receive STS-1 Telecom Bus to internally compute the Pointer Bytes, based upon the data that it receives via the "RxD_D[7:0] input pins. Note: If the Receive STS-1 Telecom Bus is being provided with pulses denoting the C1 and J1 bytes (via the "RxD_C1J1" input pin), then	Bit 1		R/W	STS-1 Telecom Bus Parity Disable – Channel 0:
Parity Verification (on the Transmit Telecom Bus. 0 – Enables Parity Calculation and Verification 8TS-1 REPHASE OFF R/W STS-1 Telecom Bus – Rephase Disable – Channel 0: This READ/WRITE bit-field permits the user to configure the Receive STS-1 Telecom Bus to internally compute the Pointer Bytes, based upon the data that it receives via the "RxD_D[7:0] input pins. Note: If the Receive STS-1 Telecom Bus is being provided with pulses denoting the C1 and J1 bytes (via the "RxD_C1J1" input pin), then			and n.	parity calculation and placement via the "STSRxD_DP_0" output pin. Further, this bit field also permits the user to enable or disable parity verification via the "STS1TxA_DP_0" input pin by the Transmit Telecom
Bit 0 STS-1 REPHASE OFF RIV STS-1 Telecom Bus – Rephase Disable – Channel 0: This READ/WRITE bit-field permits the user to configure the Receive STS-1 Telecom Bus to internally compute the Pointer Bytes, based upon the data that it receives via the "RxD_D[7:0] input pins. Note: If the Receive STS-1 Telecom Bus is being provided with pulses denoting the C1 and J1 bytes (via the "RxD_C1J1" input pin), then				
REPHASE OFF This READ/WRITE bit-field permits the user to configure the Receive STS-1 Telecom Bus to internally compute the Pointer Bytes, based upon the data that it receives via the "RxD_D[7:0] input pins. Note: If the Receive STS-1 Telecom Bus is being provided with pulses denoting the C1 and J1 bytes (via the "RxD_C1J1" input pin), then				0 – Enables Parity Calculation and Verification
REPHASE OFF This READ/WRITE bit-field permits the user to configure the Receive STS-1 Telecom Bus to internally compute the Pointer Bytes, based upon the data that it receives via the "RxD_D[7:0] input pins. Note: If the Receive STS-1 Telecom Bus is being provided with pulses denoting the C1 and J1 bytes (via the "RxD_C1J1" input pin), then	Bit 0		R/W	STS-1 Telecom Bus – Rephase Disable – Channel 0:
denoting the C1 and J1 bytes (via the "RxD_C1J1" input pin), then				This READ/WRITE bit-field permits the user to configure the Receive STS-1 Telecom Bus to internally compute the Pointer Bytes, based upon the data
<u> </u>			_	denoting the C1 and J1 bytes (via the "RxD_C1J1" input pin), then

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Roy		

	1 – Disables Rephase
	0 – Enables Rephase

The product are no ordered (OBS)

Table 33: Interface Control Register – STS-1/STM-0 Telecom Bus Interrupt Enable/Status Register (Address Location= 0x013C)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	TB2 RxParity Error Interrupt Status	TB1 RxParity Error Interrupt Status	TB0 RxParity Error Interrupt Status	Unused	TB2 RxParity Error Interrupt Enable	TB1 RxParity Error Interrupt Enable	TB0 RxParity Error Interrupt Enable
R/O	RUR	RUR	RUR	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Unused	R/O	"His red
6	Telecom Bus # 2 Receive Parity Error Interrupt Status	RUR	STS-1 Telecom Bus # 2 – Receive Parity Error Interrupt Status: This RESET-upon-READ bit-field indicates whether or "STS-1 Telecom Bus – Channel 2" has declared a "Receive Parity Error" Interrupt since the last read of this register. 0 – The "Receive Parity Error" Interrupt has not occurred since the last read of this register. 1 – The "Receive Parity Error" Interrupt has occurred since the last read of this register. Note: This bit-field is only active if "STS-1 Telecom Bus – Channel 2" has been enabled.
5	Telecom Bus # 1 Receive Parity Error Interrupt Status	RUR	STS-1 Telecom Bus # 1 – Receive Parity Error Interrupt Status: This RESET-upon-READ bit-field indicates whether or "STS-1 Telecom Bus Channel 1" has declared a "Receive Parity Error" Interrupt since the last read of this register. O – The "Receive Parity Error" Interrupt has not occurred since the last read of this register. 1 – The "Receive Parity Error" Interrupt has occurred since the last read of this register. Note: This bit-field is only active if "STS-1 Telecom Bus – Channel 1" has been enabled.
4	Telecom Bus # 0 Receive Parity Error Interrupt Status	RUR	STS-1 Telecom Bus # 0 – Receive Parity Error Interrupt Status: This RESET-upon-READ bit-field indicates whether or "STS-1 Telecom Bus – Channel 3" has declared a "Receive Parity Error" Interrupt since the last read of this register. 0 – The "Receive Parity Error" Interrupt has not occurred since the last read of this register. 1 – The "Receive Parity Error" Interrupt has occurred since the last read of this register. Note: This bit-field is only active if "STS-1 Telecom Bus – Channel 0" has been enabled.
3	Unused	R/O	
2	Telecom Bus # 2 - Receive Parity Error Interrupt	R/W	STS-1 Telecom Bus # 2 – Receive Parity Error Interrupt Enable This READ/WRITE bit-field permits the user to either enable or disable the

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

	Enable		"Receive Parity Error" Interrupt for STS-1 Telecom Bus – Channel 2. If the user enables this interrupt, then STS-1 Telecom Bus – Channel 2 will generate an interrupt anytime the "Receive STS-1 Telecom Bus" detects a parity error within the incoming STS-1 data.		
			0 – Disables the "Receive Parity Error" Interrupt.		
			1 – Enables the "Receive Parity Error" Interrupt.		
			Note: This bit-field is only active if "STS-1 Telecom Bus – Channel 2" has been enabled.		
1	Telecom Bus # 1	R/W	STS-1 Telecom Bus # 1 – Receive Parity Error Interrupt Enable		
	Receive Parity Error Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Receive Parity Error" Interrupt for STS-1Telecom Bus – Channel 1. If the user enables this interrupt, then STS-1 Telecom Bus – Channel 1 will generate an interrupt anytime the "Receive STS-1 Telecom Bus" detects a parity error within the incoming STS-1 data.		
			0 – Disables the "Receive Parity Error" Interrupt.		
			1 – Enables the "Receive Parity Error" Interrupt.		
			Note: This bit-field is only active if \$7S-1 Telecom Bus – Channel 1" has been enabled.		
0	Telecom Bus # 0 - Receive Parity Error Interrupt Enable	R/W	STS-1 Telecom Bus # 0 - Receive Parity Error Interrupt Enable This READ/WRITE bit-field permits the user to either enable or disable the "Receive Parity Error" Interrupt for STS-1 Telecom Bus - Channel 0. If the user enables this interrupt, then STS-1 Telecom Bus - Channel 0 will generate an interrupt anytime the "Receive STS-1 Telecom Bus" detects a parity error within the incoming STS-1 data. 0 - Disables the "Receive Parity Error" Interrupt. 1 - Enables the "Receive Parity Error" Interrupt. Note: This bit-field is only active if "STS-1 Telecom Bus - Channel 0" has been enabled.		
Note: This bit-field is only active if "STS-1 Telecom Bus – Channel 0" has been enabled.					

Table 34: Interface Control Register – STS-1/STM-0 Telecom Bus FIFO Status Register (Address Location = 0x013D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Unused	STS-1 Telecom Bus Tx Overrun Bus 2	STS-1 Telecom Bus Tx Underrun Bus 2	STS-1 Telecom Bus Tx Overrun Bus 1	STS-1 Telecom Bus Tx Underrun Bus 1	STS-1 Telecom Bus Tx Overrun Bus 0	STS-1 Telecom Bus Tx Underrun Bus 0
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Unused	R/O	khis rec
6	Unused	R/O	in chi
5	STS-1	R/O	STS-1 Telecom Bus – Transmit FIFO Overrun Indicator – Channel 2:
	Telecom Bus – TxFIFO Overrun # 2		This READ-ONLY bit-field indicates whether or not "STS-1 Telecom Bus – Channel 2" is currently declaring a "Transmit FIFO Overrun" condition.
			0 – Indicates that "STS-1 Telecom Bus – Channel 2" is NOT declaring a "Transmit FIFO Overrun" condition.
			1 – Indicates that "STS-1 Telecom Bus – Channel 2" is currently declaring a "Transmit FIFO Overrun" condition.
			Note: This bit field is only active if "STS-1 Telecom Bus – Channel 2" has been enabled.
4	STS-1	R/O	STS-1 Telecom Bus – Transmit FIFO Underrun Indicator – Channel 2:
	Telecom Bus – TxFIFO Underrun # 2		This READ-ONLY bit-field indicates whether or not "STS-1 Telecom Bus – Channel 3" is currently declaring a "Transmit FIFO Underrun" condition.
		Alla	0 Indicates that "STS-1 Telecom Bus – Channel 2" is NOT declaring a "Transmit FIFO Underrun" condition.
		locks	1 – Indicates that "STS-1 Telecom Bus – Channel 2" is currently declaring a "Transmit FIFO Underrun" condition.
	The	10 (Note: This bit-field is only active if "STS-1 Telecom Bus – Channel 2" has been enabled.
3	STS-1	R/O	STS-1 Telecom Bus – Transmit FIFO Overrun Indicator – Channel 1:
	Telecom Bus – TxFIFO Overrun # 1	0	This READ-ONLY bit-field indicates whether or not "STS-1 Telecom Bus – Channel 1" is currently declaring a "Transmit FIFO Overrun" condition.
			0 - Indicates that "STS-1 Telecom Bus - Channel 1" is NOT declaring a "Transmit FIFO Overrun" condition.
			1 – Indicates that "STS-1 Telecom Bus – Channel 1" is currently declaring a "Transmit FIFO Overrun" condition.
			Note: This bit-field is only active if "STS-1 Telecom Bus – Channel 1" has been enabled.
2	STS-1	R/O	STS-1 Telecom Bus – Transmit FIFO Underrun Indicator – Channel 1:
	Telecom Bus – TxFIFO Underrun # 1		This READ-ONLY bit-field indicates whether or not "STS-1 Telecom Bus – Channel 1" is currently declaring a "Transmit FIFO Underrun" condition.
			0 - Indicates that "STS-1 Telecom Bus - Channel 1" is NOT declaring a

EXAR Experience Our Connectivit

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			"Transmit FIFO Underrun" condition.	
			1 – Indicates that "STS-1 Telecom Bus – Channel 1" is currently declaring a "Transmit FIFO Underrun" condition.	
			Note: This bit-field is only active if "STS-1 Telecom Bus – Channel 1" has been enabled.	
1	STS-1	R/O	STS-1 Telecom Bus – Transmit FIFO Overrun Indicator – Channel 0:	
	Telecom Bus – TxFIFO Overrun # 0		This READ-ONLY bit-field indicates whether or not "STS-1 Telecom Bus – Channel 0" is currently declaring a "Transmit FIFO Overrun" condition.	
			0 - Indicates that "STS-1 Telecom Bus - Channel 0" is NOT declaring a "Transmit FIFO Overrun" condition.	
			1 – Indicates that "STS-1 Telecom Bus – Channel 0" is currently declaring a "Transmit FIFO Overrun" condition.	
			Note: This bit-field is only active if "ST\$1 Telecom Bus – Channel 0" has been enabled.	
0	STS-1	R/O	STS-1 Telecom Bus – Transmit FIFO Underrun Indicator – Channel 0:	
	Telecom Bus – TxFIFO Underrun # 0		This READ-ONLY bit-field indicates whether or not "STS-1 Telecom Bus – Channel 0" is currently declaring a "Transmit FIFO Underrun" condition.	
			0 - Indicates that "STS-1 Telecom Bus - Channel 0" is NOT declaring a "Transmit FIFO Underrun" condition.	
			1 – Indicates that "STS-7 Telecom Bus – Channel 0" is currently declaring a "Transmit FIFO Underrun" condition	
			Note: This bit-field is only active if "STS-1 Telecom Bus – Channel 0" has been enabled.	
Note: This bit-field is only active if "STS-1 Telecom Bus – Channel 0" has been enabled.				

Table 35: Interface Control Register – STS-1/STM-0 Telecom Bus FIFO Interrupt Status Register (Address Location= 0x013E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Unused	STS-1 Telecom Bus # 2 Tx Overrun Interrupt Status	STS-1 Telecom Bus # 2 Tx Underrun Interrupt Status	STS-1 Telecom Bus # 1 Tx Overrun Interrupt Status	STS-1 Telecom Bus # 1 Tx Underrun Interrupt Status	STS-1 Telecom Bus # 0 Tx Overrun Interrupt Status	STS-1 Telecom Bus # 0 Tx Underrun Interrupt Status
R/O	R/O	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7	Unused	R/O	
6	Unused	R/O	911, 2ct
5	STS-1 Telecom Bus # 2 - TxFIFO Overrun Interrupt Status	RUR	STS-1 Telecom Bus – TxFIFO Overrun Interrupt Status – Channel 2: This RESET-upon-READ bit field indicates whether or not "STS-1 Telecom Bus – Channel 2" has declared a "TxFIFO Overrun" Interrupt since the last read of this register. 0 – Indicates that "STS-1 Telecom Bus – Channel 2" has NOT declared a "TxFIFO Overrun" Interrupt since the last read of this register. 1 – Indicates that "STS-1 Telecom Bus – Channel 2" has declared a "TxFIFO Overrun" Interrupt since the last read of this register. Note: This bit-field is only active if "STS-1 Telecom Bus – Channel 2" has been enabled.
4	STS-1 Telecom Bus # 2 - TxFIFO Underrun Interrupt Status	RUR	STS-1 Telecom Bus – TxFIFO Underrun Interrupt Status – Channel 2: This RESET-upon-READ bit-field indicates whether or not "STS-1 Telecom Bus – Channel 2" has declared a "TxFIFO Underrun" Interrupt since the last read of this register. O Indicates that "STS-1 Telecom Bus – Channel 2" has NOT declared a "TxFIFO Underrun" Interrupt since the last read of this register. 1 – Indicates that "STS-1 Telecom Bus – Channel 2" has declared a "TxFIFO Overrun" Interrupt since the last read of this register. Note: This bit-field is only active if "STS-1 Telecom Bus – Channel 2" has been enabled.
3	STS-1 Telecom Bus # 1 – TxFIFO Overrun Interrupt Status	RUR	STS-1 Telecom Bus – TxFIFO Overrun Interrupt Status – Channel 1: This RESET-upon-READ bit-field indicates whether or not "STS-1 Telecom Bus – Channel 1" has declared a "TxFIFO Overrun" Interrupt since the last read of this register. 0 – Indicates that "STS-1 Telecom Bus – Channel 1" has NOT declared a "TxFIFO Overrun" Interrupt since the last read of this register. 1 – Indicates that "STS-1 Telecom Bus – Channel 1" has declared a "TxFIFO Overrun" Interrupt since the last read of this register. Note: This bit-field is only active if "STS-1 Telecom Bus – Channel 1" has been enabled.
2	STS-1 Telecom Bus # 1 –	RUR	STS-1 Telecom Bus – TxFIFO Underrun Interrupt Status – Channel 1:

EXARExperience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

	TxFIFO Underrun Interrupt Status		This RESET-upon-READ bit-field indicates whether or not "STS-1 Telecom Bus – Channel 1" has declared a "TxFIFO Underrun" Interrupt since the last read of this register.
			0 – Indicates that "STS-1 Telecom Bus – Channel 1" has NOT declared a "TxFIFO Underrun" Interrupt since the last read of this register.
			1 – Indicates that "STS-1 Telecom Bus – Channel 1" has declared a "TxFIFO Overrun" Interrupt since the last read of this register.
			Note: This bit-field is only active if "STS-1 Telecom Bus – Channel 1" has been enabled.
1	STS-1 Telecom	RUR	STS-1 Telecom Bus – TxFIFO Overrun Interrupt Status – Channel 0:
	Bus # 0 – TxFIFO Overrun Interrupt Status		This RESET-upon-READ bit-field indicates whether or not "STS-1 Telecom Bus – Channel 0" has declared a "TxFIFO Overrun" Interrupt since the last read of this register.
			0 – Indicates that "STS-1 Telecom Bus." Channel 0" has NOT declared a "TxFIFO Overrun" Interrupt since the last read of this register.
			1 – Indicates that "STS-1 Telecom Bus – Channel 0" has declared a "TxFIFO Overrun" Interrupt since the last read of this register.
			Note: This bit-field is only active if STS-1 Telecom Bus – Channel 0" has been enabled.
0	STS-1 Telecom	RUR	STS-1 Telecom Bus – TxFIFO Underrun Interrupt Status – Channel 0:
	Bus # 0 – TxFIFO Underrun Interrupt Status		This RESET-upon-READ bit-field indicates whether or not "STS-1 Telecom Bus – Channel 0" has declared a "TxFIFO Underrun" Interrupt since the last read of this register.
			0 – Indicates that "STS-1 Telecom Bus – Channel 0" has NOT declared a "TxFIFO Underrun" interrupt since the last read of this register.
			1 – Indicates that "STS-1 Telecom Bus – Channel 0" has declared a "TxFIFO Overrun" Interrupt since the last read of this register.
			Note: This bit-field is only active if "STS-1 Telecom Bus – Channel 0" has been enabled.
	The	produ data	"TxFIFO Overrun" Interrupt since the last read of this register. Note: This bit-field is only active if "STS-1 Telecom Bus – Channel 0" has been enabled.

Rev 2.0.0

Table 36: Interface Control Register – STS-1/STM-0 Telecom Bus FIFO Interrupt Enable Register (Address Location= 0x013F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Unused	STS-1 Telecom Bus # 2 Tx Overrun Interrupt Enable	STS-1 Telecom Bus # 2 Tx Underrun Interrupt Enable	STS-1 Telecom Bus # 1 Tx Overrun Interrupt Enable	STS-1 Telecom Bus # 1 Tx Underrun Interrupt Enable	STS-1 Telecom Bus # 0 Tx Overrun Interrupt Enable	STS-1 Telecom Bus # 0 Tx Underrun Interrupt Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7	Unused	R/O	in the
6	Unused	R/O	9, 430
O.	STS-1 Telecom Bus # 2 TxFIFO Overrun Interrupt Enable		STS-1 Telecom Bus - TxFIFO Overrun Interrupt Enable - Channel 2: This READ/WRITE bit-field permits the user to either enable or disable the "TxFIFO Overrun" Interrupt, associated with STS-1 Telecom Bus - Channel 2. If the user enables this interrupt, then the "STS-1 Telecom Bus - Channel 2" will generate an interrupt anytime it declares the "TxFIFO Overrun" condition. 0 - Disables the "TxFIFO Overrun" Interrupt, associated with "STS-1 Telecom Bus - Channel 2. 1 Enables the "TxFIFO Overrun" Interrupt, associated with "STS-1 Telecom Bus - Channel 2. Note: This bit-field is only active if "STS-1 Telecom Bus - Channel 2" has been enabled.
4	STS-1 Telecom Bus # 2 TxFIFO Underrun Interrupt Enable	JIBW S	This READ/WRITE bit-field permits the user to either enable or disable the "TxFIFO Underrun" Interrupt, associated with STS-1 Telecom Bus — Channel 2. If the user enables this interrupt, then the "STS-1 Telecom Bus — Channel 2" will generate an interrupt anytime it declares the "TxFIFO Underrun" condition. 0 — Disables the "TxFIFO Underrun" Interrupt, associated with "STS-1 Telecom Bus — Channel 2. 1 — Enables the "TxFIFO Underrun" Interrupt, associated with "STS-1 Telecom Bus — Channel 2. Note: This bit-field is only active if "STS-1 Telecom Bus — Channel 2" has been enabled.
3	STS-1 Telecom Bus # 1 TxFIFO Overrun Interrupt Enable	R/W	STS-1 Telecom Bus – TxFIFO Overrun Interrupt Enable – Channel 1: This READ/WRITE bit-field permits the user to either enable or disable the "TxFIFO Overrun" Interrupt, associated with STS-1 Telecom Bus – Channel 1. If the user enables this interrupt, then the "STS-1 Telecom Bus – Channel 1" will generate an interrupt anytime it declares the "TxFIFO Overrun" condition. 0 – Disables the "TxFIFO Overrun" Interrupt, associated with "STS-1 Telecom Bus – Channel 1. 1 – Enables the "TxFIFO Overrun" Interrupt, associated with "STS-1

			Telecom Bus – Channel 1.
			Note: This bit-field is only active if "STS-1 Telecom Bus – Channel 1" has been enabled.
2	STS-1 Telecom	R/W	STS-1 Telecom Bus – TxFIFO Underrun Interrupt Enable – Channel 1:
	Bus # 1 TxFIFO Underrun Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "TxFIFO Underrun" Interrupt, associated with STS-1 Telecom Bus – Channel 1. If the user enables this interrupt, then the "STS-1 Telecom Bus – Channel 1" will generate an interrupt anytime it declares the "TxFIFO Underrun" condition.
			0 - Disables the "TxFIFO Underrun" Interrupt, associated with "STS-1 Telecom Bus - Channel 1.
			1 - Enables the "TxFIFO Underrun" Interrupt, associated with "STS-1 Telecom Bus - Channel 1.
			Note: This bit-field is only active it STS Telecom Bus – Channel 1" has been enabled.
1	STS-1 Telecom	R/W	STS-1 Telecom Bus – TxFIFO Overrun Interrupt Enable – Channel 0:
	Bus # 0 TxFIFO Overrun Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "TxFIFO Overrun" Interrupt, associated with STS-1 Telecom Bus – Channel 0. If the user enables this interrupt, then the "STS-1 Telecom Bus – Channel 0" will generate an interrupt anytime it declares the "TxFIFO Overrun" condition.
			 0 - Disables the "TxFIFO Overrun" Interrupt, associated with "STS-1 Telecom Bus - Channel 0. 1 - Enables the "TxFIFO Overrun" Interrupt, associated with "STS-1 Telecom Bus - Channel 0.
			Note: This bit-field is only active if "STS-1 Telecom Bus – Channel 0" has been enabled.
0	STS-1 Telecom	R/W	STS-1 Telecom Bus – TxFIFO Underrun Interrupt Enable – Channel 0:
	Bus # 0 TxFIFO Underrun Interrupt Enable	nterrupt	This READ/WRITE bit-field permits the user to either enable or disable the "TxFIFO Underrun" Interrupt, associated with STS-1 Telecom Bus – Channel 3. If the user enables this interrupt, then the "STS-1 Telecom Bus – Channel 0" will generate an interrupt anytime it declares the "TxFIFO Underrun" condition.
	the	10	Disables the "TxFIFO Underrun" Interrupt, associated with "STS-1 Velecom Bus – Channel 0.
	8	and	1 - Enables the "TxFIFO Underrun" Interrupt, associated with "STS-1 Telecom Bus - Channel 0.
			Note: This bit-field is only active if "STS-1 Telecom Bus – Channel 0" has been enabled.

Table 37: Operation General Purpose Input/Output Register – Byte 0 (Address Location= 0x0147)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
GPIO_7	GPIO_6	GPIO_5	GPIO_4	GPIO_3	GPIO_2	GPIO_1	GPIO_0
R/W							
0	0	0	0	0	0	0	0

7	GPIO_7	R/W	General Purpose Input/Output Pin # 7: The exact function of this READ/WRITE bit-field depends upon whether the "GPIO_7" pin is configured to be an input or an output pin.
			If GPIO_7 is configured to be an input pin:
			If GPIO_7 is configured to be an input pin, then this register bit operates as a READ-ONLY bit-field that reflects the state of the "GPIO_7" (pin number AA25) input pin.
			If the "GPIO_7" input pin is pulled to a logic "HIGH", then this register bit will be set to "1". Conversely, if the "GPIO_7" input pin is pulled to a logic "LOW", then this register bit will be set to "0".
			If GPIO_7 is configured to be an output pin:
			If GPIO_7 is configured to be an output pin, then the user can control the logic level of "GPIO_7" by writing the appropriate value into this bit-field.
			Setting this bit-field to "0" causes the GPIO_7 output pin to be driven "LOW". Conversely, setting this bit-field to "1" causes the GPIO_7 output pin to be driven "HIGH".
			Note: This register bit-field is only active if STS-1 Telecom Bus – Channel 2 is enabled.
6	GPIO_6	R/W	General Purpose Input/Output Pin # 6:
			The exact function of this READ/WRITE bit-field depends upon whether the "GPIO_6" pin is configured to be an input or an output pin.
		000	If GRIO_6 is configured to be an input pin:
	the	ro K	If GPIO_6 is configured to be an input pin, then this register bit operates as a READ-ONLY bit-field that reflects the state of the "GPIO_6" (pin number W24) input pin.
	8	and	If the "GPIO_6" input pin is pulled to a logic "HIGH", then this register bit will be set to "1". Conversely, if the "GPIO_6" input pin is pulled to a logic "LOW", then this register bit will be set to "0".
			If GPIO_6 is configured to be an output pin:
			If GPIO_6 is configured to be an output pin, then the user can control the logic level of "GPIO_6" by writing the appropriate value into this bit-field.
			Setting this bit-field to "0" causes the GPIO_6 output pin to be driven "LOW". Conversely, setting this bit-field to "1" causes the GPIO_6 output pin to be driven "HIGH".
			Note: This register bit-field is only active if STS-1 Telecom Bus – Channel 2 is enabled.
5	GPIO_5	R/W	General Purpose Input/Output Pin # 5:
			The exact function of this READ/WRITE bit-field depends upon whether the "GPIO_5" pin is configured to be an input or an output pin.

			If GPIO_5 is configured to be an input pin:			
			If GPIO_5 is configured to be an input pin, then this register bit operates as a READ-ONLY bit-field that reflects the state of the "GPIO_5" (pin number AC26) input pin.			
			If the "GPIO_5" input pin is pulled to a logic "HIGH", then this register bit will be set to "1". Conversely, if the "GPIO_5" input pin is pulled to a logic "LOW", then this register bit will be set to "0".			
			If GPIO_5 is configured to be an output pin:			
			If GPIO_5 is configured to be an output pin, then the user can control the logic level of "GPIO_5" by writing the appropriate value into this bit-field.			
			Setting this bit-field to "0" causes the GPIO_5 output pin to be driven "LOW". Conversely, setting this bit-field to "1" causes the GPIO_5 output pin to be driven "HIGH".			
			Note: This register bit-field is only active it STS-1 Telecom Bus – Channel 1 is enabled.			
4	GPIO_4	R/W	General Purpose Input/Output Pin #4:			
			The exact function of this READ/WRITE bit-field depends upon whether the "GPIO_4" pin is configured to be an input or an output pin.			
			If GPIO_4 is configured to be an input pin:			
			If GPIO_4 is configured to be an input pin, then this register bit operates as a READ-ONLY bit-field that reflects the state of the "GPIO_4" (pin number Y25) input pin.			
			If the "GPIO_4" input pin is pulled to a logic "HIGH", then this register bit will be set to "1". Conversely, if the "GPIO_4" input pin is pulled to a logic "LOW", then this register bit will be set to "0".			
			If GPIO_4,is configured to be an output pin:			
			If GPIO_4 is configured to be an output pin, then the user can control the logic level of "GPIO_4" by writing the appropriate value into this bit-field.			
		۷	Setting this bit-field to "0" causes the GPIO_4 output pin to be driven "LOW". Conversely, setting this bit-field to "1" causes the GPIO_4 output pin to be driven "HIGH".			
		orol	Note: This register bit-field is only active if STS-1 Telecom Bus – Channel 1 is enabled.			
3	GPIO_3	P/W	General Purpose Input/Output Pin # 3:			
		gar	The exact function of this READ/WRITE bit-field depends upon whether the "GPIO_3" pin is configured to be an input or an output pin.			
		.0.	If GPIO_3 is configured to be an input pin:			
			If GPIO_3 is configured to be an input pin, then this register bit operates as a READ-ONLY bit-field that reflects the state of the "GPIO_3" (pin number AB26) input pin.			
			If the "GPIO_3" input pin is pulled to a logic "HIGH", then this register bit will be set to "1". Conversely, if the "GPIO_3" input pin is pulled to a logic "LOW", then this register bit will be set to "0".			
			If GPIO_3 is configured to be an output pin:			
			If GPIO_3 is configured to be an output pin, then the user can control the logic level of "GPIO_3" by writing the appropriate value into this bit-field.			
			Setting this bit-field to "0" causes the GPIO_3 output pin to be driven "LOW". Conversely, setting this bit-field to "1" causes the GPIO_3 output pin to be driven "HIGH".			

			Note: This register bit-field is only active if STS-1 Telecom Bus – Channel 1 is enabled.
2	GPIO_2	R/W	General Purpose Input/Output Pin # 2:
			The exact function of this READ/WRITE bit-field depends upon whether the "GPIO_2" pin is configured to be an input or an output pin.
			If GPIO_2 is configured to be an input pin:
			If GPIO_2 is configured to be an input pin, then this register bit operates as a READ-ONLY bit-field that reflects the state of the "GPIO_2" (pin number V23) input pin.
			If the "GPIO_2" input pin is pulled to a logic "HIGH", then this register bit will be set to "1". Conversely, if the "GPIO_2" input pin is pulled to a logic "LOW", then this register bit will be set to "0".
			If GPIO_2 is configured to be an output pin:
			If GPIO_2 is configured to be an output pin, then the user can control the logic level of "GPIO_2" by writing the appropriate value into this bit-field.
			Setting this bit-field to "0" causes the GPIO_2 output pin to be driven "LOW". Conversely, setting this bit-field to "1" causes the GPIO_2 output pin to be driven "HIGH".
			Note: This register bit-field is only active if STS-1 Telecom Bus – Channel 0 is enabled.
1	GPIO_1	R/W	General Purpose Input/Output Pin # 1:
			The exact function of this READ/WRITE bit-field depends upon whether the "GPIO_1" pin is configured to be an input or an output pin.
			If GPIO_1 is configured to be an input pin:
			If GPIO_1 is configured to be an input pin, then this register bit operates as a READ ONLY bit-field that reflects the state of the "GPIO_1" (pin number AC27) input pin.
			If the "GPIO_1" input pin is pulled to a logic "HIGH", then this register bit will be set to "1". Conversely, if the "GPIO_1" input pin is pulled to a logic "LOW", then this register bit will be set to "0".
		90	GPIO_1 is configured to be an output pin:
		in she	If GPIO_1 is configured to be an output pin, then the user can control the logic level of "GPIO_1" by writing the appropriate value into this bit-field.
	The	grand	Setting this bit-field to "0" causes the GPIO_1 output pin to be driven "LOW". Conversely, setting this bit-field to "1" causes the GPIO_1 output pin to be driven "HIGH".
		' O'	Note: This register bit-field is only active if STS-1 Telecom Bus – Channel 0 is enabled.
0	GPIO_0	R/W	General Purpose Input/Output Pin # 0:
			The exact function of this READ/WRITE bit-field depends upon whether the "GPIO_0" pin is configured to be an input or an output pin.
			If GPIO_0 is configured to be an input pin:
			If GPIO_0 is configured to be an input pin, then this register bit operates as a READ-ONLY bit-field that reflects the state of the "GPIO_0" (pin number W25) input pin.
			If the "GPIO_0" input pin is pulled to a logic "HIGH", then this register bit will be set to "1". Conversely, if the "GPIO_0" input pin is pulled to a logic "LOW", then this register bit will be set to "0".
			then this register bit will be set to 0.

Rev 2.0.0

	If GPIO_0 is configured to be an output pin:			
	If GPIO_0 is configured to be an output pin, then the user can control the logic level of "GPIO_0" by writing the appropriate value into this bit-field.			
	Setting this bit-field to "0" causes the GPIO_0 output pin to be driven "LOW". Conversely, setting this bit-field to "1" causes the GPIO_0 output pin to be driven "HIGH".			
	Note: This register bit-field is only active if STS-1 Telecom Bus – Channel 0 is enabled.			

The product are no longered (OBS)

The product are no longered (OBS)

The product are no longered (OBS)

Table 38: Operation General Purpose Input/Output Direction Register 0 (Address Location= 0x014B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	GPIO_DIR[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION
7	GPIO_DIR[7]	R/W	GPIO_7 Direction Select:
			This READ/WRITE bit-field permits the user to configure the "GPIO_7" pin (pin number AA25) to function as either an input or an output pin.
			0 – Configures GPIO_7 to function as an input pin.
			1 – Configures GPIO_7 to function as an output pin.
			Note: This register bit-field is only active if STS-1 Telecom Bus Interface – Channel 2 is enabled.
6	GPIO_DIR[6]	R/W	GPIO_6 Direction Select.
			This READ/WRITE bit field permits the user to configure the "GPIO_6" pin (pin number W24) to function as either an input or an output pin.
			0 – Configures GPIO_6 to function as an input pin.
			1 – Configures GPIO 6 to function as an output pin.
			Note: This register bit-field is only active if STS-1 Telecom Bus Interface – Channel 2 is enabled.
5	GPIO_DIR[5]	R/W	GPIO_5 Direction Select:
			This READ/WRITE bit-field permits the user to configure the "GPIO_5" pin (pin number AC26) to function as either an input or an output pin.
			0 Configures GPIO_5 to function as an input pin.
		AUG	1- Configures GPIO_5 to function as an output pin.
	•	log hee	Note: This register bit-field is only active if STS-1 Telecom Bus Interface – Channel 1 is enabled.
4	GPIO_DIR[4]	R/W	GPIO_4 Direction Select:
	1,9	ardli	This READ/WRITE bit-field permits the user to configure the "GPIO_4" pin (pin number Y25) to function as either an input or an output pin.
		'0'	0 – Configures GPIO_4 to function as an input pin.
			1 – Configures GPIO_4 to function as an output pin.
			Note: This register bit-field is only active if STS-1 Telecom Bus Interface – Channel 1 is enabled.
3	GPIO_DIR[3]	R/W	GPIO_3 Direction Select:
			This READ/WRITE bit-field permits the user to configure the "GPIO_3" pin (pin number AB26) to function as either an input or an output pin.
			0 – Configures GPIO_3 to function as an input pin.
			1 – Configures GPIO_3 to function as an output pin.
			Note: This register bit-field is only active if STS-1 Telecom Bus Interface – Channel 1 is enabled.

EXARExperience *Qur* Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

GPIO_DIR[2]	R/W	GPIO_2 Direction Select:				
		This READ/WRITE bit-field permits the user to configure the "GPIO_2" pin (pin number V23) to function as either an input or an output pin.				
		0 – Configures GPIO_2 to function as an input pin.				
		1 – Configures GPIO_2 to function as an output pin.				
		Note: This register bit-field is only active if STS-1 Telecom Bus Interface – Channel 0 is enabled.				
GPIO_DIR[1]	R/W	GPIO_1 Direction Select:				
		This READ/WRITE bit-field permits the user to configure the "GPIO_1" pin (pin number AC27) to function as either an input or an output pin.				
		0 – Configures GPIO_1 to function as an input pin.				
		1 – Configures GPIO_1 to function as an output pin.				
		Note: This register bit-field is only active if STS-1 Telecom Bus Interface – Channel 0 is enabled.				
GPIO_DIR[0]	R/W	GPIO_0 Direction Select:				
		This READ/WRITE bit-field permits the user to configure the "GPIO_0" pin (pin number W25) to function as either an input or an output pin.				
		0 – Configures GPIO_0 to function as an input pin.				
		1 – Configures GPIO 0 to function as an output pin.				
		Note: This register bit field is only active if STS-1 Telecom Bus Interface – Channel 0 is enabled.				
	GPIO_DIR[1] GPIO_DIR[0]	GPIO_DIR[1] R/W GPIO_DIR[0] R/W				

Table 39: Operation Output Control Register – Byte 1 (Address Location= 0x0150)

В	IT 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
STU	Hz or FF Out able	8kHz OUT Select	Egress Direction Monitored – STUFF Output			Unused		
R	R/W	R/W	R/W	R/O	R/O	R/O	R/O	R/O
	0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре		DESCRIPTION					
7	8kHz or STUFF Out Enable	R/W	8kHz or STUFF Output Enable – LOF Output Pin: This READ/WRITE bit-field, along with Bit 6 (8kHz OUT Select) permits the user to define the role of the LOF output pin (pin AD11). The relationship between the states of these bit-fields and the corresponding role of the LOF output pin is presented below.						
			Bit 7 (8kHz Bit 6 (8kHz Role of LOF output pi or STUFF OUT Select)						
			0	0,00	OF or AIS-L Indicator				
			0	4 CD LO	OF or AIS-L Indicator				
			1,110,101	В	it Stuff Indicator Output				
			10,000,10	1 8	kHz Output				
6	8kHz OUT Select	Heet a	Note: 1. If Bit Ds set to "0", then Bit 1 (AIS-L Output Enable) within the STS-3 Transport — Auto AIS (in Downstream STS-1s) Control (Address Location= 0x116B) will indictate whether or not pin AI "LOF" or the "AIS-L" output indicator. 2. If Bit 1 (AIS-L Output Enable) is set to "0", then pin AD11 wi as the LOF output indicator. 3. If Bit 1 (AIS-L Output Enable) is set to "1", then pin AD11 wi as the AIS-L output indicator. R/W 8kHz OUT – LOF Output Pin: This READ/WRITE bit-field, along with Bit 6 (8kHz OUT Select the user to define the role of the LOF output pin (pin AD1 relationship between the states of these bit-fields and the correct role of the LOF output pin is presented below.						
			Bit 7 (8kHz or STUFF Out Select) 0						
			0	1	LOF or AIS-L Indicator				
			1	0	Bit Stuff Indicator Output				
			1	1	8kHz Output				

EXARExperience *Qur* Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

5	Egress Direct	R/W	Egress Direction Monitored – STUFF Output:
	Monitored –STUFF Output		If the LOF output pin has been configured to function as a "STUFF Indicator" output, then it can be configured to reflect the current stuff opportunities of the channel designated by Bits 7 through 4 (Stuff Indicator Channel Select[3:0]) within the Operation Output Control Register – Byte 0.
			This READ/WRITE bit-field permits the user to configure the LOF output pin to either reflect the "current stuff opportunities" for the Ingress or Egress Path of the selected channel.
			0 – Configures the LOF output pin to reflect the "current stuff opportunity" of the Ingress Path of the "selected" channel.
			1 – Configures the LOF output pin to reflect the "current stuff opportunity" of the Egress Path of the "selected" channel.
			Note: This bit-field will be ignored if the "selected" channel has been configured to operate in the STS-7 Mode.
4 – 0	Unused	R/O	in city
	the	ata and a	Lor products in being than the city. Lor products in being the condered (OBS) Later to be ordered (OBS) Later to be ordered (OBS) Later to be ordered (OBS)

Table 40: Operation Output Control Register – Byte 0 (Address Location= 0x0153)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused		Stuff Indicator Channel Select[1:0]		Unused		8kHz Source Channel Select[1:0]	
R/O	R/O	R/W	R/W	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 6	Unused	R/O	
5 – 4	Stuff Indicator	R/W	Stuff Indicator – Channel Select[1:0]:
	Channel Select[1:0]		These two (2) READ/WRITE bit-fields permit the user to identify which of the 3 channels should have their "bit-stuff opportunity" status reflected on the LOF output pin.
			Setting these bit-fields to [0, 0] configures the LOF output pin to reflect the bit-stuff opportunity status of Channel 0. Likewise, setting these bit-fields to [1, 0] configures the LOF output pin to reflect the bit-stuff opportunity status of Channel 2.
			Note: These bit-fields are ignored if any of the following are true.
			1. If the corresponding channel has been configured to operate in the STS-1 Mode.
			2. If the LOF output pin has been configured to function as the LOF or AIS-L indicator output.
			3 If the LOF output pin has been configured to function as an 8kHz output pin.
3 – 2	Unused	R/O	20 19g
1 – 0	8kHz Source Channel	R/W	8kHz Source Channel Select[1:0]:
	Select[1:0]	est of	If the LOF output pin has been configured to output an 8kHz clock output signal, then the XRT94L33 will derive this 8kHz clock signal, from the Ingress DS3/E3 or Receive STS-1 signal of the "Selected" channel.
	8kHz Source Channel Select[1:0]	Way	These two(2) READ/WRITE bit-fields permit the user to specify the "Selected" channel.
			Setting these bit-fields to [0, 0] configures the LOF output pin to output an 8kHz clock signal, that is derived from the Ingress DS3/E3 or Receive STS-1 input signal of Channel 0. Likewise, setting these bit-fields to [1, 0] configures the LOF output pin to reflect the bit-stuff opportunity status of Channel 2.
			Note: These bit-fields are ignored if any of the following are true.
			1. If the LOF output pin has been configured to function as the LOF or AIS-L indicator output.
			2. If the LOF output pin has been configured to function as the "Stuff Indicator" output pin.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 41: Operation Slow Speed Port Control Register – Byte 1 (Address Location= 0x0154)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
SSI Enable	SSI Insert	SSI Force Zero	Unused	SSE Enable	SSE Insert	SSE Force Zero	Unused
R/W	R/W	R/W	R/O	R/W	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	SSI Enable	R/W	Slow-Speed Ingress – Interface Port Enable:
			This READ/WRITE bit-field permits the user to enable or disable the SSI (Slow-Speed Ingress) Interface Port.
			If the SSI Interface port is enabled, then it can be used to either monitor (e.g., extract) or to replace (e.g., insert) a DS3, E3 or STS-1 signal, into the Ingress DS3/E3 or Receive STS-1 path of the "Selected" channel.
			0 – Disables the SSI Interface Port.
			1 – Enables the SSI Interface Port
6	SSI Insert	R/W	Slow-Speed Ingress - Interface Port - Insert:
			This READ/WRITE bit-field permits the user to configure the SSI Interface port to either monitor (e.g., extract) an "Ingress DS3/E3" or "Receive STS-1" signal, or to replace (e.g., insert) a DS3, E3 or STS-1 signal into the Ingress DS3/E3 or Receive STS-1 path of the "Selected" channel.
			If the user configures the SSI Interface port to monitor a given DS3, E3 or STS-1 signal, then the SSI Interface will then be configured to be an "output" interface. In this case, the SSI Interface port will consist of an "SSI_POS", "SSI_NEG" and "SSI_CLK" output signals. Additionally, a copy of the Ingress DS3/E3 or Receive STS-1 signal will be output via this output port.
		orodu	If the user configures the SSI Interface port to replace (e.g., insert) an "Ingress DS3/E3" or Receive STS-1 signal, then the SSI Interface will then be configured to be an "input" interface. In this case, the SSI Interface port will consist of an "SSI_POS", "SSI_NEG" and "SSI_CLK" input signals. Additionally, the DS3, E3 or STS-1 signal, that is applied at this input port will overwrite that of the "Ingress DS3/E3" or the Receive STS-1 signal.
	The	10	Configures the SSI Interface as an output port that will permit the user to monitor the "selected" Ingress DS3/E3 or Receive STS-1 signal.
	•	gastic	1 – Configures the SSI Interface as an input port. In this configuration, the DS3, E3 or STS-1 signal that is input via this port will replace/overwrite the "Ingress" DS3/E3 or Receive STS-1 signal, within the "selected" channel, prior to being mapped into STS-3.
			Note: This bit-field will be ignored if the SSI Interface port is disabled.
5	SSI Force Zero	R/W	Slow Speed Ingress – Interface Port – Force to All Zeros:
			This READ/WRITE bit-field permits the user to force the Ingress DS3/E3 or Receive STS-1 signal, within the "selected" channel to an "All Zeros" pattern.
			0 – Configures the Ingress DS3/E3 or Receive STS-1 signal (within the "selected" channel) to flow to the DS3/E3 Mapper Block or to the Transmit SONET POH Processor block, in a normal manner.
			1 - Forces the data, within the Ingress DS3/E3 or Receive STS-1 signal (within the "selected" channel) to an "All Zeros" pattern.

			Note: This bit-field will be ignored if the SSI Interface port is disabled.
4	Unused	R/O	
3	SSE Enable	R/W	Slow-Speed Egress – Interface Port Enable:
			This READ/WRITE bit-field permits the user to enable or disable the SSE (Slow Speed Egress) Interface Port.
			If the SSE Interface port is enabled, then it can be used to either monitor (e.g., extract) or to replace (e.g., insert) a DS3, E3 or STS-1 signal, into the Egress DS3/E3 or Transmit STS-1 path of the "Selected" channel.
			0 – Disables the SSE Interface Port
			1 – Enables the SSE Interface Port.
2	SSE Insert	R/W	Slow Speed Egress – Interface Port – Insert:
			This READ/WRITE bit-field permits the user to configure the SSE Interface port to either monitor (e.g., extract) an "Egress DS3/E3" or "Receive STS-1" signal, or to replace (e.g., insert) a DS3, E3 or STS-1 signal into the Egress DS3/E3 or Transmit STS-1 path of the "Selected" channel.
			If the user configures the SSE Interface port to monitor a given DS3, E3 or STS-1 signal, then the SSE Interface will then be configured to be an "output" interface. In this case, the SSE Interface port will consist of an "SSE_POS", "SSE_NEG" and "SSE_CLK" output signals. Additionally, a copy of the Egress DS3/E3 or Transmit STS-1 signal will be output via this output port.
			If the user configures the SSE Interface port to replace (e.g., insert) an "Egress DS3/E3" or Transmit STS-1 signal, then the SSE Interface will then be configured to be an "input" interface. In this case, the SSE Interface port will consist of an "SSE_POS", "SSE_NEG" and "SSE_CLK" input signals. Additionally, the DS3, E3 or STS-1 signal, that is applied at this input port will overwrite that of the "Egress DS3/E3" or the Transmit STS-1 signal. 0 - Configures the SSE Interface as an output port that will permit the user to monitor the "selected" Egress DS3/E3 or Transmit STS-1 signal.
	,(duct	1 Configures the SSE Interface as an input port. In this configuration, the DS3, E3 or STS-1 signal, that is input via this port will replace/overwrite the "Egress" DS3/E3 or Transmit STS-1 signal, within the "selected" channel, prior to being mapped into STS-3.
	6,	50	Note: This bit-field will be ignored if the SSE Interface port is disabled.
1	SSE Force Zero	R/W	Slow Speed Egress – Interface Port – Force to All Zeros:
	, 9,0	ano	This READ/WRITE bit-field permits the user to force the Egress DS3/E3 or Transmit STS-1 signal, within the "selected" channel to an "All Zeros" pattern.
			0 - Configures the Egress DS3/E3 or Transmit STS-1 signal (within the "selected" channel) to flow to the DS3/E3/STS-1 LIU IC in a normal manner.
			1 - Forces the data, within the Egress DS3/E3 or Transmit STS-1 signal (within the "selected" channel) to an "All Zeros" pattern.
			Note: This bit-field will be ignored if the SSE Interface port is disabled.
0	Unused	R/O	

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 42: Operation Slow Speed Port Control Register – Byte 0 (Address Location= 0x0157)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unu	ised	SSI_Channel_Select[1:0]		Unused		SSE_Channel_Select[1:0]	
R/O	R/O	R/W	R/W	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 6	Unused	R/O	
5 – 4			Slow-Speed Ingress – Interface Port – Channel Select[1:0]:
	1:0]:		These READ/WRITE bit-fields permit the user to select which of the 3 Ingress DS3/E3 or Receive STS-1 signals will be processed via the SSI Interface port.
			Setting SSI_Channel_Select[1:0] to [0,0] configures the SSI Interface port to process the Ingress DS3/E3 or Receive STS-1 signal associated with Channel 0. Likewise, setting SSI_Channel_Select[1:0] to [1, 0] configures the SSI Interface port to process the Ingress DS3/E3 or Receive STS-1 signal associated with Channel 2.
			Note: These bit-fields are ignored if the SSI Interface port is disabled.
3 –2	Unused	R/O	El relias
1 – 0	SSE_Channel_Select [1:0]	R/W	Slow Speed Egress – Interface Port – Channel Select[1:0]: These READ/WRITE bit-fields permit the user to select which of the 3 Egress DS3/E3 or Receive STS-1 signals will be processed via the SSE Interface port. Setting SSE_Channel_Select[1:0] to [0, 0] configures the SSE Interface port to process the Egress DS3/E3 or Transmit STS-1 signal associated with Channel 0. Likewise, setting SSE_Channel_Select[1:0] to [1, 0] configures the SSE Interface port to process the Egress DS3/E3 or Transmit STS-1 signal associated with Channel 2. Note: These bit-fields are ignored if the SSE Interface port is disab led.
	The	atandr	

Table 43: Operation – DS3/E3/STS-1 Clock Frequency Out of Range Detection – Direction Register (Address Location= 0x0158)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			Unused				ON_EGRESS DIRECTION
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT Number	Nаме	Түре	DESCRIPTION
7 – 1	Unused	R/O	
0	ON_EGRESS_DIRECTION	R/W	Frequency Out of Range Detection on Egress Direction: This READ/WRITE bit-field permits the user to configure the "DS3/E3/STS-1 Clock Frequency — Out of Range Detector" to operate in either the Ingress or Egress direction. 0 — Configures the DS3/E3/STS-1 Clock Frequency — Out of Range Detector" to operate on the DS3, E3 or STS-1 clock signals in the Ingress Direction. 1 — Configures the DS3/E3/STS-1 Clock Frequency — Out of Range Detector" to operate on the DS3, E3 or STS-1 clock signals in the Egress Direction.

Table 44: Operation – DS3/E3/STS-1Clock Frequency – DS3 Out of Range Detection Threshold Register (Address Location= 0x015A)

Віт 7	Віт 6	Віт 5	Вл 4	Віт 3	Віт 2	Віт 1	Віт 0			
	DS3_OUT_OF_RANGE_DETECTION_THRESHOLD[7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0	0	00 0	0	0	0	0	0			

BIT Number	NAME	Түре	DESCRIPTION
7 – 0	DS3_OUT_OF_RANGE_ DETECTION_THR	R/W	DS3 Out of Range – Detection Threshold[7:0]: These eight READ/WRITE bit-fields permit the user to define (in terms of ppm) the frequency difference that must exist between a given DS3 signal (in either the Ingress or Egress direction) and that of the REFCLK45 input clock signal; before the XRT94L33 will declare a "DS3 Clock Frequency – Out of Range" condition.



Table 45: Operation – DS3/E3/STS-1Clock Frequency – STS-1/E3 Out of Range Detection Threshold Registers (Address Location= 0x015B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
STS-1/E3_OUT_OF_RANGE_DETECTION_THRESHOLD[7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT Number	NAME	Түре	DESCRIPTION
7-0	STS1/E3_OUT_OF_RAN GE_DETECTION_THR	R/W	STS-1/E3 Out of Range – Detection Threshold[7:0]: These eight READ/WRITE bit-fields permit the user to define (in terms of ppm) the frequency difference that must exist between a given STS-1 or E3 signal (in either the Ingress or Egress direction) and that of the REFCLK51/REFCLK34 input clock signal; before the XRT94L33 will declare a STS-1/E3 Clock Frequency – Out of Range" condition.

Table 46: Operation – DS3/E3/STS-1 Frequency Out of Range Interrupt Enable Register – Byte 0 (Address Location=0x015D)

					A		
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Unused		ducts	Out of Range – Channel 2 Interrupt enable	Out of Range – Channel 1 Interrupt Enable	Out of Range – Channel 0 Interrupt Enable
R/O	R/O	R/O	R/O	R/0	R/W	R/W	R/W
0	0	0	0	0	0	0	0

	1	10,	N OF
BIT NUMBER	NAME	Түре	DESCRIPTION
7-3	Unused	R/O	
2	Out of Range – Channel 2 Interrupt Enable	A 7	DS3/E3/STS-1 Frequency – Out of Range – Channel 2 – Interrupt Enable:
	Interrupt Enable	Mar	This READ/WRITE bit-field permits the user to either enable or disable the "DS3/E3/STS-1 Frequency – Out of Range" Interrupt for Channel 2.
	♂		If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the frequency of the DS3, E3 or STS-1 signal (in the selected direction – Ingress or Egress) within Channel 2, differs from its corresponding Reference Clock signal (e.g., REFCLK45, REFCLK34 or REFCLK51) by its "Out of Range Detection Threshold" (in terms of ppm) or more.
			0 - Disables the "DS3/E3/STS-1 Frequency - Out of Range" Interrupt for Channel 2.
			1 - Enables the "DS3/E3/STS-1 Frequency - Out of Range" Interrupt for Channel 2.
1	Out of Range – Channel 1 Interrupt Enable	R/W	DS3/E3/STS-1 Frequency – Out of Range – Channel 1 – Interrupt Enable:
			This READ/WRITE bit-field permits the user to either enable or disable the "DS3/E3/STS-1 Frequency – Out of Range" Interrupt

		for Channel 1.
		If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the frequency of the DS3, E3 or STS-1 signal (in the selected direction – Ingress or Egress) within Channel 1, differs from its corresponding Reference Clock signal (e.g., REFCLK45, REFCLK34 or REFCLK51) by its "Out of Range Detection Threshold" (in terms of ppm) or more.
		0 - Disables the "DS3/E3/STS-1 Frequency - Out of Range" Interrupt for Channel 1.
		1 - Enables the "DS3/E3/STS-1 Frequency - Out of Range" Interrupt for Channel 1.
Out of Range – Channel 0 Interrupt Enable	R/W	DS3/E3/STS-1 Frequency – Out of Range – Channel 0 – Interrupt Enable:
		This READ/WRITE bit-field permits the user to either enable or disable the "DS3/E3/STS 1 Frequency – Out of Range" Interrupt for Channel 0.
		If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the frequency of the DS3, E3 or STS-1 signal (in the selected direction – Ingress or Egress) within Channel 0, differs from its corresponding Reference Clock signal (e.g., REFCLK45, REFCLK34 or REFCLK51) by its "Out of Range Detection Threshold" (in terms of ppm) or more.
		0 – Disables the "DS3/E3/STS-1 Frequency – Out of Range" Interrupt for Channel 0.
		1 Enables the "DS3/E3/STS-1 Frequency - Out of Range" Interrupt for Channel 0.
The product of and many	of Processing	Jondereo Se ordereo
	Interrupt Enable	

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 47: Operation – DS3/E3/STS-1 Frequency Out of Range Interrupt Status Register – Byte 0 (Address Location=0x015F)

Віт 7	Віт 6	Віт 5	Віт 5 Віт 4 Віт 3		Віт 2	Віт 1	Віт 0
Unused				Out of Range – Channel 2 Interrupt Status	Out of Range – Channel 1 Interrupt Status	Out of Range – Channel 0 Interrupt Status	
R/O	R/O	R/O	R/O	R/O	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7-3	Unused	R/O	
2	Out of Range – Channel 2 Interrupt Status	RUR	DS3/E3/STS-1 Frequency – Out of Range – Channel 2 – Interrupt Status: This RESET-Upon-READ bit-field indicates whether or not the XRT94L33 has declares the "DS3/E3/STS-1 Frequency – Out of Range" Interrupt for Channel 2, since the last read of this register.
			 0 - Indicates that the "DS3/E3/STS-1 Frequency - Out of Range" Interrupt for Channel 2 has NOT occurred since the last read of this register. 1 - Indicates that the "DS3/E3/STS-1 Frequency - Out of Range" Interrupt for Channel 2 has occurred since the last read of this register.
1	Out of Range – Channel 1 Interrupt Status	RUR	DS3/E3/STS-1 Frequency – Out of Range – Channel 1 – Interrupt Status: This RESET-Upon-READ bit-field indicates whether or not the XRT94L33 has declares the "DS3/E3/STS-1 Frequency – Out of Range" Interrupt for Channel 1, since the last read of this register. 0 – Indicates that the "DS3/E3/STS-1 Frequency – Out of Range" Interrupt for Channel 1 has NOT occurred since the last read of this register. 1 – Indicates that the "DS3/E3/STS-1 Frequency – Out of Range" Interrupt for Channel 1 has occurred since the last read of this register.
0	Out of Range – Channel 0 Interrupt Status	RUR	D\$3/E3/STS-1 Frequency – Out of Range – Channel 0 – Interrupt Status: This RESET-Upon-READ bit-field indicates whether or not the XRT94L33 has declares the "D\$3/E3/STS-1 Frequency – Out of Range" Interrupt for Channel 0, since the last read of this register. 0 – Indicates that the "D\$3/E3/STS-1 Frequency – Out of Range" Interrupt for Channel 0 has NOT occurred since the last read of this register. 1 – Indicates that the "D\$3/E3/STS-1 Frequency – Out of Range" Interrupt for Channel 0 has occurred since the last read of this register.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 48: APS Mapping Register (Address Location= 0x0180)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Protection	n Channel		Protected Channel				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7-4	Protection Channel	R/W	Protection Channel:
3-0	Protected Channel	R/W	Protected Channel:

Table 49: APS Control Register - 1:1 & 1:N Protection Map (Address Location= 0x0181)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Group Enable	APS Type	Timing	Receive Payload Bypass	Group Reset	Line Port In Use	APS Auto Switch Enable	APS Auto Switch
R/W	R/W	R/W	R/W	R/W	R/O	R/W	R/W
0	0	0	0	(A)	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Group Enable	R/W	Group Enable:
,	Group Enable	1000	this READ/WRITE bit-field permits the user to enable the APS for this group.
		(0)	1 Enables the APS for this group
		C	2 – Disables the APS for this group
6	APS Type	R/W	APS Type:
	e Pr	Sheat	This READ/WRITE bit-field permits the user to determine the type of APS for this group.
	KHO N		0 – Configures the type of APS to be 1+1
	9.0	70	1 – Configures the type of APS to be 1:N
5	Timing	P/W	Timing:
			This READ/WRITE bit-field permits the user to specify whether the protection or the protected channel should dominate the timing of transmit APS.
			0 – Protected channel dominates the timing
			1 – Protection Channel dominates the timing
4	Receive Payload	R/W	Receive Payload Bypass:
	Bypass		This READ/WRITE bit-field permits the user to bypass the receive payload of protection channel.
			0 – Receive payload is not bypassed.
			1 – Receive payload is bypassed.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

3	Group Reset	R/W	Group Reset:					
			This READ/WRITE bit-field permits the user to reset the APS control and FIFO.					
			A "0" to "1" transition will cause the APS control and FIFO to be reset.					
2	Line Port In Use	R/O	Line Port In Use:					
			This READ-ONLY bit-field permits the user to check the current line port being in used for receiving OC3 data.					
			0 – Port 0 (main port) is the current line port in used					
			1 - Port 1 (backup port) is the current line port in used					
1	APS Auto Switch	R/W	APS Auto Switch Enable:					
	Enable		This READ/WRITE bit-field permits the user to configure the XRT94L33 to automatically switch from the "Primary" to the "Redundant" port, whenever the Receive STS-3 TOH Processor block declares an LOS (Loss of Signal) condition.					
			0 – Disables the APS Auto Switch feature. In this mode, the XRT94L33 will not automatically switch from the "Primary" port to the "Redundant" port, whenever the Receive STS-3 TOH Processor block declares an LOS condition.					
			1 – Enables the APS Auto Switch feature					
0	APS Switch	R/W	APS Switch: This READ/WRITE bit-field permits the user to command an APS switch (from one port to the other) via software control.					
			0 - Configures the Receive STS-3 TOH Processor block to use the "Primary Receive" Port. 1 - Configures the Receive STS-3 TOH Processor block to use the					
			"Redundant Receive" Port.					
	"Primary Receive" Port. 1 — Configures the Receive STS-3 TOH Processor block to use the "Redundant Receive" Port.							

Table 50: APS Status Register (Address Location= 0x0194)

	Віт 7	Віт 7 Віт 6 Віт 5		Віт 5 Віт 4		Віт 2	Віт 1	Віт 0
	Unused		Receive APS Parity Enable	Receive APS Transmit AP Parity Type Parity Enable		Transmit APS Parity Type	Transmit APS Parity Error	Receive APS Parity Error
Ī	R/O	R/O	R/W	R/W	R/W	R/W	R/O	R/O
Ī	0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7-6	Unused	R/O	
5	Receive APS Parity	R/W	Receive APS Parity Enable:
	Enable		This READ/WRITE bit-field permits the user to enable receive APS parity check.
			0 – Disables receive APS parity check
			1 – Enables receive APS parity check
4	Receive APS Parity	R/W	Receive APS Parity Type
	Туре		This READ/WRITE bit-field permits the user to specify the type of parity used for receive APS.
			0 – Even parity is used
			1 – Odd parity is used
3	Transmit APS Parity	R/W	Transmit APS Parity Enable:
	Enable	Ç	This READ/WRITE bit-field permits the user to enable transmit APS parity check
		10	0 Disables transmit APS parity check
			1 – Enables transmit APS parity check
2	Transmit APS Parity Type	R/W	Transmit APS Parity Type:
	Туре	S, C	This READ/WRITE bit-field permits the user to specify the type of parity used for transmit APS.
	100	3	0 – Even parity is used
	11, 31, 9		1 – Odd parity is used
1	Transmit APS Parity Error	R/O	Transmit APS Parity Error:
	Ellol		This READ-ONLY bit-field permits the user to check the parity error status in transmit APS module
			0 – Indicates "NO" parity error occurs
			1 – Indicates parity error occurs
0	Receive APS Parity	R/O	Receive APS Parity Error:
	Error		This READ-ONLY bit-field permits the user to check the parity error status in receive APS module
			0 – Indicates "NO" parity error occurs
			1 – Indicates parity error occurs

Table 51: APS Status Register (Address Location= 0x0196)

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Group Overflow Status [7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7-0	Group Overflow Status	R/O	Group Overflow Status:
			This READ/WRITE bit-field indicates whether or not a FIFO overflow has occurred in group n 1+1 APS protection channel.
			0 – Indicates "NO" FIFO overflow
			1 – Indicates a FIFO overflow

Table 52: APS Status Register (Address Location= 0x0197)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Group Underflow Status [7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	0	0	0 0 0 0 0					
	a meins							

BIT NUMBER	Name	Түре	DESCRIPTION
7-0	Group Underflow Status	R/O	Group Underflow Status:
		4	This READ/WRITE bit-field indicates whether or not a FIFO underflow has occurred in group n 1+1 APS protection channel.
		(0)	0 -Indicates "NO" FIFO underflow
		.6	1- Indicates a FIFO underflow
	The data	id nay	not

Table 53: APS Interrupt Register (Address Location= 0x0198)

Віт 7	Віт 6	Віт 5	Bit 5 Bit 4 Bit 3 Bit 2		Віт 1	Віт 0	
		Transmit APS Parity Error Interrupt Status	Receive APS Parity Error Interrupt Status				
R/O	R/O	R/O R/O R/O R/O				RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7-2	Unused	R/O	
1	Transmit APS Parity Error Interrupt Status	RUR	Transmit APS Parity Error Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the transmit APS module has declared a "Transmit APS Parity Error" Interrupt since the last read of this register. 0 – The "Transmit APS Parity Error" Interrupt has not occurred since the last read of this register. 1 - The "Transmit APS Parity Error" Interrupt has occurred since the last read of this register.
7-0	Receive APS Parity Error Interrupt Status	RUR	Receive APS Parity Error Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the receive APS module has declared a "Receive APS Parity Error" Interrupt since the last read of this register. O The "Receive APS Parity Error" Interrupt has not occurred since the last read of this register. 1 - The "Receive APS Parity Error" Interrupt has occurred since the last read of this register
	The product	a not y	

EXAR

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 54: APS Interrupt Register (Address Location= 0x019A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		(Group Overflow	Interrupt Status	3		
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7-0	Group Overflow Interrupt Status	RUR	Group Overflow Interrupt Status: This RESET-upon-READ bit-field indicates whether or not group n (0-7) APS protection channel has declared a "FIFO overflow" Interrupt since the last read of this register. 0 – The "FIFO overflow" interrupt has not occurred since the last read of this register.
			1 - The "FIFO overflow" Interrupt has occurred since the last read of this register.

Table 55: APS Interrupt Register (Address Location= 0x019B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		G	Froup Underflow	/ Interrupt Status	31		
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0.0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-0	Group Underflow Interrupt Status	RUR	Group Underflow Interrupt Status: This RESET-upon-READ bit-field indicates whether or not group n (0-7) APS protection channel has declared a "FIFO underflow" Interrupt since the last read of this register. 0 – The "FIFO underflow" Interrupt has not occurred since the last read of this register. 1 - The "FIFO underflow" Interrupt has occurred since the last read of this register.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 56: APS Interrupt Enable Register (Address Location= 0x019C)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Unu	ised			Transmit APS Parity Error Interrupt Enable	Receive APS Parity Error Interrupt Enable
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7-2	Unused	R/O	
1	Transmit APS Parity Error Interrupt Enable	R/W	Transmit APS Parity Error Interrupt Enable: This READ/WRITE bit-field permits the user to enable or disable the "Transmit APS Parity Error" Interrupt in Transmit APS module 0 – Disables the "Transmit APS Parity Error" Interrupt 1 – Enables the "Transmit APS Parity Error" Interrupt
7-0	Receive APS Parity Error Interrupt Enable	R/W	Receive APS Parity Error Interrupt Enable: This READ/WRITE bit-field permits the user to enable or disable the "Receive APS Parity Error" Interrupt in Receive APS module 0 – Disables the "Receive APS Parity Error" Interrupt 1 – Enables the "Receive APS Parity Error" Interrupt

Table 57: APS Interrupt Enable Register (Address Location= 0x019E)

		4	<u> </u>				
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		G	roup Overflow	Interrupt Enable	e		
R/W	R/W	RW	R/W	R/W	R/W	R/W	R/W
0	0	000	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7-0	Group Overflow	R/W	Group Overflow Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to enable or disable the "FIFO overflow" interrupt in group n APS protection channel.
			0 – Disables "FIFO overflow" interrupt .
			1 – Enables "FIFO overflow" Interrupt

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 58: APS Interrupt Enable Register (Address Location= 0x019F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Group Underflow Interrupt Enable								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7-0	Group Underflow	R/W	Group Underflow Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to enable or disable the "FIFO underflow" interrupt in group n APS protection channel.
			0 – Disables "FIFO underflow" interrupt .
			1 – Enables "FIFO underflow" Interrupt
	Theory	aduct of and man	1 - Enables "FIFO underflow" Interrupt 2 - Enables "FIFO underflow" Interrupt 2 - Enables "FIFO underflow" Interrupt 3 - Enables "FIFO underflow" Interrupt 4 - Enables "FIFO underflow" Interrupt 5 - Enables "FIFO underflow" Interrupt 6 - Enables "FIFO underflow" Interrupt 7 - Enables "FIFO underflow" Interrupt 8 - Enables "FIFO underflow" Interrupt 9 - Enables "FIFO underflow" Interrupt 1 - Enables "FIFO underflow" Interrupt 1 - En



1.3 LINE INTERFACE CONTROL BLOCK

1.3.1 LINE INTERFACE CONTROL REGISTER

Table 59: Line Interface Control Register - Address Map

0x02 0x0302 Receive Line Interface Control Register – Byte 1 0x00 0x03 0x0303 Receive Line Interface Control Register – Byte 0 0x00 0x04 – 0x06 0x0304 – 0x0306 Reserved 0x00 0x07 0x0307 Receive Line Status Register 0x00 0x08 – 0x0A 0x0308 – 0x030A Reserved 0x00 0x0B 0x030B Receive Line Interrupt Register 0x00 0x0C – 0x0E 0x030C – 0x030E Reserved 0x00 0x0F 0x030F Receive Line Interrupt Enable Register 0x00 0x10 – 0x82 0x0310 – 0x0382 Reserved 0x00 0x83 0x0383 Transmit Line Interface Control Register 0x00	INDIVIDUAL REGISTER ADDRESS	Address Location	REGISTER NAME	DEFAULT VALUES
0x04 - 0x06 0x0304 - 0x0306 Reserved 0x00 0x07 0x0307 Receive Line Status Register 0x00 0x08 - 0x0A 0x0308 - 0x030A Reserved 0x00 0x0B 0x030B Receive Line Interrupt Register 0x00 0x0C - 0x0E 0x030C - 0x030E Reserved 0x00 0x0F 0x030F Receive Line Interrupt Enable Register 0x00	0x02	0x0302	Receive Line Interface Control Register – Byte 1	0x00
0x07 0x0307 Receive Line Status Register 0x00 0x08 -0x0A 0x0308 -0x030A Reserved 0x00 0x0B 0x030B Receive Line Interrupt Register 0x00 0x0C - 0x0E 0x030C - 0x030E Reserved 0x00 0x0F 0x030F Receive Line Interrupt Enable Register 0x00	0x03	0x0303	Receive Line Interface Control Register – Byte 0	0x00
0x08 -0x0A 0x0308 -0x030A Reserved 0x00 0x0B 0x030B Receive Line Interrupt Register 0x00 0x0C - 0x0E 0x030C - 0x030E Reserved 0x00 0x0F 0x030F Receive Line Interrupt Enable Register 0x00	0x04 - 0x06	0x0304 - 0x0306	Reserved	0x00
0x0B 0x030B Receive Line Interrupt Register 0x00 0x0C - 0x0E 0x030C - 0x030E Reserved 0x00 0x0F 0x030F Receive Line Interrupt Enable Register 0x00	0x07	0x0307	Receive Line Status Register	0x00
0x0C - 0x0E 0x030C - 0x030E Reserved 0x00 0x0F 0x030F Receive Line Interrupt Enable Register 0x00	0x08 -0x0A	0x0308 -0x030A	Reserved	0x00
0x0F 0x030F Receive Line Interrupt Enable Register 0x00	0x0B	0x030B	Receive Line Interrupt Register	0x00
	0x0C - 0x0E	0x030C - 0x030E	Reserved	0x00
0x10 - 0x82 0x0310 - 0x0382 Reserved 0x00 0x83 0x0383 Transmit Line Interface Control Register 0x00	0x0F	0x030F	Receive Line Interrupt Enable Register	0x00
0x83 0x0383 Transmit Line Interface Control Register 0x00	0x10 - 0x82	0x0310 - 0x0382	Reserved	0x00
The product or products in be ordered (OBS)	0x83	0x0383	Transmit Line Interface Control Register	0x00
		The product	or productive design of the production of the pr	



Rev 2.0.0

1.3.2 LINE INTERFACE CONTROL REGISTER DESCRIPTION

Table 60: Receive Line Interface Control Register – Byte 1 (Address Location= 0x0302)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Loop-timing Mode	Split Loop Back	Unused	Remote Serial Loop Back	Unused	Analog Local Loop Back Enable	Digital Local Loop Back Enable
R/W	R/W	R/W	R/O	R/W	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Unused	R/O	is ad
6	Loop Timing Mode	R/W	Loop-Timing Mode:
			This READ/WRITE bit-field permits the user to configure the 94L33 to operate in the Loop-timing Mode. If the user implements this configuration, then the Transmit Line Interface Block will use the Recovered Clock as its timing source.
			0 - Configures the Transmit Line Interface Block to use "Local-Timing" Mode (e.g., the timing source is from the Clock Synthesizer block).
			1 - Configures the Transmit Line Interface Block to operate in the "Loop-Timing" Mode.
5	Split Loop Back	R/W	Split Loop-back Enable
			This READ/WRITE bit-field permits the user to configure the 94L33 to operate in the "Split Loop-back" Mode. If the user implements this configuration, then two types of loop-backs will exist within the chip simultaneously. a A Local Loop-back
	the	roduc	This toop-back path will originate from the Transmit STS-3 TOH Processor block. It will be routed through a portion of the "Transceiver circuitry" (through the "Transmit Parallel-to-Serial Converter" block) and then back to the "Receive Serial-to-Parallel Converter" block, before being routed to the Receive STS-3 TOH Processor block.
	The	KO.	b. A Remote Loop-back
	` 8	and	This loop-back path will originate from the Receive STS-3/STM-1 PECL Interface input. It will be routed through the CDR (Clock & Data Recovery) block; before being routed to the Transmit STS-3/STM-1 PECL Interface output.
			0 - Configures the 94L33 to disable split loop back
			1 – Configures the 94L33 to enable split loop back
4	Unused	R/W	
3	Remote Serial		Remote Serial Loop-back Enable:
	Loop Back		This READ/WRITE bit-field permits the user to configure the 94L33 to operate in the "Remote Serial Loop-back" Mode. In this mode, the incoming (Received Data) will enter the device via the Receive STS-3/STM-1 PECL Interface Input. This signal will then be processed via the CDR (Clock and Data Recovery) Block. At this point, this input signal will proceed via two paths in parallel. In one path, the signal will proceed onto the "Receive Serial-to-Parallel" Converter and then the Receive STS-3

		TOH Processor block (and so on). The other path will not proceed through the "Receive Serial-to Parallel" Converter block. Instead this signal will proceed on towards the "Transmit STS-3/STM-1 PECL Interface Output, thereby completing the loop-back path.				
		0 – Configures the 94L33 to NOT operate in the Remote Serial Loop-back Mode.				
		1 - Configures the 94L33 to operate in the Remote Serial Loop-back Mode.				
Unused	R/O					
Analog Local Loop	R/W	Analog Local Loop Back:				
Back Enable		This READ/WRITE bit field permits the user to configure the 94L33 to operate in the "Analog Local Loop Back" Mode. If the user implements this configuration, analog local loop back including data and clock recovery will be enabled. 0 – Analog local loop back is enabled. 1 – Analog local loop back is enabled.				
Digital Local Local	DAM	↑ √				
Back Enable		Digital Local Loop Back This READ/WRITE bit field permits the user to configure the 94L33 to operate in the "Digital Local Loop Back" Mode. If the user implements this configuration, digital local loop back NOT including data and clock recovery will be enabled.				
		1 – Digital local loop back is disabled				
	Analog Local Loop Back Enable Digital Local Loop Back Enable	Analog Local Loop Back Enable Digital Local Loop Back Enable R/W				

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 61: Receive Line Interface Control Register – Byte 0 Address Location= 0x0303)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Receive Line Interface Module Power Down	Redundant Receive Line Interface Module Power Down	Force Training Mode Upon LOS			Unused		
R/W	R/W	R/W	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7	Receive Line	R/W	Receive Line Interface Module Power Down
	Interface Module Power Down		This READ/WRITE bit field permits the user to power down receive line interface module
			0 – Turn on receive line interface module
			1 – Power down receive line interface module
6	Redundant Receive Line	R/W	Redudant Receive Line Interface Module Power Down:
	Interface Module Power Down		This READ/WRITE bit field permits the user to power down redundant receive line interface module
			0 - Turn on redundant receive line interface module
			1 – Power down redundant receive line interface module
5	Force Training	R/W	Force Training Mode Upon LOS:
	Mode Upon LOS		This READ/WRITE bit field permits the receive line interface phase lock loop to stay in training mode as long as the external LOS is asserted.
			0 Receive Line Interface PLL will NOT stay in training mode
		, c	1 - Receive Line Interface PLL will stay in training mode
4-0	Unused	R/O	e o
	Unused	atand	May

Table 62: Receive Line Interface Status Register (Address Location= 0x0307)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused			Clock Lock Status	Loss of Signal Status	Redundant Receiver Clock Lock Status	Redundant Receiver Loss of Signal Status
R/W	R/O	R/O	R/O	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7-4	Unused	R/O	
3	Clock Lock Status	RUR	Clock Lock Status: This RESET-upon-READ bit field indicates whether or not the clock lock status is detected by transceiver 0 – Indicates clock lock is NOT detected by transceiver 1 – Indicates clock lock is detected by transceiver
2	Loss of Signal Status	RUR	Loss of Signal Status: This RESET-upon-READ bit field indicates whether or not the loss of signal status is detected by transceiver 0 – Indicates loss of signal is NOT detected by transceiver 1 – Indicates loss of signal is detected by transceiver
1	Redundant Receiver Clock Lock Status	RUR	Redundant Receiver Clock Lock Status: This RESET-upon-READ bit field indicates whether or not the clock lock status is detected by redundant receiver 0 —Indicates clock lock is NOT detected by redundant receiver Indicates clock lock is detected by redundant receiver
0	Redundant Receiver Loss of Signal Status	RUR	Redundant Receiver Loss of Signal Status: This RESET-upon-READ bit field indicates whether or not the loss of signal status is detected by redundant receiver 0 – Indicates loss of signal is NOT detected by redundant receiver 1 – Indicates loss of signal is detected by redundant receiver

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 63: Receive Line Interface Interrupt Register (Address Location= 0x030B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused				Clock Lock Interrupt	Loss of Signal Interrupt	Redundant Receiver Clock Lock Interrupt	Redundant Receiver Loss of Signal Interrupt
R/W	R/O	R/O	R/O	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7-4	Unused	R/O	
3	Clock Lock Interrupt	RUR	Clock Lock Interrupt: This RESET-upon-READ bit field indicates whether or not a clock lock interrupt has occurred. A clock lock interrupt occurs when the signal "Clock Lock Status" (address location, 0x0307) makes a "0" to "1" or "1" to "0" transition. 0 – Indicates clock lock interrupt is NOT declared. 1 – Indicates clock lock is declared
2	Loss of Signal Interrupt	RUR	Loss of Signal Interrupt: This RESET-upon-READ bit field indicates whether or not a loss of signal interrupt has occurred. A clock lock interrupt occurs when the signal "Loss of Signal Status" (Address Location: 0x0307) makes a "0" to "1" or "1" to "0" transition. 0 – Indicates a loss of signal interrupt is NOT declared. 1 – Indicates a loss of signal is declared
1	Redundant Receiver Clock Lock Interrupt	RUR	Redundant Receiver Clock Lock Interrupt: This RESET-upon-READ bit field indicates whether or not a clock lock interrupt has occurred in the redundant receiver block. A clock lock interrupt occurs when the signal "Clock Lock Status" (address location: 0x0307) makes a "0" to "1" or "1" to "0" transition. 0 Indicates clock lock interrupt is NOT declared. 1 – Indicates clock lock is declared
0	Redundant Receiver Loss of Signal Interrupt	RUR	Redundant Receiver Loss of Signal Interrupt: This RESET-upon-READ bit field indicates whether or not a loss of signal interrupt has occurred in the redundant receiver block. A clock lock interrupt occurs when the signal "Loss of Signal Status" (Address Location: 0x0307) makes a "0" to "1" or "1" to "0" transition. 0 – Indicates a loss of signal interrupt is NOT declared. 1 – Indicates a loss of signal is declared

Table 64: Receive Line Interface Interrupt Register (Address Location= 0x030F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused				Loss of Signal Interrupt Enable	Redundant Receiver Clock Lock Interrupt Enable	Redundant Receiver Loss of Signal Interrupt Enable
R/W	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7-4	Unused	R/O	is ad
3	Clock Lock Interrupt Enable	R/W	Clock Lock Interrupt Enable: This READ/WRITE bit field disables or enables the clock lock interrupt. 0 – Disables clock lock interrupt 1 – Enables clock lock interrupt
2	Loss of Signal Interrupt	R/W	Loss of Signal Interrupt Enable: This READ/WRITE bit field disables or enables the loss of signal interrupt. 0 – Disables loss of signal interrupt 1 – Enables loss of signal interrupt
1	Redundant Receiver Clock Lock Interrupt Enable	R/W	Redundant Receiver Clock Lock Interrupt Enable: This READ/WRITE bit field disables or enables the clock lock interrupt for the redundant receiver block. 0 – Disables clock lock interrupt 1 – Enables clock lock interrupt
0	Redundant Receiver Loss of Signal Interrupt	R/W	Redundant Receiver Loss of Signal Interrupt Enable: This READ/WRITE bit field disables or enables the loss of signal interrupt for the redundant receiver block. 0 – Disables loss of signal interrupt 1 – Enables loss of signal interrupt

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 65: Transmit Line Interface Control Register (Address Location= 0x0383)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit Line Interface Module Power Down	Transmit Clock Enable	Clock Synthesizer	Redundant Enable	Unused	Unused	Reference (Clock Divide
R/W	R/W	R/W	R/W	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Transmit Line	R/W	Transmit Line Interface Module Power Down:
	Interface Module Power Down		This READ/WRITE bit field permits the user to enable or disable both transmitter data and clock outputs in the transmit line interface module.
			0 - Disables both transmitter data and clock outputs in transmit line interface
			1 - Enables both transmitter data and clock outputs in transmit line interface
6	Transmit Clock	R/W	Transmit Clock Enable:
	Enable		This READ/WRITE bit field permits the user to enable or disable the transmitter clock output.
			0 – Disables transmitter clock output
			1 – Enables transmitter clock output
5	Clock	R/W	Clock Synthesizer:
	Synthesizer		This READ/WRITE bit field permits the user to determine the source of transmit SONET clock.
		Ċ	0 -Uses reference clock as SONET transmit clock
		gu	Uses 19MHz generated by clock synthesizer as SONET transmit clock
4	Redundant	R/W	Redundant Enable:
	Enable	10	This READ/WRITE bit field permits the user to enable or disable the redundant transmit output pads
	, 9	,40	0 – Disables redundant transmit output
		3.	1 – Enables redundant transmit output
3	Unused	R/W	Serial Loopback:
			This READ/WRITE bit field permits the user to enable or disable serial loopback.
			0 – Disables Serial loopback
			1 – Enables Serial loopback
2	Unused	R/O	
1-0	Reference Clock	R/W	Reference Clock Divide:
	Divide		This READ/WRITE bit field permits the user to select the desired reference clock speed as follows:
			00 = 19.44 MHz
	l .	l .	

	01 = 38.88 MHz
	10 = 51.85 MHz
	11 = 77.76 MHz

The product are no products man to be ordered (OBS)



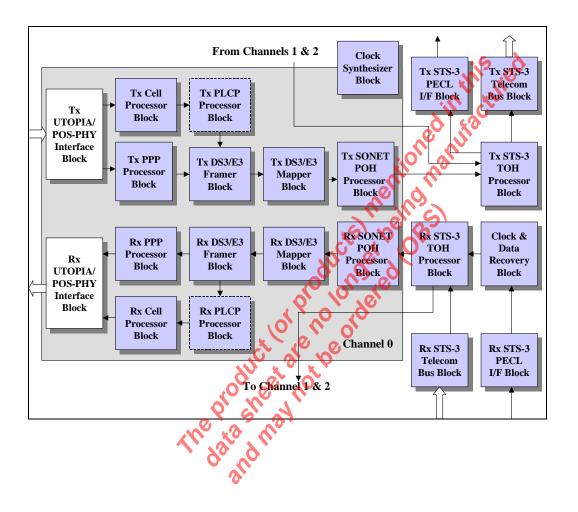
Rev 2.0.0

1.4 RECEIVE/TRANSMIT UTOPIA INTERFACE BLOCK

The register map for the Receive/Transmit Utopia Interface Block is presented in the Table below. Additionally, a detailed description of each of the "Receive/Transmit UTOPIA Interface" Block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33, with the "Receive and Transmit UTOPIA Interface Blocks "highlighted" is presented below in Figure 6

Figure 5: Illustration of the Functional Block Diagram of the XRT94L33, with the Receive/Transmit UTOPIA Interface Blocks "High-lighted".



1.4.1 RECEIVE/TRANSMIT UTOPIA INTERFACE BLOCK REGISTER

Table 66: Receive/Transmit UTOPIA Interface Block Register - Address Map

	RECEIVE/TRANSMIT UTOPIA INTERFACE REGISTERS					
0x0384 - 0x0502	Reserved	0x00				
0x0503	Receive UTOPIA Control Register – Byte 0	0x8F				
0x0504 - 0x0512	Reserved	0x00				
0x0513	Receive UTOPIA Port Address	0x00				
0x0514 - 0x0516	Reserved	0x00				
0x0517	Receive UTOPIA Port Number	0x00				
0x0518 - 0x0582	Reserved	0x00				
0x0583	Transmit UTOPIA Control Register – Byte 0	0x8F				
0x0584 - 0x0592	Reserved	0x00				
0x0593	Transmit UTOPIA Port Address 0x00					
0x0594 - 0x0596	Reserved 0x00					
0x0597	Transmit UTOPIA Port Number 0x00					
0x0598 - 0x1102	Reserved 0x00					
	Reserved Reserved Reserved Reserved					



1.4.2 RECEIVE UTOPIA INTERFACE BLOCK REGISTER DESCRIPTION

Table 67: Receive UTOPIA/POS-PHY Control Register – Byte 0 (Address = 0x0503)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
UTOPIA Level Select	Multi-PHY Polling Enable	Back to Back Polling Enable	Direct Status Indication Enable	UTOPIA/POS-PHY Data Bus Width		Cell Si	ze[1:0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	0	0	1	1	1	1

BIT NUMBER	NAME	Түре	DESCRIPTION
7	UTOPIA Level Select	R/W	UTOPIA Level Select:
			This READ/WRITE bit-field permits the user to select either UTOPIA level 3, UTOPIA level 2, or UTOPIA level 1 standard to be used. If the user selects UTOPIA level 3 to be used, the UTOPIA interface will support cell-level handshakes compliant to the UTOPIA level 3 standard. If the user selects UTOPIA level 2 or 1, then the UTOPIA interface will support cell-level handshakes compliant to both UTOPIA level 2 and 1 standards. 0 Configures the Receive UTOPIA interface block to use UTOPIA Level 1 or 2 standards
		,00	1 - Configures the Receive UTOPIA interface block to use UTOPIA Level 3 standard.
6	Multi-PHY Polling Enable	R/W	Multi-PHY Polling Enable:
	Multi-PHY Polling Enable	are to	This READ/WRITE bit-field permits the user to either enable or disable Multi-PHY Polling for the Receive UTOPIA Interface block. If the user implements this feature (and configures the XRT94L33 to operate in the Multi-PHY Mode) then the RxUClav output pin will be driven (either "high" or "low") based upon the fill-status of the Receive FIFO within the Channel that corresponds to the "Receive UTOPIA Address" that is currently being applied to the "RxUAddr[4:0]" input pins. If the user does not implement this feature (and then configures the XRT94L33 to operate in the Single-PHY Mode),
	⊘ *		then the "RxUClav" output pin will unconditionally reflect the "Receive FIFO fill-status" for Channel 0. No attention will be paid to the address values placed upon the "RxUAddr[4:0]" input pins.
			0 – Configures the Receive UTOPIA Interface block to operate in the Single-PHY Mode.
			1 – Configures the Receive UTOPIA Interface block to operate in the Multi-PHY Mode.
5	Back-to-Back Polling Enable	R/W	Back-to-Back Polling Enable:
			This READ/WRITE bit-field permits the user to configure the Receive UTOPIA Interface block to support "Back-to-Back Polling".
			Ordinarily, for Multi-PHY polling, the user is required to interleave all UTOPIA Address values (that are to be placed

			0x1F). However, in Interface block to differ the user also endoes not need to NULL Address. In "back-to-back" stree "RxUAddr[4:0]" input driving the RxUCl (depending upon the "Depending upon the "RxUAddr[4:0]" in the "Rx	if the interpretation of the interlement of this arm of the interpretation of the interp	put pins) with the NULL A user configures the Rece e in the "UTOPIA Level 3 "Back-to-Back Polling", rave the UTOPIA Addressic case, the user can sin "relevant" UTOPIA Address, and the XRT94L33 will utput pins to the approprietive FIFO fill-status). The addresses (that are the total pins) with the NULL Addresses (Polling. In this more all UTOPIA Addresses (Addresses Addresses (Addresses addresses (Polling) input pins) with the NULL Addresses (Polling).	" Mode, and then he/she ses with the apply apply a esses to the respond by priate states de, the user to be applied ldress. de, the user to be the applied ldress. de, the user to the user to be the user to be applied ldress.
			block to the user 1.Configure the Re "UTOPIA Level 3" (UTOPIA Level 3 D 2.Configure the Re	operat must a eceive Mode. Disable eceive	figure the Receive UTOF te in the "Back-to-Back Po also do the following. This is accomplished by e) within this Register to "C UTOPIA Interface to su complished by setting Bit	polling" Mode, perate in the setting Bit 7 ". "pport "Multi-
4	Direct Status Indication	R/W	Polling Enable) with			`
	Enable	All .	96,46			
3 - 2	Enable UTOPIA/POS-PHY Data Bus Width[1:0]	BW (These READ/WRI width of the Receiv relationship betwee corresponding widt Data Bus is tabulat	TE bit re UTC en the ths of	t-fields permit the user to DPIA and POS-PHY Data contents of these bit-fie the Receive UTOPIA and	Buses. The elds and the
	arodreet, n	0,	UTOPIA/POS-PH Data Bus Width[Corresponding UTOP PHY Data Bus Width	A/POS-
	10 1 25 103	00			Not Valid	
	M. Astradio		01		8 bits	
	all		10		16 bits	
			11		Not Valid	
1 – 0	Cell Size[1:0]		Cell Size[1:0]:		•	
			the size of the AT UTOPIA Interface	M cell block bit-fiel	E bit-fields permit the uson that will be handled by the relationship to the corresponding the corresp	the Receive etween the
			Cell Size[1:0]	Resi	ulting Cell Size (Bytes)	

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

01	53 bytes (Only valid for UTOPIA Level 1, and if the UTOPIA Data Bus Width is set to 8 bits)
10	54 bytes (Only valid for UTOPIA Levels 1 and 2)
11	56 bytes
the U7	r must bear in mind the UTOPIA Level and FOPIA Data Bus width selected, when g the Cell Size.

The product are no ordered (OES)

Table 68: Receive UTOPIA Port Address Register (Address = 0x0513)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused			Receive l	JTOPIA Port Add	dress [4:0]	
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 5	Unused	R/O	
4 - 0	Receive UTOPIA Port	R/W	Receive UTOPIA Port Address[4:0]:
	Address [4:0]		These READ/WRITE register bits, along with the "Receive UTOPIA Port Number [4:0]" bits (within the "Receive UTOPIA Port Number" Register (Address = 0x0517) permit the user to assign a unique Receive UTOPIA address to each of the three STS-1 channels within the XRT94L33.
			For UTOPIA Level 2/3 applications, the user can write in any value, ranging from 0x00 through 0x1E into this register.
			The Receive UTOPIA Address Assignment Procedure:
			In order to assign a UTOPIA Address to a given Channel (or Port) within the XRT94L33, the user must do the following.
			a. Write the value corresponding to a given XRT94L33 Channel into the "Receive UTOPIA Port Number" Register (Address = 0x0517).
		40	b) Write the corresponding UTOPIA Address value into this register.
	ta ta	61,61	Once this "two-step" procedure has been executed, then the XRT94L33 Channel (as specified during step "a") will be assigned the "Receive UTOPIA Address" value (as specified during step "b").
	The product	et a not	, o c

EXARExperience *Qur* Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 69: Receive UTOPIA Port Number Register (Address = 0x0517)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Unused			Receive UTOPIA Port Number[4:0]					
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 5	Unused	R/O	
			Receive UTOPIA Port Number[4:0]: These READ/WRITE register bits, along with the "Receive UTOPIA Port Address[4:0]" bits (within the "Receive UTOPIA Port Address" Register (Address = 0x0513) permit the user to assign a unique Receive UTOPIA address to each of the three STS-1 channels within the XRT94L33. In the XRT94L33, the following are the only valid values that can be written into these register bits, during the "Receive UTOPIA Address Assignment" process. 0x00 - XRT94L33 Channel 0 0x01 - XRT94L33 Channel 1 0x02 - XRT94L33 Channel 2 The Receive UTOPIA Address Assignment Procedure: In order to assign a UTOPIA Address to a given Channel (or Port) within the XRT94L33, the user must do the following. a. Write the value corresponding to a given XRT94L33 Channel into this register. b. Write the corresponding UTOPIA Address value into the "Receive UTOPIA Port Address" Register (Address =
	prod	heet a	0x0513). Once this "two-step" procedure has been executed, then the XRT94L33 Channel (as specified during step "a") will be assigned the "Receive UTOPIA Address" value (as specified during step "b").

1.4.3

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 70: Transmit UTOPIA/POS-PHY Control Register – Byte 0 (Address = 0x0583)

TRANSMIT UTOPIA INTERFACE BLOCK REGISTER DESCIPTION

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
UTOPIA Level 3 Disable	Multi-PHY Polling Enable	Back to Back Polling Enable	Direct Status Indication Enable	UTOPIA/POS-PHY Data Bus Width		Cell Si	ze[1:0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	0	0	1	1	1	1

BIT NUMBER	Name	Түре	DESCRIPTION
7	UTOPIA Level 3 Disable	R/W	The state of the s
6	Multi-PHY Polling Enable	R/W	Multi-PHY Polling Enable:
			This READ/WRITE bit-field permits the user to either enable or disable Multi-PHY Polling for the Transmit UTOPIA Interface block. If the user implements this feature (and configures the XRT94L33 to operate in the Multi-PHY Mode) then the TxUClav output pin will be driven (either "high" or "low") based upon the fill-status of the Transmit FIFO within the Channel that corresponds to the "Transmit UTOPIA Address" that is currently being applied to the "TxUAddr[4:0]" input pins. If the user does not implement this feature (and then configures
		Proof	the XRT94L33 to operate in the Single-PHY Mode), then the "TxUClav" output pin will unconditionally reflect the "Transmit FIFO fill-status" for Channel 0. No attention will be paid to the address values placed upon the "TxUAddr[4:0]" input pins.
		(e) e	O – Configures the Transmit UTOPIA Interface block to operate in the Single-PHY Mode.
	oduleta	oto	1 – Configures the Transmit UTOPIA Interface block to operate in the Multi-PHY Mode.
5	Back-to-Back Polling	R/W	Back-to-Back Polling Enable:
	Enable His		This READ/WRITE bit-field permits the user to configure the Transmit UTOPIA Interface block to support "Back-to-Back Polling".
	**		Ordinarily, for Multi-PHY polling, the user is required to interleave all UTOPIA Address values (that are to be placed on the "TxUAddr[4:0]" input pins) with the NULL Address (e.g., 0x1F). However, if the user configures the Transmit UTOPIA Interface block to operate in the "UTOPIA Level 3" Mode, and if the user also enables "Back-to-Back Polling", then he/she does not need interleave the UTOPIA Addresses with the NULL Address. In this case, the user can simply apply a "back-to-back" stream of "relevant" UTOPIA Addresses to the "TxUAddr[4:0]" input pins, and the XRT94L33 will respond by driving the TxUClav output pins to the appropriate states (depending upon the Transmit FIFO fill-status).
			0 – Disables "Back-to-Back" Polling. In this mode, the user must interleave all UTOPIA Addresses (that are to be applied to the "TxUAddr[4:0]" input pins) with the NULL Address.
			1 - Enables "Back-to-Back" Polling. In this mode, the user does

EXARExperience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

					all UTOPIA Addresses (t 4:0]" input pins) with the N	
			block to	opera	nfigure the Transmit UTC te in the "Back-to-Back I also do the following.	
			"UTOPIA Level 3"	Mode.	nit UTOPIA Interface to o This is accomplished b within this Register to "0"	y setting Bit 7
				is is ac	nit UTOPIA Interface to s ecomplished by setting Bi s register to "1".	
4	Direct Status Indication Enable	R/W				
3 - 2	UTOPIA/POS-PHY Data	R/W	UTOPIA/POS-PHY	Y Data	Bus Width[1:0]:	
	Bus Width[1:0]		of the Transmit relationship between	UTOPI een the Iths of	fields permit the user to so A and POS-PHY Data e contents of these bit-f the Transmit UTOPIA a ow.	Buses. The lields and the
			UTOPIA/POS-PI Data Bus Width		Corresponding UTO PHY Data Bus Width	PIA/POS-
			00		Not Valid	
			01.5	6	8 bits	
			180 61		16 bits	
		30	1111910		Not Valid	
1 – 0	Cell Size[1:0]	OTO	Cell Size[1:0]: These two READ/size of the ATM centerface blocks. The bit-fields and the centerface.	ell that v The rela	is bit-fields permit the user will be handled by the Tra ationship between the cor onding Cell Sizes are tabu	nsmit UTOPIA ntents of these
	210 10	, 100	Cell Size[1:0]	Resu	ulting Cell Size (Bytes)	
		37	00	52 by	ytes	
	Thedatandr		01	UTO UTO	bytes (Only valid for PIA Level 1, and if the PIA Data Bus Width is 5 8 bits)	
			10		bytes (Only valid for PIA Levels 1 and 2)	
			11	56 by	ytes	
				Data	bear in mind the UTOPIA Bus width selected, wher	

Table 71: Transmit UTOPIA Port Address Register (Address = 0x0593)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Unused			Transmit UTOPIA Port Address[4:0]					
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 5	Unused	R/O	
4 - 0	Transmit UTOPIA	R/W	Transmit UTOPIA Port Address[4:0]:
	Port Address[4:0]		These READ/WRITE register bits, along with the "Transmit UTOPIA Port Number[4:0]" bits (within the "Transmit UTOPIA Port Number" Register (Address = 0x0597) permit the user to assign a unique Transmit UTOPIA address to each of the three STS-1 channels within the XRT94L33.
			For UTOPIA Level 2/3 applications, the user can write in any value, ranging from 0x00 through 0x1E into this register.
			The Transmit UTOPIA Address Assignment Procedure:
			In order to assign a UTOPIA Address to a given Channel (or Port) within the XRT94L33, the user must do the following.
			a. Write the value corresponding to a given XRT94L33 Channel into the "Transmit UTOPIA Port Number" Register (Address = 0x0597).
		40	b. Write the corresponding UTOPIA Address value into this register.
	N. Carlotte	(01,01	Once this "two-step" procedure has been executed, then the XRT94L33 Channel (as specified during step "a") will be assigned the "Transmit UTOPIA Address" value (as specified during step "b").
	The product	et all of	

EXAR Experience Our Connectivit

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 72: Transmit UTOPIA Port Number Register (Address = 0x0597)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Unused			Transmit UTOPIA Port Number[4:0]					
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

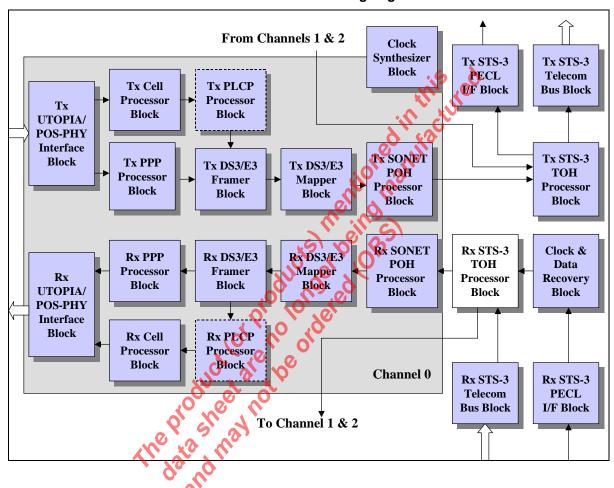
BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 5	Unused	R/O	
	ransmit UTOPIA Port Number[4:0]	R/W	Transmit UTOPIA Port Number[4:0]: These READ/WRITE register bits, along with the "Transmit UTOPIA Port Address[4:0]" bits (within the "Transmit UTOPIA Port Address" Register (Address = 0x0593), permit the user to assign a unique Transmit UTOPIA address to each of the three STS-1 channels within the XRT94L33. In the XRT94L33, the following are the only valid values that can be written into these register bits, during the "Transmit UTOPIA Address Assignment" process. 0x00 – XRT94L33 Channel 0 0x01 – XRT94L33 Channel 1 0x02 – XRT94L33 Channel 2 The Transmit UTOPIA Address Assignment Procedure: In order to assign a UTOPIA Address to a given Channel (or Port) within the XRT94L33, the user must do the following. a. Write the value corresponding to a given XRT94L33 Channel into this register. b. Write the corresponding UTOPIA Address value into the "Transmit UTOPIA Port Address" Register (Address = 0x0593). Once this "two-step" procedure has been executed, then the XRT94L33 Channel (as specified during step "a") will be assigned the "Transmit UTOPIA Address" value (as specified during step "b").

1.5 RECEIVE STS-3 TOH PROCESSOR BLOCK

The register map for the Receive STS-3 TOH Processor Block is presented in the Table below. Additionally, a detailed description of each of the "Receive STS-3 TOH Processor" Block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33, with the "Receive STS-3 TOH Processor Block "highlighted" is presented below in Figure 6

Figure 6: Illustration of the Functional Block Diagram of the XRT94L33, with the Receive STS-3 TOH Processor Block "High-lighted".





1.5.1 RECEIVE STS-3 TOH PROCESSOR BLOCK REGISTER

Table 73: Receive STS-3 TOH Processor Block Control Register – Address Map

Individual Register Address	Address Location	REGISTER NAME	DEFAULT VALUES
0x00 - 0x02	0x1000 – 0x1102	Reserved	
0x03	0x1103	Receive STS-3 Transport Control Register – Byte 0	0x00
0x04 - 0x05	0x1104 – 0x1105	Reserved	0x00
0x06	0x1106	Receive STS-3 Transport Status Register – Byte 1	0x00
0x07	0x1107	Receive STS-3 Transport Status Register Byte	0x02
0x08	0x1108	Reserved	0x00
0x09	0x1109	Receive STS-3 Transport Interrupt Status Register – Byte 2	0x00
0x0A	0x110A	Receive STS-3 Transport Interrupt Status Register – Byte 1	0x00
0x0B	0x110B	Receive STS-3 Transport Interrupt Status Register – Byte 0	0x00
0x0C	0x110C	Reserved	0x00
0x0D	0x110D	Receive STS-3 Transport Interrupt Enable Register – Byte 2	0x00
0x0E	0x110E	Receive STS-3 Transport Interrupt Enable Register – Byte 1	0x00
0x0F	0x110F	Receive STS3 Transport Interrupt Enable Register – Byte 0	0x00
0x10	0x1110	Receive STS-3 Transport B1 Error Count – Byte 3	0x00
0x11	0x1111	Receive STS-3 Transport B1 Error Count – Byte 2	0x00
0x12	0x1112	Receive STS-3 Transport B1 Error Count – Byte 1	0x00
0x13	0x1113	Receive STS-3 Transport B1 Error Count – Byte 0	0x00
0x14	0x1114	Receive STS-3 Transport B2 Error Count – Byte 3	0x00
0x15	0x1/15	Receive STS-3 Transport B2 Error Count – Byte 2	0x00
0x16	0x1116	Receive STS-3 Transport B2 Error Count – Byte 1	0x00
0x17	0x1117	Receive STS-3 Transport B2 Error Count – Byte 0	0x00
0x18	0x1118	Receive STS-3 Transport REI-L Error Count – Byte 3	0x00
0x19	0x1119	Receive STS-3 Transport REI-L Error Count – Byte 2	0x00
0x1A	0x111A	Receive STS-3 Transport REI-L Error Count – Byte 1	0x00
0x1B	0x111B	Receive STS-3 Transport REI-L Error Count – Byte 0	0x00
0x1C	0x111C	Reserved	0x00
0x1D - 0x1E	0x111D - 0x111E	Reserved	0x00
0x1F	0x111F	Receive STS-3 Transport K1 Byte Value	0x00

INDIVIDUAL REGISTER ADDRESS	Address Location	REGISTER NAME	DEFAULT VALUES
0x20 - 0x22	0x1120 - 0x1122	Reserved	0x00
0x23	0x1123	Receive STS-3 Transport K2 Byte Value	0x00
0x24 - 0x26	0x1124 - 0x1126	Reserved	0x00
0x27	0x1127	Receive STS-3 Transport S1 Byte Value	0x00
0x28 - 0x2A	0x1128 – 0x112A	Reserved	0x00
0x2B	0x112B	Receive STS-3 Transport – In-Sync Threshold Value	0x00
0x2C, 0x2D	0x112C, 0x112D	Reserved	0x00
0x2E	0x112E	Receive STS-3 Transport – LOS Threshold Value – MSB	0xFF
0x2F	0x112F	Receive STS-3 Transport – LOS Threshold Value – LSB	0xFF
0x30	0x1130	Reserved	0x00
0x31	0x1131	Receive STS-3 Transport - SF Set Monitor Interval - Byte 2	0x00
0x32	0x1132	Receive STS-3 Transport – SF Set Monitor Interval – Byte 1	0x00
0x33	0x1133	Receive STS-3 Transport SF Set Monitor Interval – Byte 0	0x00
0x34, 0x35	0x1134 - 0x1135	Reserved	0x00
0x36	0x1136	Receive STS 3 Transport - SF Set Threshold - Byte 1	0x00
0x37	0x1137	Receive STS-3 Transport – SF Set Threshold – Byte 0	0x00
0x38, 0x39	0x1138, 0x1139	Reserved	0x00
0x3A	0x113A	Receive STS-3 Transport – SF Clear Threshold – Byte 1	0x00
0x3B	0x113B	Receive STS-3 Transport – SF Clear Threshold – Byte 0	0x00
0x3C	0x113C	Reserved	0x00
0x3D	0x113B	Receive STS-3 Transport – SD Set Monitor Interval – Byte 2	0x00
0x3E	0x113E	Receive STS-3 Transport – SD Set Monitor Interval – Byte 1	0x00
0x3F	0x113F	Receive STS-3 Transport – SD Set Monitor Interval – Byte 0	0x00
0x40, 0x41	0x1140, 0x1141	Reserved	0x00
0x42	0x1142	Receive STS-3 Transport – SD Set Threshold – Byte 1	0x00
0x43	0x1143	Receive STS-3 Transport – SD Set Threshold – Byte 0	0x00
0x44, 0x45	0x1144, 0x1145	Reserved	0x00
0x46	0x1146	Receive STS-3 Transport – SD Clear Threshold – Byte 1	0x00
0x47	0x1147	Receive STS-3 Transport – SD Clear Threshold – Byte 0	0x00
0x48 – 0x4A	0x1148 – 0x114A	Reserved	0x00
0x4B	0x114B	Receive STS-3 Transport – Force SEF Condition	0x00

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Individual Register Address	Address Location	REGISTER NAME	DEFAULT VALUES
0x4C, 0x4E	0x114C, 0x114E	Reserved	0x00
0x4F	0x114F	Receive STS-3 Transport – Receive J0 Trace Buffer Control	0x00
0x50, 0x51	0x1150, 0x1151	Reserved	0x00
0x52	0x1152	Receive STS-3 Transport – SD Burst Error Count Tolerance – Byte 1	0x00
0x53	0x1153	Receive STS-3 Transport – SD Burst Error Count Tolerance – Byte 0	0x00
0x54, 0x55	0x1154, 0x1155	Reserved	0x00
0x56	0x1156	Receive STS-3 Transport – SF Burst Error Count Tolerance – Byte 1	0x00
0x57	0x1157	Receive STS-3 Transport – SF Burst Error Count Tolerance – Byte 0	0x00
0x58	0x1158	Reserved	0x00
0x59	0x1159	Receive STS-3 Transport Receive SD Clear Monitor Interval – Byte 2	0xFF
0x5A	0x115A	Receive STS-3 Transport & Receive SD Clear Monitor Interval – Byte 1	0xFF
0x5B	0x115B	Receive STS-3 Transport - Receive SD Clear Monitor Interval - Byte 0	0xFF
0x5C	0x115C	Reserved	0x00
0x5D	0x115D	Receive ST\$ 3 Transport – Receive SF Clear Monitor Interval – Byte 2	0xFF
0x5E	0x115E	Receive STS-3 Transport – Receive SF Clear Monitor Interval – Byte 1	0xFF
0x5F	0x115F	Receive STS-3 Transport - Receive SF Clear Monitor - Byte 0	0xFF
0x60 - 0x62	0x1160 - 0x1162	Reserved	0x00
0x63	0x1163	Receive STS-3 Transport – Auto AIS Control Register	0x00
0x64 - 0x66	0x1164 - 0x1166	Reserved	0x00
0x67	0x1167	Receive STS-3 Transport – Serial Port Control Register	0x00
0x68 – 0x6A	0x1168 - 0x116A	Reserved	0x00
0x6B	0x116B	Receive STS-3 Transport – Auto AIS (in Downstream STS-1s) Control Register	0x000
0x6C - 0x79	0x116C - 0x1179	Reserved	
0x7A	0x117A	Receive STS-3 Transport – TOH Capture Indirect Address	0x00
0x7B	0x117B	Receive STS-3 Transport – TOH Capture Indirect Address	0x00
0x7C	0x117C	Receive STS-3 Transport – TOH Capture Indirect Data	0x00

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

INDIVIDUAL REGISTER ADDRESS	Address Location	REGISTER NAME	DEFAULT VALUES
0x7D	0x117D	Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x7E	0x117E	Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x7F	0x117F	Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x80 – 0xFF	0x1180 – 0x11FF	Reserved	0x00

The product or products mentioned in this are no ordered (OBS)



1.5.2 RECEIVE STS-3 TOH PROCESSOR BLOCK REGISTER DESCRIPTION

Table 74: Receive STS-3 Transport Control Register – Byte 0 (Address Location= 0x1103)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
STS-N OH Extract	SF Detect Enable	SD Detect Enable	Descramble Disable	SDH/ SONET*	REI-L Error Type	B2 Error Type	B1 Error Type
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	STS-N OH	R/W	STS-N Overhead Extract (Revision C Silicon Only):
	Extract		This READ/WRITE bit-field permits the user to configure the RxTOH output port to output the TOH for all lower tributary STS-1s within the incoming STS-3 signal.
			0 – Disables this feature. In this mode, the RxTOH output port will only output the TOH for the first STS-1 within the incoming STS-3 signal.
			1 – Enables this feature.
6	SF Detect	R/W	Signal Failure (SF) Detect Enable:
	Enable		This READ/WRITE bit-field permits the user to enable or disable SF Detection by the Receive STS-3 TOH Processor Block.
			0 – SF Detection is disabled.
			1 – SF Detection is enabled:
5	SD Detect	R/W	Signal Degrade (SD) Detect Enable:
	Enable		This READ/WRITE bit-field permits the user to enable or disable SD Detection by the Receive STS-3 TOH Processor Block.
			0 – SD Detection is disabled.
		111	1 – SD Detection is enabled.
4	Descramble	R/W	De-Scramble Disable:
	Disable	6, 2,	This READ/WRITE bit-field permits the user to either enable or disable descrambling by the Receive STS-3 TOH Processor block.
		300	0 – De-Scrambling is enabled.
		o Win	1 – De-Scrambling is disabled.
3	SDH/SONET*	R/W	SDH/SONET Select:
			This READ/WRITE bit-field permits the user to configure the Receiver to operate in either the SONET or SDH Mode.
			0 - Configures the Receiver to operate in the SONET Mode.
			1 – Configures the Receiver to operate in the SDH Mode.
2	REI-L Error	R/W	REI-L (Line – Remote Error Indicator) Error Type:
	Type		This READ/WRITE bit-field permits the user to specify how the "Receive Transport REI-L Error Count" register is incremented.
			0 – Configures the Receive STS-3 TOH Processor block to count REI-L Bit Errors.
			In this case the "Receive Transport REI-L Error Count" register will be

			incremented by the value of the lower nibble within the M0/M1 byte.
			1 – Configures the Receive STS-3 TOH Processor block to count REI-L Frame Errors.
			In this case the "Receive Transport REI-L Error Count" register will be incremented each time the STS-3 Receiver receives a "non-zero" M0/M1 byte.
1	B2 Error Type	R/W	B2 Error Type:
			This READ/WRITE bit-field permits the user to specify how the "Receive Transport B2 Error Count" register is incremented.
			$\rm 0$ – Configures the Receive STS-3 TOH Processor block to count B2 bit errors.
			In this case, the "Receive Transport B2 Error Count" register will be incremented by the number of bits, within the B2 value, that is in error.
			1 – Configures the Receive STS 3 TOH Processor block to count B2 frame errors.
			In this case, the "Receive Transport B2 Error Count" register will be incremented by the number of erred STS-3 frames.
0	B1 Error Type	R/W	B1 Error Type:
			This READ/WRITE bit-field permits the user to specify how the "Receive Transport B1 Error Count" register is incremented.
			0 - Configures the Receive STS-3 TOH Processor block to count B1 bit errors.
			In this case, the "Receive Transport B1 Error Count" register will be incremented by the number of bits, within the B1 value, that is in error.
			1 Configures the Receive STS-3 TOH Processor block to count B2 bit errors.
			In this case, the "Receive Transport B1 Error Count" register will be incremented by the number of erred STS-3 frames.
	The day	and ma	In the case, the "Receive Transport B1 Error Count" register will be incremented by the number of erred STS-3 frames.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 75: Receive STS-3 Transport Status Register – Byte 1 (Address Location= 0x1106)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused				J0 Message Mismatch Defect Declared	J0 Message Unstable Defect Declared	AIS_L Defect Declared	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 3	Unused	R/O	
2	J0 Message Mismatch Defect Declared	R/O	J0 – Section Trace Mismatch Indicator: This READ-ONLY bit-field indicates whether or not the Receive STS-3 TOH Processor block is currently declaring the Section Trace Mismatch condition. The Receive STS-3 TOH Processor block will declare a J0 (Section Trace) Mismatch condition, whenever it accepts a J0 Message that differs from the "Expected J0 Message". 0 – Section Trace Mismatch Condition is NOT declared. 1 – Section Trace Mismatch Condition is currently declared.
1	J0 Message Unstable Defect Declared	R/O	J0 – Section Trace Unstable Indicator: This READ-ONLY bit-field indicates whether or not the Receive STS-3 TOH Processor block is currently declaring the Section Trace Instability condition. The Receive STS-3 TOH Processor block will declare a J0 (Section Trace) Unstable condition, whenever the "J0 Unstable" counter reaches the value 8. The "J0 Unstable" counter will be incremented for each time that it receives a J0 message that differs from the "Expected J0 Message". The "J0 Unstable" counter is cleared to "0" whenever the Receive STS-3 TOH Processor block has received a given J0 Message 3 (or 5) consecutive times. Note: Receiving a given J0 Message 3 (or 5) consecutive times also sets this bit-field to "0". 0 — Section Trace Instability condition is NOT declared.
0	AIS_L Defect Declared	R/O	AIS-L (Line AIS) State: This READ-ONLY bit-field indicates whether or not the Receive STS-3 TOH Processor block is currently detecting an AIS-L (Line AIS) pattern in the incoming STS-3 data stream. AIS-L is declared if bits 6, 7 and 8 (e.g., the Least Significant Bits, within the K2 byte) value the value "1, 1, 1" for five consecutive STS-1 frames. 0 – AIS-L is NOT currently declared. 1 – AIS-L is currently being declared.

Table 76: Receive STS-3 Transport Status Register – Byte 0 (Address Location= 0x1107)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
RDI-L Defect Declared	S1 Byte Unstable Defect Declared	(K1, K2) APS Byte Unstable	SF Defect Declared	SD Defect Declared	LOF Defect Declared	SEF Defect Declared	LOS Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION					
7	RDI-L Defect	R/O	RDI-L (Line Remote Defect Indicator) Defect Declared:					
	Declared		This READ-ONLY bit-field indicates whether or not the Receive STS-3 TOH Processor block is currently declaring a Line-Remote Defect Indicator (RDI-L), in the incoming STS-3 signal. RDI-L is declared when bits 6, 7 and 8 (e.g., the three least significant bits) of the K2 byte contains the "1, 1, 0" pattern in 5 consecutive STS-3 frames.					
			0 – RDI-L is NOT being declared					
			1 – RDI-L is currently being declared.					
6	S1 Byte	R/O	S1 Byte Unstable Defect Declared Condition:					
	Unstable Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive STS-3 TOH Processor block is currently declaring the "S1 Byte Instability" condition. The Receive STS-3 TOH Processor block will declare an "S1 Byte Instability" condition whenever the "S1 Byte Unstable Counter" reaches the value 32. The "S1 Byte Unstable Counter" is incremented for each time that the Receive STS-3 TOH Processor block receives an S1 byte that differs from the previously received S1 byte. The "S1 Byte Unstable Counter" is cleared to "0" when the same S1 byte is received for 8 consecutive STS-3 frames.					
			Note: Receiving a given S1 byte, in 8 consecutive STS-3 frames also sets this bit-field to "0".					
			0 – S1 Instability Condition is NOT declared.					
		291	1 S1 Instability Condition is currently declared.					
5	(K1, K2)	R/O	APS (K1, K2 Byte) Unstable Condition:					
	APS Byte Unstable		This READ-ONLY bit-field indicates whether or not the Receive STS-3 TOH Processor block is currently declaring the "K1, K2 Byte Unstable" condition. The Receive STS-3 TOH Processor block will declare a "K1, K2 Byte Unstable" condition whenever the Receive STS-3 TOH Processor block fails to receive the same set of K1, K2 bytes, in 12 consecutive STS-3 frames. The "K1, K2 Byte Unstable" condition is cleared whenever the Receive STS-3 TOH Processor block receives a given set of K1, K2 byte values in three consecutive STS-3 frames.					
			0 – K1, K2 Unstable Condition is NOT currently declared.					
			1 – K1, K2 Unstable Condition is currently declared.					
4	SF Defect	R/O	SF (Signal Failure) Defect Declared:					
	Declared		This READ-ONLY bit-field indicates whether or not the Receive STS-3 TOH Processor block is currently declaring the SF defect. The SF defect is declared when the number of B2 errors observed over a given time interval exceeds a certain threshold.					
			0 – SF Defect is NOT being declared.					
			This bit is set to "0" when the number of B2 errors (accumulated over a given					

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			interval of time) does not exceed the "SF Declaration" threshold.
			1 – SF Defect is being declared.
			This bit is set to "1" when the number of B2 errors (accumulated over a given interval of time) does exceed the "SF Declaration" threshold.
3	SD Defect	R/O	SD (Signal Degrade) Defect Declared:
	Declared		This READ-ONLY bit-field indicates whether or not the Receive STS-3 TOH Processor block is currently declaring the SD defect. The SD defect is declared when the number of B2 errors observed over a given time interval exceeds a certain threshold.
			0 – SD Defect is NOT being declared.
			This bit is set to "0" when the number of B2 errors (accumulated over a given interval of time) does not exceed the "SD Declaration" threshold.
			1 – SD Defect is being declared.
			This bit is set to "1" when the number of B2 errors (accumulated over a given interval of time) does exceed the "SD Declaration" threshold.
2	LOF	R/O	LOF (Loss of Frame) Defect Declared:
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive STS-3 TOH Processor block is currently declaring an LOF defect condition. The Receive STS-3 TOH Processor block will declare an LOF defect condition, if continues to declare the SEF (Severely Errored Frame) condition for 3ms (or 24 SONET frame periods). 0 – LOF is NOT being declared. 1 – LOF is currently being declared.
		5/0	
1	SEF Defect Declared	R/O	SEF (Severely Errored Frame) Defect Declared: This READ-ONLY bit-field indicates whether or not the Receive STS-3 TOH Processor block is currently declaring an SEF condition. The SEF condition is declared, if the "SEF Declaration Criteria"; per the settings of the FRPATOUT[1:0] bits, within the Receive STS-3 Transport – In-Sync Threshold Value Register (Address Location= 0x112B). O SEF condition is NOT being declared. 1 – SEF condition is currently being declared.
0	LOS	R/O	LOS (Loss of Signal) Indicator:
	Defect Declared	n dat	This READ-ONLY bit-field indicates whether or not the Receive STS-3 TOH Processor block is currently declaring an LOS (Loss of Signal) defect condition. The Receive STS-3 TOH Processor block will declare an LOS defect condition if it detects "LOS_THRESHOLD[15:0]" consecutive "All Zero" bytes in the incoming STS-3 data stream. Note: The user can set the "LOS_THRESHOLD[15:0]" value by writing the appropriate data into the "Receive STS-3 Transport – LOS Threshold
			Value" Register (Address Location= 0x112E and 0x112F). 0 - Indicates that the Receive STS-3 TOH Processor block is NOT currently
			declaring an LOS defect condition. 1 – Indicates that the Receive STS-3 TOH Processor block is currently declaring an LOS defect condition.

Table 77: Receive STS-3 Transport Interrupt Status Register – Byte 2 (Address Location= 0x1109)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Change of AIS-L Condition Interrupt Status	Change of RDI-L Condition Interrupt Status				
R/O	R/O	R/O	R/O	R/O	R/O	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 2	Unused	R/O	
1	Change of AIS-L Condition Interrupt Status	RUR	Change of AIS-L (Line AIS) Condition Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change of AIS-L Condition" interrupt has occurred since the last read of this register. 0 – The "Change of AIS-L Condition" interrupt has not occurred since the last read of this register. 1 – The "Change of AIS-L Condition" interrupt has occurred since the last read of this register. Note: The user can obtain the current state of AIS-L by reading the contents of Bit 0 (AIS-L Defect Declared) within the "Receive STS-3 Transport Status Register – Byte 1" (Address Location=0x1106)
0	Change of RDI-L Condition Interrupt Status	RUR	Change of RDI-L (Line - Remote Defect Indicator) Condition Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change of RDI-L Condition" interrupt has occurred since the last read of this register. 0 - The "Change of RDI-L Condition" interrupt has not occurred since the last read of this register. 1 - The "Change of RDI-L Condition" interrupt has occurred since the last read of this register. Note: The user can obtain the current state of RDI-L by reading out the state of Bit 7 (RDI-L Declared) within the "Receive STS-3 Transport Status Register - Byte 0" (Address Location = 0x1107).

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 78: Receive STS-3 Transport Interrupt Status Register – Byte 1 (Address Location= 0x110A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
New S1 Byte Interrupt Status	Change in S1 Unstable State Interrupt Status	Change in J0 Message Unstable State Interrupt Status	New J0 Message Interrupt Status	Change in J0 Mismatch Condition Interrupt Status	Receive TOH CAP DONE Interrupt Status	Change in (K1, K2) APS Bytes Unstable State Interrupt Status	NEW K1K2 Byte Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION					
7	New S1 Byte	RUR	New S1 Byte Value Interrupt Status					
	Value Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "New S1 Byte Value" Interrupt has occurred since the last read of this register.					
			0 - Indicates that the "New S1 Byte Value" Interrupt has NOT occurred since the last read of this register.					
			1 – Indicates that the "New S1 Byte Value" interrupt has occurred since last read of this register.					
			Note: The user can obtain the value for this most recently accepted value of the S1 byte by reading the "Receive STS-3 Transport S1 Value" register (Address Location= 0x1127).					
6	Change in S1	RUR	Change in S1 Byte Unstable State – Interrupt Status:					
	Byte Unstable State Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in S1 Byte Unstable State" Interrupt has occurred since the last read of this register.					
			O Indicates that the "Change in S1 Byte Unstable State" Interrupt has occurred since the last read of this register.					
		di	1 Indicates that the "Change in S1 Byte Unstable State" Interrupt has not occurred since the last read of this register.					
	Me	O'S	Note: The user can obtain the current "S1 Unstable" state by reading the contents of Bit 6 (S1 Unstable) within the "Receive STS-3 Transport Status Register – Byte 0" (Address Location= 0x1107).					
5	Change in J0 Message	RUR	Change of J0 (Section Trace) Message Unstable condition – Interrupt Status:					
	Unstable State Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of J0 (Section Trace) Message Instability" condition interrupt has occurred since the last read of this register.					
			0 – Indicates that the "Change of J0 (Section Trace) Message Instability" condition interrupt has not occurred since the last read of this register.					
			1 – Indicates that the "Change of J0 (Section Trace) Message Instability" condition interrupt has occurred since the last read of this register.					
4	New J0 Message	RUR	New J0 Trace Message Interrupt Status:					
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "New J0 Trace Message" interrupt has occurred since the last read of this register.					
			$0-\mbox{Indicates}$ that the "New J0 Trace Message Interrupt" has not occurred since the last read of this register.					

			1 – Indicates that the "New J0 Trace Message Interrupt" has occurred since
			the last read of this register.
			Note: The user can read out the contents of the "Receive J0 Trace Buffer", which is located at Address location 0x1300 through 0x133F.
3	Change in J0	RUR	Change in J0 – Section Trace Mismatch Condition" Interrupt Status:
	Mismatch Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in J0 – Section Trace Mismatch Condition" interrupt has occurred since the last read of this register.
			0- Indicates that the "Change in J0 $-$ Section Trace Mismatch Condition" interrupt has not occurred since the last read of this register.
			1 - Indicates that the "Change in J0 - Section Trace Mismatch Condition" interrupt has occurred since the last read of this register.
			Note: The user can determine whether the "J0 – Section Trace Mismatch" condition is "cleared" or "declared" by reading the state of Bit 2 (J0_MIS) within the "Receive STS-3 Transport Status Register – Byte 1 (Address Location= 0x1106).
2	Receive TOH	RUR	Receive TOH Capture DONE - Interrupt Status:
	CAP DONE Interrupt Status		This RESET-upon-READ bit-field indicates whether the "Receive TOH Data Capture" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-3 TOH Processor block will generate an interrupt anytime it has captured the last TOH byte into the Capture Buffer.
			Note: Once the TOH (of a given STS-3 frame) has been captured and loaded into the "Receive TOH Capture" buffer, it will remain there for one SONET frame period.
			0 Indicates that the "Receive TOH Data Capture" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Receive TOH Data Capture" Interrupt has occurred since the last read of this register.
1	Change in APS	RUR	Change of APS (K1, K2 Byte) Unstable Condition – Interrupt Status:
	(K1, K2 Byte) Unstable Status Interrupt Status	She	This RESET-upon-READ bit-field indicates whether or not the "Change of APS (K1, K2 Byte) Instability Condition" interrupt has occurred since the last read of this register.
	1 hogy	49 111	0 – Indicates that the "Change of APS (K1, K2 Byte) Instability Condition" interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change of APS (K1, K2 Byte) Instability Condition" interrupt has occurred since the last read of this register.
			Note: The user can determine whether the "K1, K2 Unstable Condition" is being declared or cleared by reading out the contents of Bit 5 (APS Unstable), within the "Receive STS-3 Transport Status Register – Byte 0" (Address Location = 0x1107).
0	NEW K1K2 Byte	RUR	New K1, K2 Byte Value Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "New K1, K2 Byte Value" Interrupt has occurred since the last read of this register.
			0- Indicates that the "New K1, K2 Byte Value" Interrupt has NOT occurred since the last read of this register.
			$1-\mbox{Indicates}$ that the "New K1, K2 Byte Value" Interrupt has occurred since the last read of this register.
			Note: The user can obtain the contents of the new K1 byte by reading out

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

	the contents of the "Receive STS-3 Transport K1 Value" Register (Address Location= 0x111F). Further, the user can also obtain the contents of the new K2 byte by reading out the contents of the "Receive STS-3 Transport K2 Value" Register (Address Location= 0x1123).
--	--

The product or products mentioned in this deline of the product of products of being manufactured. The product are no ordered (OBS)

Table 79: Receive STS-3 Transport Interrupt Status Register – Byte 0 (Address Location= 0x110B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Change in SF Condition Interrupt Status	Change in SD Condition Interrupt Status	Detection of REI-L Error Interrupt Status	Detection of B2 Error Interrupt Status	Detection of B1 Error Interrupt Status	Change of LOF Condition Interrupt Status	Change of SEF Condition Interrupt Status	Change of LOS Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7	Change in SF	RUR	Change of Signal Failure (SF) Condition Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of SF Condition Interrupt" has occurred since the last read of this register.
			0 - The "Change of SF Condition Interrupt" has NOT occurred since the last read of this register.
			1 – The "Change of SF Condition Interrupt" has occurred since the last read of this register.
			Note: The user can determine the current "SF" condition by reading out the state of Bit 4 (SF Declared) within the "Receive STS-3 Transport Status Register – Byte 0 (Address Location= 0x1107).
6	Change of SD	RUR	Change of Signal Degrade (SD) Condition Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of SD Condition Interrupt" has occurred since the last read of this register.
		, 6	The "Change of SD Condition Interrupt" has NOT occurred since the last read of this register.
		.ct	1. The Change of SD Condition Interrupt" has occurred since the last read of this register.
	or	dueet	Note: The user can determine the current "SD" condition by reading out the state of Bit 3 (SD Declared) within the "Receive STS-3 Transport Status Register – Byte 0 (Address Location= 0x1107).
5	Detection of REI-	RUR	Detection of Line – Remote Error Indicator Interrupt Status:
	L Interrupt Status	andi	This RESET-upon-READ bit-field indicates whether or not the "Declaration of Line – Remote Error Indicator" Interrupt has occurred since the last read of this register.
			0 - The "Declaration of Line - Remote Error Indicator" Interrupt has NOT occurred since the last read of this register.
			1 – The "Declaration of Line – Remote Error Indicator" Interrupt has occurred since the last read of this register.
4	Detection of B2	RUR	Detection of B2 Error Interrupt Status:
	Error Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of B2 Error Interrupt" has occurred since the last read of this register.
			0 - The "Detection of B2 Error Interrupt" has NOT occurred since the last read of this register.
			1 – The "Detection of B2 Error Interrupt" has occurred since the last read of this register.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

3	Detection of B1	RUR	Detection of B1 Error Interrupt Status:
	Error Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of B1 Error Interrupt" has occurred since the last read of this register.
			0 - The "Detection of B1 Error Interrupt" has NOT occurred since the last read of this register.
			1 – The "Detection of B1 Error Interrupt" has occurred since the last read of this register
2	Change of LOF	RUR	Change of Loss of Frame (LOF) Condition Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of LOF Condition" interrupt has occurred since the last read of this register.
			0 - The "Change of LOF Condition" interrupt has NOT occurred since the last read of this register.
			1 – The "Change of LOF Condition" interrupt has occurred since the last read of this register.
			Note: The user can determine the current "LOF" condition by reading out the state of Bit 2 (LOF Defect Declared) within the "Receive STS-3 Transport Status Register – Byte 0 (Address Location=0x1107).
1	Change of SEF Condition	RUR	Change of SEF Condition Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of SEF" Condition Interrupt has occurred since the last read of this register.
			0 - The "Change of SEF Condition" Interrupt has NOT occurred since the last read of this register.
			1 - The "Change of SEF Condition" Interrupt has occurred since the last read of this register.
			Note: The user can determine the current "SEF" condition by reading out the state of Bit 1 (SEF Defect Declared) within the "Receive STS-3 Transport Status Register – Byte 0 (Address Location=0x1107).
0	Change of LOS Condition	RUR	Change of Loss of Signal (LOS) Condition Interrupt Status:
	Interrupt Status	oroll (This RESET-upon-READ bit-field indicates whether or not the "Change of LOS Condition" interrupt has occurred since the last read of this register.
	1/he		The "Change of LOS Condition" Interrupt has NOT occurred since the last read of this register.
	•	grano	1 - The "Change of LOS Condition" Interrupt has occurred since the last read of this register.
			Note: The user can determine the current "LOS" status by reading out the contents of Bit 0 (LOS Defect Declared) within the Receive STS-3 Transport Status Register – Byte 0 (Address Location= 0x1107).

Table 80: Receive STS-3 Transport Interrupt Enable Register – Byte 2 (Address Location= 0x110D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Change of AIS-L Condition Interrupt Enable	Change of RDI-L Condition Interrupt Enable				
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 2	Unused	R/O	
1	Change of AIS-L Condition Interrupt Enable	R/W	Change of AIS-L (Line AIS) Condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change of AIS-L Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions. • When the Receive STS-3 TOH Processor block declares the "AIS-L" condition. • When the Receive STS-3 TOH Processor block clears the "AIS-L" condition. 0 – Disables the "Change of AIS-L Condition" Interrupt. 1 – Enables the "Change of AIS-L Condition" Interrupt. Note: The user can determine the current "AIS-L" condition by reading out the state of Bit 0 (AIS-L) within the "Receive STS-3 Transport Status Register – Byte 1" (Address Location= 0x1106).
0	Change of RDI-L Condition Interrupt Enable	RAVIO	Change of RDI-L (Line Remote Defect Indicator) Condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change of RDI-L Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions. When the Receive STS-3 TOH Processor block declares the "RDI-L" condition. When the Receive STS-3 TOH Processor block clears the "RDI-L" condition. Disables the "Change of RDI-L Condition" Interrupt. This READ/WRITE bit-field permits the user to either enable or disable the "RDI-L" of the user enables the "RDI-L" condition.

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 81: Receive STS-3 Transport Interrupt Enable Register – Byte 1 (Address Location= 0x110E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
New S1 Byte Interrupt Enable	Change in S1 Byte Unstable State Interrupt Enable	Change in J0 Message Unstable State Interrupt Enable	New J0 Message Interrupt Enable	J0 Mismatch Interrupt Enable	Receive TOH CAP DONE Interrupt Enable	Change in APS Unstable State Interrupt Enable	NEW K1K2 Byte Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	New S1 Byte Value Interrupt Enable	R/W	New S1 Byte Value Interrupt Enable: This READ/WRITE bit-field permits the user to enable or disable the "New S1 Byte Value" Interrupt. If the user enables, this interrupt, then the Receive STS-3 TOH Processor block will generate this interrupt anytime it receives and accepts a new S1 byte value. The Receive STS-3 TOH Processor block will accept a new S1 byte after it has received it for 8 consecutive STS-3 frames. 0 – Disables the "New S1 Byte Value" Interrupt. 1 – Enables the "New S1 Byte Value" Interrupt.
6	Change in S1 Unstable State Interrupt Enable	R/W	Change in S1 Byte Unstable State Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change in S1 Byte Unstable State" Interrupt. If the user enables this bit-field, then the Receive STS-3 TOH Processor block will generate an interrupt in response to either of the following conditions. • When the Receive STS-3 TOH Processor block declares the "S1 Byte Instability" condition. • When the Receive STS-3 TOH Processor block clears the "S1 Byte Instability" condition. • Disables the "Change in S1 Byte Unstable State" Interrupt. 1 – Enables the "Change in S1 Byte Unstable State" Interrupt.
5	Change in J0 Message Unstable State Interrupt Enable	RAW	 Change of J0 (Section Trace) Message Instability condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change of J0 Message Instability Condition" Interrupt. If the user enables this interrupt, then the Receive STS-3 TOH Processor block will generate an interrupt in response to either of the following conditions. Whenever the Receive STS-3 TOH Processor block declares the "J0 Message Instability" condition. Whenever the Receive STS-3 TOH Processor block clears the "J0 Message Instability" condition. Disable the "Change of J0 Message Instability" Interrupt. Enables the "Change of J0 Message Instability" Interrupt.
4	New J0 Message Interrupt Enable	R/W	New J0 Trace Message Interrupt Enable: This READ/WRITE bit-field permits the user to enable or disable the "New J0 Trace Message" interrupt. If the user enables this interrupt, then the Receive STS-3 TOH Processor block will generate this interrupt anytime it receives and accepts a new J0 Trace Message. The Receive STS-3 TOH Processor block will accept a new J0

			Trace Message after it has received it 3 (or 5) consecutive times.
			0 – Disables the "New J0 Trace Message" Interrupt.
			1 – Enables the "New J0 Trace Message" Interrupt.
3	J0	R/W	Change in "J0 – Section Trace Mismatch Condition" interrupt enable:
	Mismatch Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in J0 – Section Trace Mismatch condition" interrupt. If the user enables this interrupt, then the Receive STS-3 TOH Processor block will generate an interrupt in response to either of the following events.
			The Receive STS-3 TOH Processor block declares a "J0 – Section Trace Mismatch" condition.
			The Receive STS-3 TOH Processor block clears the "J0 – Section Trace Mismatch" condition.
			Note: The user can determine whether the "JO – Section Trace Mismatch" condition is "cleared or "declared" by reading the state of Bit 2 (J0 Message Mismatch Defect Declared) within the "Receive STS-3 Transport Status Register – Byte 1 (Address Location= 0x1106).
2	Receive	R/W	Receive TOH Capture DONE – Interrupt Enable:
	TOH CAP DONE Interrupt		This READ/WRITE bit-field permits the user to either enable or disable the "Receive TOH Data Capture" interrupt, within the Receive STS-3 TOH Processor Block.
	Enable		If this interrupt is enabled, then the Receive STS-3 TOH Processor block will generate an interrupt anytime it has captured the last TOH byte into the Capture Buffer.
			Note: Once the TOH (of a given STS-3 frame) has been captured and loaded into the "Receive TOH Capture" buffer, it will remain there for one SONET frame period.
			0 – Disables the "Receive TOH Capture" Interrupt.
			1 – Enables the "Receive TOH Capture" Interrupt.
1	Change in APS	R/W	Change of APS (K1, K2 Byte) Instability Condition - Interrupt Enable:
	Unstable State Interrupt	,00	This READ/WRITE bit-field permits the user to either enable or disable the "Change of APS (K1, K2 Byte) Instability condition" interrupt. If the user enables this interrupt, then the Receive STS-3 TOH Processor block will generate an Interrupt in response to either of the following events.
	Enable	6 70	The Receive STS-3 TOH Processor block declares a "K1, K2 Instability" condition.
		98	If the Receive STS-3 TOH Processor block clears the "K1, K2 Instability" condition.
0	New K1K2 Byte Interrupt Enable	R/W	New K1, K2 Byte Value Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "New K1, K2 Byte Value" Interrupt. If the user enables this interrupt, then the Receive STS-3 TOH Processor block will generate this interrupt anytime it receives and accepts a new K1, K2 byte value. The Receive STS-3 TOH Processor block will accept a new K1, K2 byte value, after it has received it within 3 (or 5) consecutive STS-3 frames. 0 – Disables the "New K1, K2 Byte Value" Interrupt.
			1 – Enables the "New K1, K2 Byte Value" Interrupt.

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 82: Receive STS-3 Transport Interrupt Status Register – Byte 0 (Address Location= 0x110F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Change of SF Condition Interrupt Enable	Change of SD Condition Interrupt Enable	Detection of REI-L Error Interrupt Enable	Detection of B2 Error Interrupt Enable	Detection of B1 Error Interrupt Enable	Change of LOF Condition Interrupt Enable	Change of SEF Condition Interrupt Enable	Change of LOS Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION	
7	Change of SF	R/W	Change of Signal Failure (SF) Condition Interrupt Enable:	
	Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of Signal Failure (SF) Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Receive STS-3 TOH Processor block either declares or clears the SF defect.	
			0 - Disables the "Change of SF Condition Interrupt".	
			1 – Enables the "Change of SF Condition Interrupt".	
6	Change of SD	R/W	Change of Signal Degrade (SD) Condition Interrupt Enable:	
	Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of Signal Degrade (SD) Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Receive STS-3 TOH Processor block either declares or clears the SD defect.	
			0 - Disables the "Change of SD Condition Interrupt".	
			1 – Enables the "Change of SD Condition Interrupt".	
5	Detection of	R/W	Detection of Line – Remote Error Indicator Interrupt Enable:	
	REI-L Interrupt Enable		,001	This READ/WRITE bit-field permits the user to either enable or disable the "Declaration of Line – Remote Error Indicator" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Receive STS-3 TOH Processor block declares the "REI-L" defect.
		6, 9	0 – Disables the "Line - Remote Error Indicator" Interrupt.	
	\n'		Enables the "Line – Remote Error Indicator" Interrupt.	
4	Detection of B2	R/W	Detection of B2 Error Interrupt Enable:	
	Error Interrupt Enable	∾.	This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B2 Error" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Receive STS-3 TOH Processor block detects a B2 error.	
			0 – Disables the "Detection of B2 Error Interrupt".	
			1 – Enables the "Detection of B2 Error Interrupt".	
3	Detection of B1	R/W	Detection of B1 Error Interrupt Enable:	
	Error Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B1 Error" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Receive STS-3 TOH Processor block detects a B1 error.	
			0 – Disables the "Detection of B1 Error Interrupt".	
			1 – Enables the "Detection of B1 Error Interrupt".	

2	Change of LOF Condition	R/W	Change of Loss of Frame (LOF) Condition Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of LOF Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions.
			When the Receive STS-3 TOH Processor block declares the "LOF" condition.
			When the Receive STS-3 TOH Processor clears the "LOF" condition.
			0 – Disables the "Change of LOF Condition Interrupt.
			1 – Enables the "Change of LOF Condition" Interrupt.
1	Change of SEF	R/W	Change of SEF Condition Interrupt Enable:
	Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of SEF Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions.
			 When the Receive STS-3 TOH Processor block declares the "SEF" condition. When the Receive STS-3 TOH Processor block clears the
			"SEF" condition.
			0 – Disables the "Change of SEF Condition Interrupt".
			1 – Enables the "Change of SEF Condition Interrupt".
0	Change of LOS	R/W	Change of Loss of Signal (LOS) Condition Interrupt Enable:
	Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of LOF Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions.
		المبي	When the Receive STS-3 TOH Processor block declares the "LOF" condition.
		NI	When the Receive STS-3 TOH Processor block clears the "LOF" condition.
	4	0,00	0 Disables the "Change of LOF Condition Interrupt.
	9	6	1 - Enables the "Change of LOF Condition" Interrupt.
		A .	♥ ·



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 83: Receive STS-3 Transport – B1 Error Count Register – Byte 3 (Address Location= 0x1110)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	B1_Error_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT Number	NAME	Түре	DESCRIPTION
7 - 0	B1_Error_Count [31:24]	RUR	B1 Error Count – MSB: This RESET-upon-READ register, along with "Receive Transport – B1 Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3 TOH Processor block detects a B1 byte error. Note: 1. If the B1 Error Type is configured to be "bit errors", then the Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of bits, within the B1 value that are in error. 2. If the B1 Error Type is configured to be "frame errors", then the Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B1 bytes.

Table 84: Receive STS-3 Transport – B1 Error Count Register – Byte 2 (Address Location= 0x1111)

Віт 7	Віт 6	Віт 5	Віт4	Віт 3	Віт 2	Віт 1	Віт 0		
			B1_Error_C	ount[23:16]					
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	8	0	0	0	0		
	MC ST DE								

		0	0.	
BIT NUMBER	NAME	TYPE	0 (DESCRIPTION
7 - 0	B1_Error_Count	RUR	B1 Erro	or Count (Bits 23 through 16):
	[23:16]	data	Count I	ESET-upon-READ register, along with "Receive Transport – B1 Error Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is ented anytime the Receive STS-3 TOH Processor block detects a B1 or.
			Note:	
			TOH Pi	B1 Error Type is configured to be "bit errors", then the Receive STS-3 rocessor block will increment this 32 bit counter by the number of bits, the B1 value that are in error.
			STS-3	B1 Error Type is configured to be "frame errors", then the Receive TOH Processor block will increment this 32 bit counter by the number es that contain erred B1 bytes.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 85: Receive STS-3 Transport – B1 Error Count Register – Byte 1 (Address Location= 0x1112)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			B1_E	Frror_Count[15	5:8]		
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	B1_Error_Count	RUR	B1 Error Count – (Bits 15 through 8)
	[15:8]		This RESET-upon-READ register, along with "Receive Transport – B1 Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3 TOH Processor block detects a B1 byte error. Note: 1. If the B1 Error Type is configured to be "bit errors", then the Receive STS-3 TOH Processor block with increment this 32 bit counter by the number of bits, within the B1 value that are in error. 2. If the B1 Error Type is configured to be "frame errors", then the Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B1 bytes.

Table 86: Receive STS-3 Transport – B1 Error Count Register – Byte 0 (Address Location= 0x1113)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0
			B1_Error_	Count[7:0]			
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0 (0	0	0	0	0	0

BIT NUMBER	Name	TYPE	DESCRIPTION
7 - 0	B1_Error_Count [7:0]	RUR	This RESET-upon-READ register, along with "Receive Transport – B1 Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STS-3 TOH Processor block detects a B1 byte error. Note: 1. If the B1 Error Type is configured to be "bit errors", then the Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of bits, within the B1 value that are in error. 2. If the B1 Error Type is configured to be "frame errors", then the Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B1 bytes.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 87: Receive STS-3 Transport – B2 Error Count Register – Byte 3 (Address Location= 0x1114)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			B2_Error_C	Count[31:24]			
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	B2_Error_Count	RUR	B2 Error Count – MSB:
	[31:24]		This RESET-upon-READ register, along with "Receive STS-3 Transport – B2 Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3 TOH Processor block detects a B2 byte error. **Note:** 1. If the B2 Error Type is configured to be "bit errors", then the Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of bits, within the B2 value that are in error. 2. If the B2 Error Type is configured to be "frame errors", then the Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B2 bytes.

Table 88: Receive STS-3 Transport – B2 Error Count Register – Byte 2 Address Location= 0x1115)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 2	Віт 1	Віт 0
			B2_Error_Count[23:16]			
RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0 00	0	0	0

BIT NUMBER	Name	TYPE	DESCRIPTION
7 - 0	B2_Error_Count	RUR	B2 Error Count (Bits 23 through 16):
	[23:16]	data	This RESET-upon-READ register, along with "Receive STS-3 Transport – B2 Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3 TOH Processor block detects a B2 byte error.
		'0	Note:
			1.If the B2 Error Type is configured to be "bit errors", then the Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of bits, within the B2 value that are in error.
			2.If the B2 Error Type is configured to be "frame errors", then the Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B2 bytes.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 89: Receive STS-3 Transport – B2 Error Count Register – Byte 1 (Address Location= 0x1116)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
B2_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	B2_Error_Count	RUR	B2 Error Count – (Bits 15 through 8)
	[15:8]		This RESET-upon-READ register, along with "Receive STS-3 Transport – B2 Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3 TOH Processor block detects a B2 byte error. Note: 1. If the B2 Error Type is configured to be "bit errors", then the Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of bits, within the B2 value that are in error. 2. If the B2 Error Type is configured to be "frame errors", then the Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B2 bytes.

Table 90: Receive STS-3 Transport – B2 Error Count Register – Byte 0 (Address Location= 0x1117)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0
	B2_Error_Count[7:0]						
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0 (0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B2_Error_Count[7:0]	RUR	B2 Error Count – LSB: This RESET-upon-READ register, along with "Receive Transport – B2 Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STS-3 TOH Processor block
	o of		Note:
			1. If the B2 Error Type is configured to be "bit errors", then the Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of bits, within the B2 value that are in error.
			2. If the B2 Error Type is configured to be "frame errors", then the Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B2 bytes.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 91: Receive STS-3 Transport – REI-L Error Count Register – Byte 3 (Address Location= 0x1118)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	REI_L_Error_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	REI_L_Error_Count	RUR	REI-L Error Count – MSB:
	[31:24]		This RESET-upon-READ register, along with "Receive Transport – REI-L Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3 TOH Processor block detects a Line - Remote Error Indicator. Note: 1. If the REI-L Error Type is configured to be "bit errors", then the Receive STS-3 TOH Processor block will increment this 32 bit counter by the value within the REI-L fields of the M1 byte. 2. If the REI-L Error Type is configured to be "frame errors", then the Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of frames that contain non-zero REI-L values.

Table 92: Receive STS-3 Transport – REI_L Error Count Register – Byte 2 (Address Location= 0x1119)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 2	Віт 1	Віт 0
			REI_L_Error_Count[23:16]			
RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	REI_L_Error_Count [23:16]	RUR	REI-L Error Count (Bits 23 through 16):
	Theatad	19.	This RESET-upon-READ register, along with "Receive Transport – REI-L Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3 TOH Processor block detects a Line – Remote Error Indicator.
	'0 '		Note:
			1. If the REI-L Error Type is configured to be "bit errors", then the Receive STS-3 TOH Processor block will increment this 32 bit counter by the value within the REI-L fields of the M1 byte.
			2. If the REI-L Error Type is configured to be "frame errors", then the Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of frames that contain non-zero REI-L values.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 93: Receive STS-3 Transport - REI_L Error Count Register - Byte 1 (Address Location= 0x111A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
REI_L_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	REI_L_Error_Count[15:8]	RUR	REI-L Error Count – (Bits 15 through 8)
			This RESET-upon-READ register, along with "Receive Transport – REI-L Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3 TOH Processor block detects a Line –Remote Error Indicator. Note: 1. If the REI-L Error Type is configured to be "bit errors", then the Receive STS-3 TOH Processor block will increment this 32 bit counter by the value within the REI-L fields of the M1 byte. 2. If the REI-L Error Type is configured to be "frame errors", then the Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of frames that contain non-zero REI-L values

Table 94: Receive STS-3 Transport – REI_L Error Count Register – Byte 0 (Address Location= 0x111B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
			REI_L_Error	Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR				
0	0	0	. ⊗ ⊗.	0	0	0	0				

	0 0		<u> </u>
BIT NUMBER	NAME TY	PE	DESCRIPTION
7 - 0	REI_L_Error_Count[7:0] RU	IR	REI-L Error Count – LSB:
	The data din no		This RESET-upon-READ register, along with "Receive Transport – REI-L Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STS-3 TOH Processor block detects a Line – Remote Error Indicator.
			Note:
			1. If the REI-L Error Type is configured to be "bit errors", then the Receive STS-3 TOH Processor block will increment this 32 bit counter by the value within the REI-L fields of the M1 byte.
			2. If the REI-L Error Type is configured to be "frame errors", then the Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of frames that contain non-zero REI-L values.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 95: Receive STS-3 Transport K1 Value (Address Location= 0x111F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			Filtered_K1	_Value[7:0]			
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Filtered_K1_Value[7:0]	R/O	Filtered/Accepted K1 Value:
			These READ-ONLY bit-fields contain the value of the most recently "filtered" K1 value, that the Receive STS-3 TOH Processor block has received. These bit-fields are valid if the K1/K2 pair (to which it belongs) has been received for 3 consecutive STS-3 frames. This register should be polled by Software in order to determine various APS codes.

Table 96: Receive STS-3 Transport K2 Value (Address Location= 0x1123)

Віт 7	Віт 6	Віт 5	Віт 4	Bit 3	Віт 2	Віт 1	Віт 0					
Filtered_K2_Value[7:0]												
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O					
0	0	0	0	800	0	0	0					

BIT NUMBER	Name	Түре	DESCRIPTION
7-0	Filtered_K2_Value[7:0]	R/O	Filtered/Accepted K2 Value: These READ-ONLY bit-fields contain the value of the most recently "filtered" K2 value, that the Receive STS-3 TOH Processor block has received. These bit-fields are valid if the K1/K2 pair (to which it belongs) has been received for 3 consecutive STS-3 frames. This register should be polled by Software in order to determine various APS codes.

Table 97: Receive STS-3 Transport S1 Value (Address Location= 0x1127)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Filtered_S1_Value[7:0]								
Filtered_S1_Value[7:0] R/O R/O R/O R/O R/O R/O							R/O	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Filtered_S1_Value[7:0]	R/O	Filtered/Accepted S1 Value:
			These READ-ONLY bit-fields contain the value of the most recently "filtered" S1 value that the Receive STS-3 TOH Processor block has received. These bit-fields are valid if it has been received for 8 consecutive STS-3 frames.

Table 98: Receive STS-3 Transport – In-Sync Threshold Value (Address Location=0x112B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Bit 2	Віт 1	Віт 0
	Unused		FRPATO	OUT[1:0]	FRPAT	IN[1:0]	Unused
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/O
0	0	0	0	0	0	0	0

D.= N	N	T		2 2			
BIT NUMBER	NAME	Түре	DESCRIPTION				
7 – 5	Unused	R/O					
4 – 3	FRPATOUT	R/W	Framing Pattern SEF Declaration Criteria:				
	[1:0]		These two READ/WRITE bit-fields permit the user to define the SEF Declaration criteria for the Receive STS-3 TOH Processor block. The relationship between the state of these bit-fields and the corresponding SEF Declaration Criteria are presented below.				
		N	FRPATOUT[1:0]	SEF Declaration Criteria			
	O	Pros	01	The Receive STS-3 TOH Processor block will declare an SEF condition if either of the following conditions are true for four consecutive SONET frame periods.			
	1/1/2	dia	If the last (of the 3) A1 bytes, in the STS-3 data stream is erred, or				
		91.		If the first (of the 3) A2 bytes, in the STS-3 data stream, is erred.			
				Hence, for this selection, a total of 16 bits are evaluated for SEF declaration.			
			10	The Receive STS-3 TOH Processor block will declare an SEF condition if either of the following conditions are true for four consecutive SONET frame periods.			
				If the last two (of the 3) A1 bytes, in the STS-3 data stream, are erred, or			
				If the first two (of the 3) A2 bytes, in the STS-3 data stream, are erred.			
				Hence, for this selection, a total of 32 bits are evaluated for SEF declaration.			

xperience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

	1			T. T
			11	The Receive STS-3 TOH Processor block will declare an SEF condition if either of the following conditions are true for four consecutive SONET frame periods.
				If the last three (of the 3) A1 bytes, in the STS-3 data stream, are erred, or
				If the first three (of the 3) A2 bytes, in the STS-3 data stream, are erred.
				Hence, for this selection, a total of 48 bits are evaluated for SEF declaration.
2 - 1	FRPATIN	R/W	Framing Pattern – S	SEF Clearance Criteria:
	[1:0]		criteria for the Rece	RITE bit-fields permit the user to define the "SEF Clearance" ive STS-3 TOH Processor block. The relationship between bit-fields and the corresponding SEF Clearance Criteria are
			FRPATIN[1:0]	SEF Clearance Criteria
			00	The Receive STS-3 TOH Processor block will clear the
			01	SEF condition if both of the following conditions are true for two consecutive SONET frame periods.
				If the last (of the 3) A1 bytes, in the STS-3 data stream is un-erred, and
				If the first (of the 3) A2 bytes, in the STS-3 data stream, is un-erred.
			, uch	Hence, for this selection, a total of 16 bits/frame are evaluated for SEF clearance.
			10 problem of the state of the	The Receive STS-3 TOH Processor block will clear the SEF condition if both of the following conditions are true for two consecutive SONET frame periods.
			TO BUS	If the last two (of the 3) A1 bytes, in the STS-3 data stream, are un-erred, and
			diet al dipe	If the first two (of the 3) A2 bytes, in the STS-3 data stream, are un-erred.
		e or	shoath	Hence, for this selection, a total of 32 bits/frame are evaluated for SEF clearance.
	•	1199	11/11	The Receive STS-3 TOH Processor block will clear the SEF condition if both of the following conditions are true for two consecutive SONET frame periods.
				If the last three (of the 3) A1 bytes, in the STS-3 data- stream, are un-erred, and
				If the first three (of the 3) A2 bytes, in the STS-3 data stream, are un-erred.
				Hence, for this selection, a total of 48 bits/frame are evaluated for SEF declaration.
0	Unused	R/O		

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 99: Receive STS-3 Transport – LOS Threshold Value - MSB (Address Location= 0x112E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
LOS_THRESHOLD[15:8]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	LOS_THRESHOLD[15:8]	R/W	LOS Threshold Value – MSB:
			These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – LOS Threshold Value – LSB" register specify the number of consecutive (All Zero) bytes that the Receive STS-3 TOH Processor block must detect before it can declare an LOS condition.

Table 100: Receive STS-3 Transport – LOS Threshold Value LSB (Address Location= 0x112F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт(3	Віт 2	Віт 1	Віт 0				
	LOS_THRESHOLD[7:0]										
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
1	1	1	1 🔇	1	1	1	1				

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	LOS_THRESHOLD[7:0]	R/W	LOS Threshold Value – LSB:
	ð	Orle	These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – LOS Threshold Value – MSB" register specify the number of consecutive (All Zero) bytes that the Receive STS-3 TOH Processor block must detect before it can declare an LOS condition.
	The production of the data and the	nayna	



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 101: Receive STS-3 Transport – Receive SF SET Monitor Interval – Byte 2 (Address Location= 0x1131)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
SF_SET_MONITOR_WINDOW[23:16]									
R/W R/W R/W R/W R/W R/W									
1	1	1	1	1	1	1	1		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SF_SET_MONITOR_ WINDOW [23:16]	R/W	SF_SET_MONITOR_INTERVAL – MSB: These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SF SET Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the number of STS-3 Frame periods that will constitute a SET Sub-Interval for SF (Signal Failure). When the Receive STS-3 TOH Processor block is checking for SF, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors exceeds that of programmed into the "Receive STS-3 Transport SF SET Threshold" register, then an SF condition will be declared.

Table 102: Receive STS-3 Transport – Receive SF SET Monitor Interval – Byte 1 (Address Location= 0x1132)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 2	Віт 1	Віт 0		
SF_SET_MONITOR_WINDOW[15:8]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	(1001	1	1	1		

BIT Number	NAME NAME	DESCRIPTION
7 - 0	SF_SET_MONITOR_WINDOW R/ [15:8]	SF_SET_MONITOR_INTERVAL (Bits 15 through 8): These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SF SET Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the number of STS-3 Frame periods that will constitute a SET Sub-Interval for SF (Signal Failure). When the Receive STS-3 TOH Processor block is checking for SF, it will accumulate B2 bit errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 bit errors exceeds that of programmed into the "Receive STS-3 Transport SE SET Threshold" register then an SE condition will be
		SF SET Threshold" register, then an SF condition will be declared.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 103: Receive STS-3 Transport – Receive SF SET Monitor Interval – Byte 0 (Address Location= 0x1133)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	SF_SET_MONITOR_WINDOW[7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
1	1	1	1	1	1	1	1			

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SF_SET_MONITOR_WINDOW[7:0]	R/W	SF_SET_MONITOR_INTERVAL - LSB:
			These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SF SET Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the number of STS-3 Frame periods that will constitute a SET Sub-Interval for SF (Signal Failure). When the Receive STS-3 TOH Processor block is checking for SF, it will accumulate B2 bit errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 bit errors exceeds that of programmed into the "Receive STS-3 Transport SF SET Threshold" register, then an SF condition will be declared.

Table 104: Receive STS-3 Transport – Receive SF SET Threshold – Byte 1 (Address Location= 0x1136)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0		
SF_SET_THRESHOLD[15:8]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1 (0	010	1	1	1	1		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SF_SET_THRESHOLO[15:8]	R/W	SF_SET_THRESHOLD – MSB: These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SF SET Threshold – Byte 0" registers permit the user to specify the number of B2 bit errors that will
	deand		cause the Receive STS-3 TOH Processor block to declare an SF (Signal Failure) condition. When the Receive STS-3 TOH Processor block is checking for
			SF, it will accumulate B2 errors for a total of 8 SET Sub- Interval periods. If the number of accumulated B2 errors exceeds that of programmed into this and the "Receive STS-3 Transport SF SET Threshold – Byte 0" register, then an SF condition will be declared.



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 105: Receive STS-3 Transport – Receive SF SET Threshold – Byte 0 Address Location= 0x1137)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
SF_SET_THRESHOLD[7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SF_SET_THRESHOLD[7:	R/W	SF_SET_THRESHOLD - LSB:
	OJ		These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SF SET Threshold – Byte 1" registers permit the user to specify the number of B2 bit errors that will cause the Receive STS-3 TOH Processor block to declare an SF (Signal Failure) condition. When the Receive STS-3 TOH Processor block is checking for SF, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors exceeds that of programmed into this and the "Receive STS-3 Transport SF SET Threshold – Byte 1" register, then an SF condition will be declared.

Table 106: Receive STS-3 Transport – Receive SF CLEAR Threshold – Byte 1 (Address Location= 0x113A)

Віт 7	Віт 6	Віт 5	Bit 4 Bit 3	Віт 2	Віт 1	Віт 0				
SF_CLEAR_THRESHOLD[15:8]										
R/W	R/W	R/W	R/W C R/W	R/W	R/W	R/W				
1	1	1	1 0 0 1	1	1	1				

BIT NUMBER	NAME TYP	DESCRIPTION
7 - 0	SF_CLEAR_THRESHOLD RAV	These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SF CLEAR Threshold – Byte 0" registers permit the user to specify the upper limit for the number of B2 bit errors that will cause the Receive STS-3 TOH Processor block to clear the SF (Signal Failure) condition. When the Receive STS-3 TOH Processor block is checking for clearing SF, it will accumulate B2 errors for a total of 8 CLEAR Sub-Interval periods. If the number of accumulated B2 errors is less than that programmed into this and the "Receive STS-3 Transport SF CLEAR Threshold – Byte 0" register, then an SF condition will be cleared.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 107: Receive STS-3 Transport – Receive SF CLEAR Threshold – Byte 0 (Address Location= 0x113B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
SF_CLEAR_THRESHOLD[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SF_CLEAR_THRESHOLD [7:0]	R/W	SF_CLEAR_THRESHOLD – LSB: These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SF CLEAR Threshold – Byte 1" registers permit the user to specify the upper limit for the number of B2 bit errors that will cause the Receive STS-3 TOH Processor block to clear the SF (Signal Failure) condition. When the Receive STS-3 TOH Processor block is checking for clearing SF, it will accumulate B2 errors for a total of 8 CLEAR Sub-Interval periods. If the number of accumulated B2 errors is less than that programmed into this and the "Receive STS-3 Transport SF CLEAR Threshold – Byte 1" register, then an SF condition will be cleared.

Table 108: Receive STS-3 Transport – Receive SD Set Monitor Interval – Byte 2 (Address Location= 0x113D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
SD_SET_MONITOR_WINDOW[23:16]										
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0	0	0	.O O	0	0	0	0			

BIT NUMBER	NAME	Түре	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW [23:16]	R/W	SD_SET_MONITOR_INTERVAL – MSB: These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SD SET Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the number of STS-3 Frame periods that will constitute a SET Sub-Interval for SD (Signal Degrade) declaration. When the Receive STS-3 TOH Processor block is checking for SD, it will accumulate B2 bit errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 bit errors exceeds that of programmed into the "Receive STS-3 Transport SD SET Threshold" register, then an SD condition will be declared.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS



Rev 2.0.0

Table 109: Receive STS-3 Transport – Receive SD Set Monitor Interval – Byte 1 (Address Location= 0x113E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
SD_SET_MONITOR_WINDOW[15:8]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW[15:8]	R/W	SD_SET_MONITOR_INTERVAL - Bits 15 through 8:
			These READ/WRITE bits, along the contents of the "Receive STS-3 Transport - SD SET Monitor Interval - Byte 2 and Byte 0" registers permit the user to specify the number of STS-3 Frame periods that will constitute a SET Sub-Interval for SD (Signal Degrade) declaration. When the Receive STS-3 TOH Processor block is checking for SD, it will accumulate B2 bit errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 bit errors exceeds that of programmed into the "Receive STS-3 Transport SD SET Threshold" register, then an SD condition will be declared.

Table 110: Receive STS-3 Transport – Receive SD Set Monitor Interval – Byte 0 (Address Location= 0x113F)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0	
SD_SET_MONITOR_WINDOW[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0 🔾	200	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW[7:0]	R/W	SD_SET_MONITOR_INTERVAL – LSB: These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SD SET Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the number of STS-3 Frame periods that will constitute a SET Sub-Interval for SD (Signal Degrade) declaration.
			When the Receive STS-3 TOH Processor block is checking for SD, it will accumulate B2 bit errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 bit errors exceeds that of programmed into the "Receive STS-3 Transport SD SET Threshold" register, then an SD condition will be declared.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 111: Receive STS-3 Transport - Receive SD SET Threshold - Byte 1 (Address Location= 0x1142)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
SD_SET_THRESHOLD[15:8]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SD_SET_THRESHOLD[15:8]	R/W	SD_SET_THRESHOLD - MSB:
			These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SD SET Threshold – Byte 0" registers permit the user to specify the number of B2 bit errors that will cause the Receive STS-3 TOH Processor block to declare an SD (Signal Degrade) condition. When the Receive STS-3 TOH Processor block is checking for SD, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors exceeds that of programmed into this and the "Receive STS-3 Transport SD SET Threshold – Byte 0" register, then an SD condition will be declared.

Table 112: Receive STS-3 Transport - Receive SD SET Threshold - Byte 0 (Address Location= 0x1143)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SD_SET_THRESHOLD[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	100	1	1	1	1		
	All to the second secon								

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SD_SET_THRESHOLD[7:0]	R/W	SD_SET_THRESHOLD – LSB: These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SD SET Threshold – Byte 1" registers permit the user to specify the number of B2 bit errors that will cause the Receive STS-3 TOH Processor block to declare an
			SD (Signal Degrade) condition. When the Receive STS-3 TOH Processor block is checking for SD, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors exceeds that of programmed into this and the "Receive STS-3 Transport SD SET Threshold – Byte 1" register, then an SD condition will be declared.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 113: Receive STS-3 Transport – Receive SD CLEAR Threshold – Byte 1 (Address Location= 0x1146)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	SD_CLEAR_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SD_CLEAR_THRESHOLD[15:8]	R/W	SD_CLEAR_THRESHOLD - MSB:
			These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SD CLEAR Threshold – Byte 0" registers permit the user to specify the upper limit for the number of B2 bit errors that will cause the Receive STS-3 TOH Processor block to clear the SD (Signal Degrade) condition. When the Receive STS-3 TOH Processor block is checking for clearing SD, it will accumulate B2 errors for a total of 8 CLEAR Sub-interval periods. If the number of accumulated B2 errors is less than that programmed into this and the "Receive STS-3 Transport SD CLEAR Threshold – Byte 0" register, then an SD condition will be cleared.

Table 114: Receive STS-3 Transport – Receive SD CLEAR Threshold – Byte 1 (Address Location= 0x1147)

	1			·			
Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0
			SD CLEAR THE	RESHOLD[7:0]]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1 .	2110	1	1	1	1

BIT NUMBER	NAME	YPE	DESCRIPTION
7 - 0	SD_CLEAR_THRESHOLD[7:0] R	R/W	SD_CLEAR_THRESHOLD - LSB:
	Ti dat and I		These READ/WRITE bits, along the contents of the "Receive STS-3 Transport – SD CLEAR Threshold – Byte 1" registers permit the user to specify the upper limit for the number of B2 bit errors that will cause the Receive STS-3 TOH Processor block to clear the SD (Signal Degrade) condition.
			When the Receive STS-3 TOH Processor block is checking for clearing SD, it will accumulate B2 errors for a total of 8 CLEAR Sub-Interval periods. If the number of accumulated B2 errors is less than that programmed into this and the "Receive STS-3 Transport SD CLEAR Threshold – Byte 1" register, then an SD condition will be cleared.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 115: Receive STS-3 Transport – Force SEF Condition Register (Address Location= 0x114B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused						
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 1	Unused	R/O	
0	SEF FORCE	R/W	SEF Force:
			This READ/WRITE bit-field permits the user to force the Receive STS-3 TOH Processor block to declare an SEF defect. The Receive STS-3 TOH Processor block will then attempt to reacquire framing. Writing a "1" into this bit-field configures the Receive STS-3 TOH Processor block to declare the SEF defect. The Receive STS-3 TOH Processor block will automatically set this bit-field to "0" once it has reacquired framing (e.g., has detected two consecutive STS-3 frames with the correct A1 and A2 bytes).

Table 116: Receive STS-3 Transport – Receive Jo Trace Buffer Control Register (Address Location= 0x114F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 2	Віт 1	Віт 0
	Unused		READ SEL ACCE		MSG L	ENGTH
R/O	R/O	R/O	R/W R/W	/ R/W	R/W	R/W
0	0	0	0 0 0	0	0	0

		MC	" all pe
BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 5	Unused	R/O	3
4	READ SEL	R/W	Receive Section Trace (J0) Message Buffer Read Selection:
	7.90	and.	This READ/WRITE bit-field permits a user to specify which of the following buffer segments to read.
			a. Valid Message Buffer
			b. Expected Message Buffer
			0 – Executing a READ to the Receive Section Trace (J0) Message Buffer, will return contents within the "Valid Message" buffer.
			1 – Executing a READ to the Receive Section Trace (J0) Message Buffer, will return contents within the "Expected Message Buffer".
			Note: In the case of the Receive STS-3 TOH Processor block, the "Receive J0 Trace Buffer" is located at Address location 0x1300 through 0x133F.
3	ACCEPT THRD	R/W	Message Accept Threshold:
			This READ/WRITE bit-field permits a user to select the number of consecutive times that the Receive STS-3 TOH Processor block must receive a given

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

		Section Trace Mess	sage, before it is accepted, as described below.				
			STS-3 TOH Processor block accepts the Section Message if it the third time in succession.				
		1 – The Receive STS-3 TOH Processor block accepts the Section Message after it has received in the fifth time in succession.					
MSG TYPE	R/W	Message Alignme	nt Type:				
		TOH Processor blo	bit-field permits a user to specify how the Receive STS-3 ock will locate the boundary of the incoming Section Trace ted below.				
		0 – The Section Tra	ace Message boundary is indicated by "Line Feed".				
		1 – The Section Trace Message boundary is indicated by the presence of a "1" in the MSB of a the first byte (within the J0 Trace Message).					
MSG LENGTH	R/W						
		Trace Message, the The relationship be	TE bit-fields permit the user to specify the length of the Johat the Receive STS-3 TOH Processor block will receive. tween the content of these bit-fields and the corresponding Length is presented below.				
		MSG LENGTH	Resulting J0 Trace Message Length				
		00	1 Byte				
		01	16 Bytes				
		10/11	64 Bytes				
Z'II	sologia	Just los biodisos sheet are not be of	de la company de				
	MSG LENGTH	MSG LENGTH R/W	MSG TYPE R/W Message Alignme This READ/WRITE TOH Processor blo Message, as indica 0 – The Section Tra in the MSB of a the MSG LENGTH R/W MSG LENGTH MSG LENGTH O0 MSG LENGTH O0				

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 117: Receive STS-3 Transport – Receive SD Burst Error Tolerance – Byte 1 (Address Location= 0x1152)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
SD_BURST_TOLERANCE[15:8]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SD_BURST_TOLERANCE	R/W	SD_BURST_TOLERANCE - MSB:
	[15:8]		These READ/WRITE bits, along with the contents of the "Receive STS-3 Transport – SD BURST Tolerance – Byte 0" registers permit the user to specify the maximum number of B2 bit errors that the Receive STS-3 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-3 frame period), when determining whether or not to declare an SD (Signal Degrade) defect condition. Note: The purpose of this feature is to permit the user to provide some level of B2 error burst filtering, when the Receive STS-3 TOH Processor block is accumulating B2 byte errors in order to declare the SD defect condition. The user can implement this feature in order to configure the Receive STS-3 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SD defect condition.

Table 118: Receive STS-3 Transport – Receive SD Burst Error Tolerance – Byte 0 (Address Location= 0x1153)

			74			
Віт 7	Віт 6	Віт 5	Віт 3	Віт 2	Віт 1	Віт 0
		SD_BURST_T	OLERANCE[7:0]		
R/W	R/W	R/W R/W	R/W	R/W	R/W	R/W
1	1	89 X X 1	1	1	1	1

10.00 10

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SD_BURST_TOLERANCE	R/W	SD_BURST_TOLERANCE - LSB: These READ/WRITE bits, along with the contents of the "Receive STS-3 Transport - SD BURST Tolerance - Byte 1" registers permit the user to specify the maximum number of B2 bit errors that the Receive STS-3 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-3 frame period), when determining whether or not to declare an SD (Signal Degrade) defect condition. Note: The purpose of this feature is to permit the user to provide some level of B2 error burst filtering, when the Receive STS-3 TOH Processor block is accumulating B2 byte errors in order to declare the SD defect condition. The user can implement this feature in order to configure the Receive STS-3 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SD defect condition.

Table 119: Receive STS-3 Transport – Receive SF Burst Error Tolerance – Byte 1 (Address Location= 0x1156)

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
SF_BURST_TOLERANCE[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SF_BURST_TOLERANCE[15:8]	R/W	SF_BURST_TOLERANCE - MSB:
			These READ/WRITE bits, along with the contents of the "Receive STS-3 Transport – SF BURST Tolerance – Byte 0" registers permit the user to specify the maximum number of B2 bit errors that the Receive STS-3 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-3 frame period), when determining whether or not to declare an SF (Signal Failure) defect condition.
			Note: The purpose of this feature is to permit the user to provide some level of B2 error burst filtering, when the Receive STS-3 TOH Processor block is accumulating B2 byte errors in order to declare the SF defect condition. The user can implement this feature in order to configure the Receive STS-3 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SF defect condition.
	The Product (of and may	production of the production o	ordered of

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 120: Receive STS-3 Transport – Receive SF Burst Error Tolerance – Byte 0 (Address Location= 0x1157)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
SF_BURST_TOLERANCE[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SF_BURST_TOLERANCE[7:0]	R/W	SF_BURST_TOLERANCE - LSB:
		wich	These READ/WRITE bits, along with the contents of the "Receive STS-3 Transport – SF BURST Tolerance – Byte 1" registers permit the user to specify the maximum number of B2 bit errors that the Receive STS-3 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-3 frame period), when determining whether or not to declare an SF (Signal Failure) defect condition. *Note: The purpose of this feature is to permit the user to provide some level of B2 error burst filtering, when the Receive STS-3 TOH Processor block is accumulating B2 byte errors in order to declare the SF defect condition. The user can implement this feature in order to configure the Receive STS-3 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SF defect condition.

Table 121: Receive STS-3 Transport - Receive SD Clear Monitor Interval - Byte 2 (Address Location= 0x1159)

			2				
Віт 7	Віт 6	Віт 5	BIT4	Віт 3	Віт 2	Віт 1	Віт 0
SD_CLEAR_MONITOR_WINDOW[23:16]							
R/W	R/W	OR/W	R/W	R/W	R/W	R/W	R/W
1	1	6, 9, 4	1	1	1	1	1

The to the

D N	<u>, Xo</u>	T	D
BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_ WINDOW[23:16]	R/W	SD_CLEAR_MONITOR_INTERVAL – MSB: These READ/WRITE bits, along with the contents of the "Receive STS-3 Transport – SD Clear Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the number of STS-3 Frame periods that will constitute a CLEAR Sub-Interval for SD (Signal Degrade). When the Receive STS-3 TOH Processor block is checking for clearing the SD defect, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors is less than that of programmed into the "Receive STS-3 Transport SD Clear Threshold" register, then the SD defect will be cleared.

Table 122: Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 1 (Address Location= 0x115A)

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
SD_CLEAR_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW[15:8]	R/W	SD_CLEAR_MONITOR_INTERVAL - Bits 15 through 8:
			These READ/WRITE bits, along with the contents of the "Receive STS-3 Transport – SD Clear Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the number of STS-3 Frame periods that will constitute a CLEAR Sub-Interval for SD (Signal Degrade). When the Receive STS-3 TOH Processor block is checking for clearing the SD defect, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors is less than that of programmed into the "Receive STS-3 Transport SD Clear Threshold" tegister, then the SD defect will be cleared.

Table 123: Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 0 (Address Location= 0x115B)

Віт 7	Віт 6	Віт 5	Віт 4	Brt 3	Віт 2	Віт 1	Віт 0
			SD_CLEAR_I	MONITOR_W	INDOW[7:0]		
R/W	R/W	R/W	R/W	O R/W	R/W	R/W	R/W
1	1	1	1 0	, ' d.	1	1	1

	ductal	Po	
BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW[7,0]	R/W	SD_CLEAR_MONITOR_INTERVAL – LSB: These READ/WRITE bits, along with the contents of the "Receive STS-3 Transport – SD Clear Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the number of STS-3 Frame periods that will constitute a CLEAR Sub-Interval for SD (Signal Degrade). When the Receive STS-3 TOH Processor block is checking for clearing the SD defect, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors is less than that of programmed into the "Receive STS-3 Transport SD Clear Threshold" register, then the SD defect will be cleared.

Table 124: Receive STS-3 Transport – Receive SF Clear Monitor Interval – Byte 2 (Address Location= 0x115D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Ş	SF_CLEAR_M	IONITOR_WIN	NDOW[23:16]		



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

| R/W |
|-----|-----|-----|-----|-----|-----|-----|-----|
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDO W [23:16]	R/W	SF_CLEAR_MONITOR_INTERVAL – MSB: These READ/WRITE bits, along with the contents of the "Receive STS-3 Transport – SF Clear Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the number of STS-3 Frame periods that will constitute a CLEAR Sub-Interval for SF (Signal Failure). When the Receive STS-3 TOH Processor block is checking for clearing the SF defect, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors is less than that of programmed into the "Receive STS-3 Transport SF Clear Threshold" register, then the SF defect will be cleared.

Table 125: Receive STS-3 Transport – Receive SF Clear Monitor Interval – Byte 1 (Address Location= 0x115E)

Віт 7	Віт 6	Віт 5	Віт 4	O BIT3	Віт 2	Віт 1	Віт 0
		SF_0	CLEAR_MONIT	OR_WINDOW[15:8]		
R/W	R/W	R/W	R/W	RW	R/W	R/W	R/W
1	1	1	10.0	, (Y	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDOW [15:8]	R/W	SF_CLEAR_MONITOR_INTERVAL – Bits 15 through 8: These READ/WRITE bits, along with the contents of the "Receive STS-3 Transport – SF Clear Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the number of STS-3 Frame periods that will constitute a CLEAR Sub-Interval for SF (Signal Failure). When the Receive STS-3 TOH Processor block is checking for clearing the SF defect, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors is less than that of programmed into the "Receive STS-3 Transport SF Clear Threshold" register, then the SF defect will be cleared.

Table 126: Receive STS-3 Transport – Receive SF Clear Monitor Interval – Byte 0 (Address Location= 0x115F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	SF_CLEAR_MONITOR_WINDOW[7:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1



Rev 2.0.0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDOW	R/W	SF_CLEAR_MONITOR_INTERVAL - LSB:
	[7:0]		These READ/WRITE bits, along with the contents of the "Receive STS-3 Transport – SF Clear Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the number of STS-3 Frame periods that will constitute a CLEAR Sub-Interval for SF (Signal Failure).
			When the Receive STS-3 TOH Processor block is checking for clearing the SF defect, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors is less than that of programmed into the "Receive STS-3 Transport SF Clear Threshold" register, then the SF defect will be cleared.

of programmed into Clear Threshold" recleared.

It cleared.

The hold the difference of the cleared of programmed into Clear Threshold" recleared.

The hold the cleared of the cleared of

Table 127: Receive STS-3 Transport – Auto AIS Control Register (Address Location= 0x1163)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit AIS-P (Down- stream) Upon J0 Message Unstable	Transmit AIS-P (Down- stream) Upon J0 Message Mismatch	Transmit AIS-P (Down- stream) Upon SF	Transmit AIS-P (Down- stream) Upon SD	Transmit AIS-P (Down- stream) upon Loss of Optical Carrier AIS	Transmit AIS-P (Down- stream) upon LOF	Transmit AIS-P (Down- stream) upon LOS	Transmit AIS-P (Down- stream) Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Name Transmit AIS-P (Down-stream) upon J0 Message Unstable	TYPE R/W	Transmit Path AIS upon Detection of Unstable Section Trace (J0): This READ/WRITE bit-field permits the user to configure the Receive STS-3 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive SONET POH Processor blocks), anytime it detects an Unstable Section Trace (J0) condition in the "incoming" STS-3 data-stream. O – Does not configure the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects an "Unstable Section Trace" condition. 1 – Configures the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects an "Unstable Section Trace" condition. Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this
6	Transmit AIS-P (Down-stream) Upon J0 Message Mismatch	RIVA	Transmit Path AIS (AIS-P) upon Detection of Section Trace (J0) Message Mismatch: This READ/WRITE bit-field permits the user to configure the Receive STS-3 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive SONET POH Processor blocks), anytime it detects a Section Trace (J0) Message Mismatch condition in the "incoming" STS-3 data stream. O – Does not configure the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects a "Section Trace Message Mismatch" condition.
			Configures the Receive STS-3 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects a "Section Trace Message Mismatch" condition. Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
5	Transmit AIS-P (Down-stream) upon SF	R/W	Transmit Path AIS upon Signal Failure (SF): This READ/WRITE bit-field permits the user to configure the Receive STS-3 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive SONET POH Processor blocks), anytime it declares an SF condition.

EXAR Experience Our Connectivit

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			transmit	not configure the Receive STS-3 TOH Processor block to the AIS-P indicator (via the "downstream" traffic) upon n of the SF defect.
				gures the Receive STS-3 TOH Processor block to transmit the icator (via the "downstream" traffic) upon declaration of the SF
				The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
4		R/W	Transmit	Path AIS upon Signal Degrade (SD):
	(Down-stream) upon SD		STS-3 TO Indicator	D/WRITE bit-field permits the user to configure the Receive H Processor block to automatically transmit a Path AIS (AIS-P) via the "downstream" traffic (e.g., towards the Receive SONET essor blocks), anytime it declares an SD condition.
			transmit declaratio	not configure the Receive STS-3 TOH Processor block to the AIS-P indicator (via the "downstream" traffic) upon n of the SD defect.
				gures the Receive STS-3 TOH Processor block to transmit the cator (via the downstream" traffic) upon declaration of the SD
				The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition
3		R/W	Transmit	Path AlS upon Loss of Optical Carrier condition:
	(Down-stream) upon Loss of Optical Carrier		STS-3 TO Indicator	DWRITE bit-field permits the user to configure the Receive H Processor block to automatically transmit a Path AIS (AIS-P) bia the "downstream" traffic (e.g., towards the Receive SONET cessor blocks), anytime it detects a "Loss of Optical Carrier"
	50.	Jucy,		not configure the Receive STS-3 TOH Processor block to ne AIS-P indicator upon detection of a "Loss of Optical Carrier"
	e P	Sho	1 - Config AIS-P indi	gures the Receive STS-3 TOH Processor block to transmit the cator upon detection of a "Loss of Optical Carrier" condition.
	111.98	da		The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
2		R/W	Transmit	Path AIS upon Loss of Frame (LOF):
	(Down-stream) upon LOF		STS-3 TO Indicator	D/WRITE bit-field permits the user to configure the Receive H Processor block to automatically transmit a Path AIS (AIS-P) via the "downstream" traffic (e.g., towards the Receive SONET essor block), anytime it declares an LOF condition.
			transmit	not configure the Receive STS-3 TOH Processor block to the AIS-P indicator (via the "downstream" traffic) upon n of the LOF defect.
				gures the Receive STS-3 TOH Processor block to transmit the cator (via the "downstream" traffic) upon declaration of the LOF
				The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-3 TOH Processor block to

			automatically transmit the AIS-P indicator, in response to this defect condition.
1	Transmit AIS-P (Down-stream) upon	R/W	Transmit Path AIS upon Loss of Signal (LOS):
	LOS		This READ/WRITE bit-field permits the user to configure the Receive STS-3 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive SONET POH Processor block), anytime it declares an LOS condition.
			0 - Does not configure the Receive STS-3 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) anytime it declares the LOS defect.
			1 – Configures the Receive STS-3 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) anytime it declares the LOS defect.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
0	Transmit AIS-P	R/W	Automatic Transmission of AIS-P Enable:
	(Down-stream) Enable		This READ/WRITE bit-field serves two purposes.
			It permits the user to configure the Receive STS-3 TOH Processor block to automatically transmit the Path AIS (AIS-P) indicator, via the downstream traffic (e.g., towards the Receive SONET POH Processor blocks), upon detection of an SF, SD, Section Trace Mismatch, Section Trace Unstable, LOF, LOS or Loss of Optical Carrier conditions.
		, <	It also permits the user to configure the Receive STS-3 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive SONET POH Processor blocks) anytime it detects an AIS-L condition in the "incoming " STS-3 data-stream.
		ct of	O Configures the Receive STS-3 TOH Processor block to NOT automatically transmit the AIS-P indicator (via the "downstream" traffic) upon detection of the AIS-L or any of the "above-mentioned" conditions.
	prodi	1001	Configures the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) upon detection of any of the "above-mentioned" condition.
	The production	Ma,	Note: The user must also set the corresponding bit-fields (within this register) to "1" in order to configure the Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator upon detection of a given a



Table 128: Receive STS-3 Transport – Serial Port Control Register (Address Location= 0x1167)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Unused				RxTOH_CLOCK_SPEED[7:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT Number	Name	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3 - 0	RxTOH_CLOCK_SPEED[7:0]	R/W	RxTOHCIk Output Clock Signal Speed: These READ/WRITE bit-fields permit the user to specify the frequency of the "RxTOHCIk output clock signal. The formula that relates the contents of these register bits to the "RxTOHCIk" frequency is presented below. FREQ = 19.44 /[24] (RxTOH_CLOCK_SPEED + 1) Note: For STS-3/STM-1 applications, the frequency of the RxTOHCIk output signal must be in the range of 0.6075MHz to 9.72MHz

Table 129: Receive STS-3 Transport – Auto AlS in Downstream STS-1s) Control Register (Address Location= 0x116B)

Віт 7	Віт 6	Віт 5	Віт 4	Bit 3	Віт 2	Віт 1	Віт 0
Unused	Unused	Transmit AIS-P (via Downstream STS-1s) upon LOS	Transmit AIS-P (via Downstream STS-1s) upon LOF	Fransmit AIS-P (via Downstream STS-1s) upon SD	Transmit AIS-P (via Downstream STS-1s) upon SF	AIS-L Output Enable	Transmit AIS-P (via Downstream STS-1s) Enable
R/O	R/O	R/W	C R/W	R/W	R/W	R/W	R/W
0	0	00 10	0	0	0	0	0

	The to supply						
BIT Number	NAME	TYPE	DESCRIPTION				
7 - 6	Unused	R/O					
5	Transmit AIS-P (via Downstream STS-1s)	R/W	Transmit AIS-P (via Downstream STS-1s) upon LOS (Loss of Signal):				
	upon LOS		This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor blocks (in each channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3 TOH Processor block declares the LOS defect.				
			0 bi	0 – Does not configure all "activated" Transmit STS-1 POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3 TOH Processor block declares the LOS defect.			
			1 - Configures all "activated" Transmit STS-1POH Processor blocks to				

		automatically transmit the AIS-P Indicator via the "downstream" STS-1
		signals, anytime the Receive STS-3 TOH Processor block declares the LOS defect.
		Note:
		1. In the "long-run" the function of this bit-field is exactly the same as that of Bit 1 (Transmit AIS-P Down-stream – Upon LOS), within the Receive STS-3 Transport – Auto AIS Control Register (Address Location= 0x1163). The only difference is that this register bit will cause each of the "downstream" Transmit STS-1 POH Processor blocks to IMMEDIATELY begin to transmit the AIS-P condition whenever the Receive STS-3 TOH Processor block declares the LOS defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the NE declaring the LOS defect.
		2. In the case of Bit 1 (Transmit AIS-P Downstream – Upon LOS), several SONET frame periods are required (after the Receive STS-3 TOH Processor block has declared the LOS defect), before the Transmit STS-1 POH Processor blocks will begin the process of transmitting the AIS-P indicators.
		3. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STS-1s Enable) within this register, in order enable this feature.
4 Transmit AIS-P (via Downstream STS-1s)	R/W	Transmit AIS-R (via Downstream STS-1s) upon LOF (Loss of Frame):
upon LOF		This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor blocks (in each channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3 TOH Processor block declares the LOF detect. 0 – Does not configures all "activated" Transmit STS-1 POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream"
produ	000	STS-1 signals, anytime the Receive STS-3 TOH Processor block declares the LOF defect. 1 Configures all "activated" Transmit STS-1POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3 TOH Processor block declares the LOF defect.
10 10	40,	Note:
The data		1. In the "long-run" the function of this bit-field is exactly the same as that of Bit 2 (Transmit AIS-P Down-stream – Upon LOF), within the Receive STS-3 Transport – Auto AIS Control Register (Address Location=0x1163). The only difference is that this register bit will cause each of the "downstream" Transmit STS-1 POH Processor blocks to IMMEDIATELY begin to transmit the AIS-P condition whenever the Receive STS-3 TOH Processor block declares the LOF defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the NE declaring the LOF defect.
		2. In the case of Bit 2 (Transmit AIS-P Downstream – Upon LOF), several SONET frame periods are required (after the Receive STS-3 TOH Processor block has declared the LOS defect), before the Transmit STS-1 POH Processor blocks will begin the process of transmitting the AIS-P indicators.
		3. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STS-1s Enable) within this register, in order enable this feature.

Experience Our Connectivity.

Rev 2.0.0

3	Transmit AIS-P (via	R/W	Transmit AIS-P (via Downstream STS-1s) upon SD (Signal Degrade):
	Downstream STS-1s) upon SD		This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor blocks (in each channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3 TOH Processor block declares the SD defect.
			0 – Does not configures all "activated" Transmit STS-1 POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3 TOH Processor block declares the SD defect.
			1 – Configures all "activated" Transmit STS-1POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3 TOH Processor block declares the SD defect.
			Note:
			1. In the "long-run" the function of this bit-field is exactly the same as that of Bit 4 (Transmit AIS-P Down-stream – Upon SD), within the Receive STS-3 Transport – Auto AIS Control Register (Address Location= 0x1163). The only difference is that this register bit will cause each of the "downstream" Transmit STS-1 POH Processor blocks to IMMEDIATELY begin to transmit the AIS-P condition whenever the Receive STS-3 TOH Processor block declares the SD defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the NE declaring the LOS defect.
			2. In the case of Bit 1 (Transmit AIS-P Downstream – Upon LOF), several SONET frame periods are required (after the Receive STS-3 TOH Processor block has declared the SD defect), before the Transmit STS-1 POH Processor blocks will begin the process of transmitting the AIS-P indicators.
			3. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STS-1s Enable) within this register, in order enable this feature.
2	Transmit AIS-P (via Downstream STS-1s)	R/W	Transmit AIS-P (via Downstream STS-1s) upon Signal Failure (SF):
	upon SF	She	This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor blocks (in each channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3 TOH Processor block declares an SF condition.
		and	0 – Does not configures all "activated" Transmit STS-1 POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3 TOH Processor block declares the SF defect.
			1 – Configures all "activated" Transmit STS-1POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3 TOH Processor block declares the SF defect.
			1. In the "long-run" the function of this bit-field is exactly the same as that of Bit 5 (Transmit AIS-P Down-stream – Upon SF), within the Receive STS-3 Transport – Auto AIS Control Register (Address Location= 0x1163). The only difference is that this register bit will cause each of the "downstream" Transmit STS-1 POH Processor blocks to IMMEDIATELY begin transmit the AIS-P condition whenever the Receive STS-3 TOH Processor block declares the SF defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the

			NE declaring the SF defect.
			2. In the case of Bit 5 (Transmit AIS-P Downstream – Upon SF), several SONET frame periods are required (after the Receive STS-3 TOH Processor block has declared the SF defect), before the Transmit STS-1 POH Processor blocks will begin the process of transmitting the AIS-P indicators.
			3. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STS-1s Enable) within this register, in order enable this feature.
1	AIS-L Output Enable	R/W	AIS-L Output Enable:
			This READ/WRITE bit-field, along with Bits 7 (8kHz or STUFF Out Enable) within the "Operation Output Control Register – Byte 1" (Address Location= 0x0150) permit the user to configure the "AIS-L" indicator to be output via the "LOF" output pin (pin AD11).
			If Bit 7 (within the "Operation Output Control Register – Byte 1") is set to "0", then setting this bit-field to "1" configures pin AD11 to function as the AIS-L output indicator.
			If Bit 7 (within the "Operation Output Control Register – Byte 1") is set to "0", then setting this bit field to "0" configures pin AD11 to function as the LOF output indicator
			If Bit 7 (within the "Operation Output Control Register – Byte 1) is set to "1", then this register bit is ignored.
0	Transmit AIS-P (via Downstream STS-1s)	R/W	Automatic Transmission of AIS-P (via the downstream STS-1s) Enable:
	Enable		This READ/WRITE bit-field permits the user to configure all "activated" Transmit STS-1 POH Processor blocks to automatically transmit the AIS-P indicator, via its "outbound" STS-1 signals, upon detection of an SF, SD, LOS and LOF condition.
		i or	0 - Does not configure the "activated" Transmit STS-1 POH Processor blocks to automatically transmit the AIS-P indicator, whenever the Receive STS-3 TOH Processor block declares either the LOS, LOF, SD or SF defects.
	produ	300	Configures the "activated" Transmit STS-1 POH Processor blocks to automatically transmit the AIS-P indicator, whenever the Receive STS-3 TOH Processor block declares either the LOS, LOF, SD or SF defects.



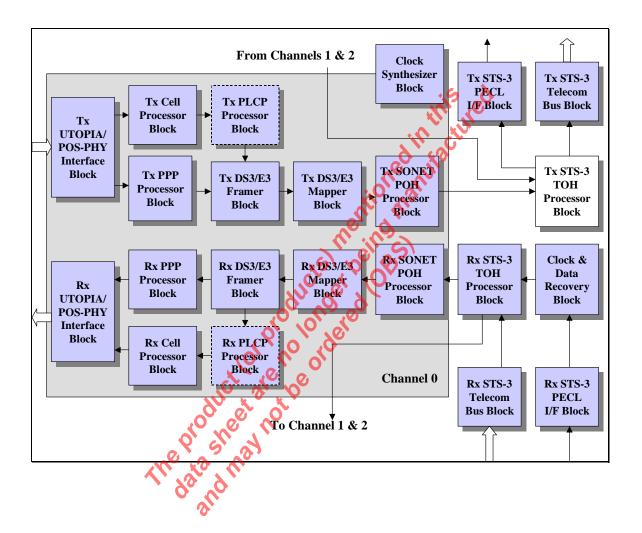
Rev 2.0.0

1.6 TRANSMIT STS-3 TOH PROCESSOR BLOCK

The register map for the Transmit STS-3 TOH Processor Block is presented in the Table below. Additionally, a detailed description of each of the "Transmit STS-3 TOH Processor" block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33, with the "Transmit STS-3 TOH Processor Block "highlighted" is presented below in Figure 7

Figure 7: Illustration of the Functional Block Diagram of the XRT94L33, with the Transmit STS-3 TOH Processor Block "High-lighted".





1.6.1 TRANSMIT STS-3 TOH PROCESSOR BLOCK REGISTER

Table 130: Transmit STS-3 TOH Processor Block Registers – Address Map

INDIVIDUAL REGISTER ADDRESS	Address Location	REGISTER NAME	DEFAULT VALUES
0x00, 0x01	0x1800 – 0x1901	Reserved	0x00
0x02	0x1902	Transmit STS-3 Transport – SONET Transmit Control Register – Byte 1	0x00
0x03	0x1903	Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0	0x00
0x04 – 0x15	0x1904 – 0x1915	Reserved	0x00
0x16	0x1916	Reserved	0x00
0x17	0x1917	Transmit STS-3 Transport – Transmit Al Byte Error Mask – Low Register – Byte 0	0x00
0x18 – 0x1D	0x1918 – 0x191D	Reserved	0x00
0x1E	0x191E	Reserved	0x00
0x1F	0x191F	Transmit STS-3 Transport - Transmit A2 Byte Error Mask - Low Register - Byte 0	0x00
0x20 - 0x22	0x1920 – 0x1921	Reserved	0x00
0x23	0x1923	Transmit STS-3 Transport – B1 Byte Error Mask Register	0x00
0x24, 0x25	0x1924 – 0x1925	Reserved @	0x00
0x26	0x1926	Reserved	0x00
0x27	0x1927	Transmit STS-3 Transport – Transmit B2 Byte Error Mask Register Byte 0	0x00
0x28 – 0x2A	0x1928 – 0x192A	Reserved	0x00
0x2B	0x192B	Transmit STS-3 Transport – Transmit B2 Byte - Bit Error Mask Register – Byte 0	0x00
0x2C, 0x2D	0x192C - 0x192D	Reserved	0x00
0x2E	0x192E	Transmit STS-3 Transport – K1K2 Byte (APS) Value Register – Byte 1	0x00
0x2F	0x192F	Transmit STS-3 Transport – K1K2 Byte (APS) Value Register – Byte 0	0x00
0x30 - 0x32	0x1930 – 0x1931	Reserved	0x00
0x33	0x1933	Transmit STS-3 Transport – RDI-L Control Register	0x00
0x34 - 0x36	0x1934 – 0x1936	Reserved	0x00

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

INDIVIDUAL REGISTER ADDRESS	Address Location	REGISTER NAME	DEFAULT VALUES
0x37	0x1937	Transmit STS-3 Transport – M1 Byte Value Register	0x00
0x38 - 0x3A	0x1938 – 0x193A	Reserved	0x00
0x3B	0x193B	Transmit STS-3 Transport – S1 Byte Value Register	0x00
0x3C - 0x3E	0x193C – 0x193E	Reserved	0x00
0x3F	0x193F	Transmit STS-3 Transport – F1 Byte Value Register	0x00
0x40 - 0x42	0x1940 – 0x1942	Reserved	0x00
0x43	0x1943	Transmit STS-3 Transport – E1 Byte Value Register	0x00
0x44	0x1944	Transmit STS-3 Transport – E2 Byte Control Register	0x00
0x45	0x1945	Reserved	0x00
0x46	0x1946	Transmit STS-3 Transport – E2 Byte Pointer Register	0x00
0x47	0x1947	Transmit STS-3 Transport – E2 Byte Value Register	0x00
0x48 – 0x4A	0x1948 – 0x194A	Reserved	0x00
0x4B	0x194B	Transmit STS-3 Transport - Transmit 10 Byte Value Register	0x00
0x4C - 0x4E	0x194C – 0x194E	Reserved	0x00
0x4F	0x194F	Transmit STS-3 Transport - Transmit J0 Byte Control Register	0x00
0x50 - 0x52	0x1950 – 0x1952	Reserved	0x00
0x53	0x1953	Transmit STS-3 Transport – Serial Port Control Register	0x00
0x54 – 0xFF	0x1954 – 0x19FF	Reserved	0x00
	In	Reserved C 100 100 100 100 100 100 100 100 100 1	

1.6.2 TRANSMIT STS-3 TOH PROCESSOR BLOCK REGISTER DESCRIPTION

Table 131: Transmit STS-3 Transport - SONET Transmit Control Register - Byte 1 (Address Location= 0x1902)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Reserved	STS-N Overhead Insert	E2 Insert Method	E1 Insert Method	F1 Insert Method	S1 Insert Method	K1K2 Insert Method	M0M1 Insert Method[1]
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Unused	R/O	in the till
6	STS-N Overhead	R/W	STS-N Overhead Insert (Revision C Silicon Only):
	Insert		This READ/WRITE bit-field permits the user to configure the TxTOH input port to inser the TOH for all lower-tributary STS-1s within the outbound STS-3 signal.
			0 - Disables this feature. In this mode, the TxTOH input port will only accept the TOH for the first STS-1 within the outbound STS-3 signal.
			1 - Enables this feature.
5	E2 Insert Method	R/W	E2 Byte Insert Method:
			This READ/WRITE bit-field permits the user to specify the source of the contents of the E2 byte, within the "transmit" output STS-3 data stream.
			0 – E2 Byte is obtained from "TxTOH" Serial Input Port.
	d	icit of	1 E2 Byte is obtained from the contents within the "Transmit STS-3 Transport – E2 Byte Value" register (Address Location= 0xN947). This selection provides the user with software control over the value of the "outbound" E2 byte.
4	E1 Insert Method	R/W	E1 Byte Insert Method:
	The ta	May	This READ/WRITE bit-field permits the user to specify the source of the contents of the E1 byte, within the "transmit" output STS-3 data stream.
	, 90 %	0	0 – E1 Byte is obtained from "TxTOH" Serial Input Port.
	♂		1 - E1 Byte is obtained from the contents within the "Transmit STS-3 Transport - E1 Byte Value" register (Address Location= 0xN943). This selection provides the user with software control over the value of the "outbound" E1 byte.
3	F1 Insert Method	R/W	F1 Byte Insert Method:
			This READ/WRITE bit-field permits the user to specify the source of the contents of the F1 byte, within the "transmit" output STS-3 data stream.
			0 – F1 Byte is obtained from "TxTOH" Serial Input Port.
			1 – F1 Byte is obtained from the contents within the "Transmit STS-3 Transport – F1 Byte Value" register (Address Location= 0xN93F). This selection provides the user with software control over the value of the "outbound" F1 byte.
2	S1 Insert Method	R/W	S1 Byte Insert Method:

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

				field permits the user to specify the source of the , within the "transmit" output STS-3 data stream.
			0 – S1 Byte is obtained	from "TxTOH" Serial Input Port.
			Transport - S1 Byte V	ed from the contents within the "Transmit STS-3 alue" register (Address Location= 0xN93B). This user with software control over the value of the
1	K1K2 Insert Method	R/W	K1K2 Byte Insert Metl	hod:
				field permits the user to specify the source of the K2 bytes, within the "transmit" output STS-3 data
			0 – K1 and K2 Bytes ar	e obtained from "TxTOH" Serial Input Port.
			STS-3 Transport – K1k = 0x192E) and the " register – Byte 2 (Add	re obtained from the contents within the "Transmit (2 Byte Value" register – Byte 1 (Address Location Transmit STS-3 Transport – K1K2 Byte Value" ress Location= 0x192F). This selection provides control over the value of the "outbound" K1 and K2
0	M0M1 Insert	R/W	M0M1 Insert Method -	- Bit 1:
	Method[1]		in the "Transmit STS-3 permit the user to spec	field, along with "M0M1 Insert Method[0]" (located 3 Transport – SONET Control Register – Byte 0") cify the source of the contents of the M0/M1 byte, but STS-3 data stream.
			The relationship betw source of the M0/M1 by	een these two bit-fields and the corresponding te is presented below.
			M0M1 Insert Method[1:0]	Source of M0/M1 Byte
		١	00 100 100	From corresponding STS-1 Receiver (B2 Error Count)
	4	oduci		Obtained from the contents of the "Transmit STS-3 Transport – M0/M1 Byte Value" register (Address Location= 0xN937).
	, ne 0	Sh.	0	M0/M1 byte is obtained from the "TxTOH" Serial Input Port.
	1,98	,49,	1 1	From corresponding STS-3 Receiver (B2 Error Count).

Table 132: Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
M0M1 Insert Method[0]	Unused	RDI-L Force	AIS-L Force	LOS Force	Scramble Enable	B2 Error Insert	A1A2 Error Insert
R/W	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE		DESCRIPTION		
7	M0M1 Insert Method[0]	R/W	MoM1 Insert Method – Bit 0: This READ/WRITE bit-field, along with "MoM1 Insert (located in the "Transmit STS-3 Transport – SONET Control Byte 1") permit the user to specify the source of the conte Mo/M1 byte, within the "transmit" output STS-3 data stream.			
			The relationship between these two bit-fields and the correspond source of the M0/M1 byte is presented below.			
			M0M1 Insert Source of M0/M1 Byte Method[1:0]			
			o moing	From corresponding STS-3 Receiver (B2 Fror Count)		
			oducis, b ob	Obtained from the contents of the "Transmit STS-3 Transport – M0/M1 Byte Value" register (Address Location= 0xN937).		
		lot	no orde o	M0/M1 byte is obtained from the "TxTOH" Serial Input Port.		
	N	it al	1 1	From corresponding STS-3 Receiver (B2 Error Count).		
6	Unused	R/O	9			
5	RDI-L Force	R/W	Transmit Line – Remo	te Defect Indicator:		
	Thedata	Mi	force the Transmit S	-field permits the user to (by software control) TS-3 TOH Processor block to generate and cator to the remote terminal equipment.		
	'		0 - Does not configure generate and transmit t	e the Transmit STS-3 TOH Processor block to he RDI-L indicator.		
			and transmit the RDI-L	ansmit STS-3 TOH Processor block to generate indicator. In this case, the STS-3 Transmitter (of the K2 byte) to the value "1, 1, 0".		
				s ignored if the Transmit STS-3 TOH Processor mitting the Line AIS (AIS-L) indicator or the LOS		
4	AIS-L Force	R/W	Transmit Line - AIS In	ndicator:		
			force the Transmit S	-field permits the user to (by software control) TS-3 TOH Processor block to generate and eator to the remote terminal equipment.		
			0 - Does not configure	e the Transmit STS-3 TOH Processor block to		

Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

1 - Configures the Transmit STS-3 TOH Processor block to generate and transmit the AIS-L indicator. In this case, the Transmit STS-3 Tame) with the exception of the Section Overhead Bytes to an "All Ones" pattern. Note: This bit-field is ignored if the Transmit STS-3 TOH Processor block is transmitting the LOS pattern. Note: This bit-field permits the user to (by software control) force the Transmit STS-3 TOH Processor block to transmit the LOS (Loss of Signal) pattern to the remote terminal equipment. 0 - Does not configure the Transmit STS-3 TOH Processor block to generate and transmit the LOS pattern. 1 - Configures the Transmit STS-3 TOH Processor block to generate and transmit the LOS pattern. 2 Scramble Enable RW Scramble Enable: This READ/WRITE bit-field permits the user to either enable or disable the Scramble; within the "Transmit STS-3 TOH Processor block circuitry on Disables the Scramble; the Scramble of the S				generate and transmit the AIS-L indicator.
Book is transmitting the LOS pattern.				1 – Configures the Transmit STS-3 TOH Processor block to generate and transmit the AIS-L indicator. In this case, the Transmit STS-3 TOH Processor block will force all bits (within the "outbound" STS-3 frame) with the exception of the Section Overhead Bytes to an "All Ones"
This READWRITE bit-field permits the user to (by software control) force the Transmit STS-3 TOH Processor block to transmit the LOS (Loss of Signal) pattern to the remote terminal equipment. 0 - Does not configure the Transmit STS-3 TOH Processor block to generate and transmit the LOS pattern. 1 - Configures the Transmit STS-3 TOH Processor block will force all bytes (within the "outbound" SONET frame) to an "All Zeros" pattern. 2 Scramble Enable R/W Scramble Enable: This READWRITE bit-field permits the user to either enable or disable the Scrambler, within the Transmit STS-3 TOH Processor block circuitry 0 - Disables the Scrambler, 1 - Enablestite Scrambler, 1 - Enablestite Scrambler, 2 Transmit B2 Byte Etror Insert Enable: This READWRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to insert errors into the "outbound" B2 bytes, per the oritents within the "Transmit STS-3 Transport - Transmit B2 Byte Etror Mask Registers" 0 Configures the Transmit STS-3 TOH Processor block to insert errors into the B2 bytes, within the outbound STS-3 signal. 1 Configures the Transmit STS-3 TOH Processor block to insert errors into the Mask Registers" 0 A1A2 Error lasert R/W Transmit A1 Byte Error Insert Enable: This READWRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to insert errors into the "outbound" A1 and A2 bytes, per the contents within the "Transmit STS-3 Transport - Transmit A1 Byte Error Insert Enable: This READWRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to insert errors into the "outbound" A1 and A2 bytes, per the contents within the "Transmit STS-3 Transport - Transmit A1 Byte Error Insert Bransmit STS-3 ToH Processor block to NOT insert errors into the A1 and A2 bytes (per the contents within the "Transmit Transmit STS-3 Transport - Transmit A1 Byte Error Bask" and Transmit STS-3 Transport - Transmit A1 Byte Error Bask Registers. 0 - Configures the Transmit STS-3 TOH Processor block to insert er				
force the Transmit STS-3 TOH Processor block to transmit the LOS (Loss of Signal) pattern to the remote terminal equipment. 0 - Does not configure the Transmit STS-3 TOH Processor block to generate and transmit the LOS pattern. 1 - Configures the Transmit STS-3 TOH Processor block will force all bytes (within the "outbound" SONET frame) to an "All Zeros" pattern. 2 Scramble Enable R/W Scramble Enable: This READ/WRITE bit-field permits the user to either enable or disable the Scrambler, within the Transmit STS-3 TOH Processor block circuitry 0 - Disables the Scrambler 1 B2 Error Insert R/W Transmit B2 Byte Error Insert Enable: This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block of insert errors into the "outbound" B2 bytes, per the contents within the "Transmit STS-3 Transport - Transmit B2 Byte Error Mask Registers" 0 - Configures the Transmit STS-3 TOH Processor block to insert errors into the B2 bytes (per the contents within the "Transmit B2 Byte Error Mask Registers") 0 A1A2 Error lasert R/W Transmit A1A2 Byte Error Insert Enable: This READ/WRITE bit-field permits the user to configure the Transmit B2 Byte Error Mask Registers") 1 Configures the Transmit STS-3 TOH Processor block to insert errors into the B2 bytes, within the outbound STS-3 signal. 1 Configures the Transmit STS-3 TOH Processor block to insert errors into the STS-3 TOH Processor block to insert errors into the STS-3 TOH Processor block to insert errors into the STS-3 Toh Processor block to NOT insert errors into the STS-3 Toh Processor block to NOT insert errors into the A1 and A2 bytes, within the outbound STS-3 datastream. 1 - Configures the Transmit STS-3 TOH Processor block to NOT insert errors into the A1 and A2 bytes, within the outbound STS-3 datastream. 1 - Configures the Transmit STS-3 TOH Processor block to insert errors into the A1 and A2 bytes, within the outbound STS-3 datastream.	3	LOS Force	R/W	Transmit LOS Pattern:
generate and transmit the LOS patter. 1 - Configures the Transmit STS-3 TOH Processor block to transmit the LOS pattern. In this case, the Transmit STS-3 TOH Processor block will force all bytes (within the "outbound" SONET frame) to an "All Zeros" pattern. 2 Scramble Enable R/W Scramble Enable: This READ/WRITE bit-field permits the user to either enable or disable the Scrambler, within the Transmit STS-3 TOH Processor block circuitry 0 - Disables the Scrambler. 1 Enables the Scrambler. 1 Enables the Scrambler. Transmit B2 Byte Error Insert Enable: This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to insert errors into the "outbound" B2 bytes, per the contents within the "Transmit STS-3 Transport - Transmit B2 Byte Error Mask Registers" 0 Configures the Transmit STS-3 TOH Processor block to insert errors into the B2 bytes, within the outbound STS-3 signal. 1 Configures the Transmit STS-3 TOH Processor block to insert errors into the B2 bytes (per the contents within the "Transmit B2 Byte Error Mask Registers") 0 A1A2 Error Insert R/W Transmit A1A2 Byte Error Insert Enable: This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to insert errors into the "outbound" A1 and A2 bytes, per the contents within the "Transmit A2 Byte Error Mask" Registers. 0 Configures the Transmit STS-3 TOH Processor block to NOT insert errors into the A1 and A2 bytes, within the outbound STS-3 datastream. 1 - Configures the Transmit STS-3 TOH Processor block to insert errors into the A1 and A2 bytes, within the outbound STS-3 datastream.				force the Transmit STS-3 TOH Processor block to transmit the LOS
LOS pattern. In this case, the Transmit STS-3 TOH Processor block will force all bytes (within the "outbound" SONET frame) to an "All Zeros" pattern. 2 Scramble Enable R/W Scramble Enable: This READ/WRITE bit-field permits the user to either enable or disable the Scrambler, within the Transmit STS-3 TOH Processor block circuitry 0 – Disables the Scrambler 1 B2 Error Insert R/W Transmit B2 Byte Error Insert Enable: This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to insert errors into the "outbound" B2 bytes, per the contents within the "Transmit STS-3 Transport – Transmit B2 Byte Error Mask Registers" 0 - Configures the Transmit STS-3 TOH Processor block to insert errors into the B2 bytes (per the contents within the "Transmit B2 Byte Error Mask Registers"). 7 Transmit A1A2 Byte Error Insert Enable: This READ/WRITE bit-field permits the user to configure the Transmit B2 Byte Error Mask Registers"). 8 Transmit A1A2 Byte Error Insert Enable: This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to insert errors into the "Outbound" A1 and A2 bytes, per the contents within the "Transmit STS-3 Transport – Transmit A1 Byte Error Mask" and Transmit A2 Byte Error Mask" Registers. 0 - Configures the Transmit STS-3 TOH Processor block to NOT insert errors into the A1 and A2 bytes, within the outbound STS-3 datastream. 1 - Configures the Transmit STS-3 TOH Processor block to insert errors into the A1 and A2 bytes, within the "Transmit errors into the A1 and A2 bytes, within the outbound STS-3 datastream.				
This READ/WRITE bit-field permits the user to either enable or disable the Scrambler, within the Transmit STS-3 TOH Processor block circuitry 0 - Disables the Scrambler 1 - Enables the Scramble the Institute the Transmit STS-3 Toh Processor block to insert errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the Enables the				LOS pattern. In this case, the Transmit STS-3 TOH Processor block will force all bytes (within the "outbound" SONET frame) to an "All
the Scrambler, within the Transmit STS-3 TOH Processor block circuitry 0 – Disables the Scrambler. 1 – Enables the Scrambler. 2 – Enables the Transmit STS-3 TOH Processor block to NOT insert errors into the B2 bytes, within the outbound STS-3 signal. 1 – Enables the Transmit STS-3 TOH Processor block to insert errors into the B2 bytes (per the contents within the "Transmit B2 Byte Error Mask Registers"). 2 – Enables the Transmit STS-3 TOH Processor block to insert errors into the "outbound" A1 and A2 bytes, per the contents within the "Transmit A1 Byte Error Mask" and Transmit A2 Byte Error Mask" Registers. 2 – Configures the Transmit STS-3 TOH Processor block to NOT insert errors into the A1 and A2 bytes, within the outbound STS-3 data-stream. 1 – Configures the Transmit STS-3 TOH Processor block to insert errors into the A1 and A2 bytes, (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (2	Scramble Enable	R/W	Scramble Enable:
1 B2 Error Insert R/W Transmit B2 Byte Error Insert Enable: This READ/WRITE bit-field permits the user to configure the Transmit ST\$-3 TOH Processor block to insert errors into the "outbound" B2 bytes, per the contents within the "Transmit STS-3 Transport – Transmit B2 Byte Error Mask Registers" 0 Configures the Transmit STS-3 TOH Processor block to NOT insert errors into the B2 bytes (per the contents within the "Transmit B2 Byte Error Mask Registers"). 0 A1A2 Error Insert R/W Transmit A1A2 Byte Error Insert Enable: This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to insert errors into the "STS-3 TOH Processor block to insert errors into the "Transmit A1 Byte Error Mask" and Transmit STS-3 Transport – Transmit A1 Byte Error Mask" and Transmit A2 Byte Error Mask" Registers. 0 - Configures the Transmit STS-3 TOH Processor block to NOT insert errors into the A1 and A2 bytes, within the outbound STS-3 datastream. 1 - Configures the Transmit STS-3 TOH Processor block to insert errors into the A1 and A2 bytes, per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors i				This READ/WRITE bit-field permits the user to either enable or disable the Scrambler, within the Transmit STS-3 TOH Processor block circuitry
Transmit B2 Byte Error Insert Enable: This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to insert errors into the "outbound" B2 bytes, per the contents within the "Transmit STS-3 Transport – Transmit B2 Byte Error Mask Registers" 0 Configures the Transmit STS-3 TOH Processor block to NOT insert errors into the B2 bytes, within the outbound STS-3 signal. 1 Configures the Transmit STS-3 TOH Processor block to insert errors into the B2 bytes (per the contents within the "Transmit B2 Byte Error Mask Registers"). 7 Transmit A1A2 Byte Error Insert Enable: This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to insert errors into the "outbound" A1 and A2 bytes, per the contents within the "Transmit A2 Byte Error Mask" Registers. 0 Configures the Transmit STS-3 TOH Processor block to NOT insert errors into the A1 and A2 bytes, within the outbound STS-3 datastream. 1 Configures the Transmit STS-3 TOH Processor block to insert errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 b				0 – Disables the Scrambler.
This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to insert errors into the "outbound" B2 bytes, per the contents within the "Transmit STS-3 Transport – Transmit B2 Byte Error Mask Registers" 0 - Configures the Transmit STS-3 TOH Processor block to NOT insert errors into the B2 bytes, within the outbound STS-3 signal. 1 - Configures the Transmit STS-3 TOH Processor block to insert errors into the B2 bytes (per the contents within the "Transmit B2 Byte Error Mask Registers"). R/W Transmit A1A2 Byte Error Insert Enable: This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to insert errors into the "outbound" A1 and A2 bytes, per the contents within the "Transmit STS-3 Transport – Transmit A1 Byte Error Mask" and Transmit A2 Byte Error Mask" Registers. 0 - Configures the Transmit STS-3 TOH Processor block to NOT insert errors into the A1 and A2 bytes, within the outbound STS-3 datastream. 1 - Configures the Transmit STS-3 TOH Processor block to insert errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents and contents and				1 – Enables the Scrambler.
ST\$-3 TOH Processor block to insert errors into the "outbound" B2 bytes, per the contents within the "Transmit STS-3 Transport – Transmit B2 Byte Error Mask Registers" 0, € Configures the Transmit STS-3 TOH Processor block to NOT insert errors into the B2 bytes, within the outbound STS-3 signal. 1 ← Configures the Transmit STS-3 TOH Processor block to insert errors into the B2 bytes (per the contents within the "Transmit B2 Byte Error Mask Registers"). R/W Transmit A1A2 Byte Error Insert Enable: This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to insert errors into the "outbound" A1 and A2 bytes, per the contents within the "Transmit STS-3 Transport – Transmit A1 Byte Error Mask" and Transmit A2 Byte Error Mask" Registers. 0 – Configures the Transmit STS-3 TOH Processor block to NOT insert errors into the A1 and A2 bytes, within the outbound STS-3 datastream. 1 – Configures the Transmit STS-3 TOH Processor block to insert errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A1 and A2 bytes (per the contents within the "Transmit errors into the A2 bytes (per the contents within the "Transmit errors into the A2 bytes (per the contents within the "Transmit errors into the A3 and A2 bytes (per the contents within the "Transmit errors into the A3 and A2 bytes (per the contents within the "Transmit errors into the A3 and A2 bytes (per the contents within the "Transmit error	1	B2 Error Insert	R/W	Transmit B2 Byte Error Insert Enable:
errors into the B2 bytes, within the outbound STS-3 signal. 1 Configures the Transmit STS-3 TOH Processor block to insert errors into the B2 bytes (per the contents within the "Transmit B2 Byte Error Mask Registers"). R/W Transmit A1A2 Byte Error Insert Enable: This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to insert errors into the "outbound" A1 and A2 bytes, per the contents within the "Transmit STS-3 Transport – Transmit A1 Byte Error Mask" and Transmit A2 Byte Error Mask" Registers. 0 – Configures the Transmit STS-3 TOH Processor block to NOT insert errors into the A1 and A2 bytes, within the outbound STS-3 data-stream. 1 – Configures the Transmit STS-3 TOH Processor block to insert errors into the A1 and A2 bytes (per the contents within the "Transmit").			. (STS-3 TOH Processor block to insert errors into the "outbound" B2 bytes, per the contents within the "Transmit STS-3 Transport – Transmit
errors into the B2 bytes (per the contents within the "Transmit B2 Byte Error Mask Registers"). 7			, ct	
This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to insert errors into the "outbound" A1 and A2 bytes, per the contents within the "Transmit STS-3 Transport – Transmit A1 Byte Error Mask" and Transmit A2 Byte Error Mask" Registers. 0 – Configures the Transmit STS-3 TOH Processor block to NOT insert errors into the A1 and A2 bytes, within the outbound STS-3 datastream. 1 – Configures the Transmit STS-3 TOH Processor block to insert errors into the A1 and A2 bytes (per the contents within the "Transmit").		or or	direct	errors into the B2 bytes (per the contents within the "Transmit B2 Byte
STS-3 TOH Processor block to insert errors into the "outbound" A1 and A2 bytes, per the contents within the "Transmit STS-3 Transport – Transmit A1 Byte Error Mask" and Transmit A2 Byte Error Mask" Registers. 0 – Configures the Transmit STS-3 TOH Processor block to NOT insert errors into the A1 and A2 bytes, within the outbound STS-3 data-stream. 1 – Configures the Transmit STS-3 TOH Processor block to insert errors into the A1 and A2 bytes (per the contents within the "Transmit")	0	A1A2 Error Insert	R/W	Transmit A1A2 Byte Error Insert Enable:
errors into the A1 and A2 bytes, within the outbound STS-3 data- stream. 1 - Configures the Transmit STS-3 TOH Processor block to insert errors into the A1 and A2 bytes (per the contents within the "Transmit		7,98	and.	STS-3 TOH Processor block to insert errors into the "outbound" A1 and A2 bytes, per the contents within the "Transmit STS-3 Transport – Transmit A1 Byte Error Mask" and Transmit A2 Byte Error Mask"
errors into the A1 and A2 bytes (per the contents within the "Transmit				errors into the A1 and A2 bytes, within the outbound STS-3 data-
				errors into the A1 and A2 bytes (per the contents within the "Transmit

Table 133: Transmit STS-3 Transport – Transmit A1 Error Mask – Low Register – Byte 0 (Address Location= 0x1917)

BIT 7 BIT 6 BIT 5 BIT 4	Віт 3 Віт 2	Віт 1 Віт 0
-------------------------	-------------	-------------

		Unused	A1 Error in STS-1 Channel 2	A1 Error in STS-1 Channel 1	A1 Error in STS-1 Channel 0		
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7-3	Unused	R/O	
2	A1 Error in STS-1	R/W	A1 Error in STS-1 Channel # 2:
	Channel # 2		This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to transmit an erred A1 byte, within STS-1 Channel 2. 0 — Configures the Transmit STS-3 TOH Processor block to NOT transmit an erred A1 byte, within STS-1 Channel 2.
			1 – Configures the Transmit STS-3 TOH Processor block to transmit an erred A1 byte, within STS-1 Channel 2.
			Note: This bit-field is only valid if Bit 0 (A1A2 Error Insert), within the "Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".
1	A1 Error in STS-1	R/W	A1 Error in STS-1 Channel # 1:
	Channel # 1		This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to transmit an erred A1 byte, within STS-1 Channel 1.
		~	0 - Configures the Transmit STS-3 TOH Processor block to NOT transmit an erred A1 byte, within STS-1 Channel 1.
		IOIP	1 Configures the Transmit STS-3 TOH Processor block to transmit an erred A1 byte, within STS-1 Channel 1.
	di	ct are	Note: This bit-field is only valid if Bit 0 (A1A2 Error Insert), within the "Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".
0	A1 Error in STS-1	R/W	A1 Error in STS-1 Channel # 0:
	Channel #0	May	This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to transmit an erred A1 byte, within STS-1 Channel 0.
	all		0 - Configures the Transmit STS-3 TOH Processor block to NOT transmit an erred A1 byte, within STS-1 Channel 0.
			1 – Configures the Transmit STS-3 TOH Processor block to transmit an erred A1 byte, within STS-1 Channel 0.
			Note: This bit-field is only valid if Bit 0 (A1A2 Error Insert), within the "Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".

Table 134: Transmit STS-3 Transport - Transmit A2 Error Mask - Low Register - Byte 0 (Address Location= 0x191F)

BIT 7 BIT 6 BIT 5 BIT 4 BIT 3 BIT 2 BIT 1	Віт 0
---	-------



		Unused	A2 Error in STS-1 Channel 2	A2 Error in STS-1 Channel 1	A2 Error in STS-1 Channel 0		
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7-3	Unused	R/O	
2	A2 Error in STS-1 Channel # 2	R/W	A2 Error in STS-1 Channel # 2: This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to transmit an erred A2 byte, within STS-1 Channel 2. 0 – Configures the Transmit STS-3 TOH Processor block to NOT transmit an erred A2 byte, within STS-1 Channel 2. 1 – Configures the Transmit STS-3 TOH Processor block to transmit an erred A2 byte, within STS-1 Channel 2. Note: This bit-field is only valid if Bit 0 (A1A2 Error Insert), within the "Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".
1	A2 Error in STS-1 Channel # 1	R/W	A2 Error in STS-1 Channel # 1: This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to transmit an erred A2 byte, within STS-1 Channel 1. 0 – Configures the Transmit STS-3 TOH Processor block to NOT transmit an erred A2 byte, within STS-1 Channel 1. 1 – Configures the Transmit STS-3 TOH Processor block to transmit an erred A2 byte, within STS-1 Channel 1. Note: This bit-field is only valid if Bit 0 (A1A2 Error Insert), within the "Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".
0	A2 Error in STS-1 Channel # 0	RMO	Az Error in STS-1 Channel # 0: This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to transmit an erred A2 byte, within STS-1 Channel 0. Configures the Transmit STS-3 TOH Processor block to NOT transmit an erred A2 byte, within STS-1 Channel 0. 1 – Configures the Transmit STS-3 TOH Processor block to transmit an erred A2 byte, within STS-1 Channel 0. Note: This bit-field is only valid if Bit 0 (A1A2 Error Insert), within the "Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 135: Transmit STS-3 Transport - B1 Byte Error Mask Register (Address Location= 0x1923)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	B1_Byte_Error_Mask[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	B1_Byte_Error_Mask [7:0]	R/W	B1 Byte Error Mask[7:0]:
			These READ/WRITE bit-fields permit the user to insert bit errors into the B1 bytes, within the outbound STS-3 data stream.
			The Transmit STS-3 TOH Processor block will perform an XOR operation with the contents of the B1 byte, and this register. The results of this calculation will be inserted into the B1 byte position within the "outbound" STS-3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the B1 byte will be in error. Note: For normal operation, the user should set this register to 0x00.

Table 136: Transmit STS-3 Transport – Transmit B2 Byte Error Mask Register – Byte 0 (Address Location= 0x1927)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 2	Віт 1	Віт 0
		Unused	or proclonderect	B2 Error in STS-1 Channel 2	B2 Error in STS-1 Channel 1	B2 Error in STS-1 Channel 0
R/O	R/O	R/O	R/O R/O	R/W	R/W	R/W
0	0	0 6	0 0	0	0	0

	<u>, O,</u>	· · · ·	
BIT NUMBER	NAME NAME	TYPE	DESCRIPTION
7-3	Unused	R/O	
2	B2 Error in STS-1 Channel # 2	R/W	B2 Byte Error in STS-1 Channel # 2: This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to transmit an erred B2 byte, within STS-1 Channel 2.
			If the user enables this feature, then the Transmit STS-3 TOH Processor block will perform an XOR operation of the contents of the B2 byte (within STS-1 Channel 2) and the contents of the "Transmit STS-3 Transport – Transmit B2 Bit Error Mask Register – Byte 0 (Address Location= 0x192B). The results of this calculation will be written back into the "B2 byte" position, within STS-1 Channel 2, prior to transmission to the remote terminal.
			0 – Configures the Transmit STS-3 TOH Processor block to NOT insert errors into the B2 byte, within STS-1 Channel 2.
			1 – Configures the Transmit STS-3 TOH Processor block to insert errors into the B2 byte, within STS-1 Channel 2.
			Note: This bit-field is only valid if Bit 1 (B2 Error Insert), within the

			"Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0 (Address = 0x1903) to "1".
1			B2 Byte Error in STS-1 Channel # 1:
	Channel # 1		This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to transmit an erred B2 byte, within STS-1 Channel 1.
			If the user enables this feature, then the Transmit STS-3 TOH Processor block will perform an XOR operation of the contents of the B2 byte (within STS-1 Channel 1) and the contents of the "Transmit STS-3 Transport – Transmit B2 Bit Error Mask Register – Byte 0 (Address Location= 0x192B). The results of this calculation will be written back into the "B2 byte" position, within STS-1 Channel 1, prior to transmission to the remote terminal.
			0 – Configures the Transmit STS-3 TOH Processor block to NOT insert errors into the B2 byte, within STS-1 Channel 1.
			1 – Configures the Transmit STS-3 TOH Processor block to insert errors into the B2 byte, within STS-1 Channel 1.
			Note: This bit-field is only valid if Bit 1 (B2 Error Insert), within the "Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".
0	B2 Error in STS-1	R/W	B2 Byte Error in STS-1 Channel # 0:
	Channel # 0		This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to transmit an erred B2 byte, within STS-1 Channel 0.
			If the user enables this feature, then the Transmit STS-3 TOH Processor block will perform an XOR operation of the contents of the B2 byte (within STS-1 Channel 0) and the contents of the "Transmit STS-3 Transport Transmit B2 Bit Error Mask Register – Byte 0 (Address Location= 0x192B). The results of this calculation will be written back into the "B2 byte" position, within STS-1 Channel 0, prior to transmission to the remote terminal.
		HICK	O Configures the Transmit STS-3 TOH Processor block to NOT insert errors into the B2 byte, within STS-1 Channel 0.
		locker	1 Configures the Transmit STS-3 TOH Processor block to insert errors into the B2 byte, within STS-1 Channel 0.
	The	ioduce ioduce	Note: This bit-field is only valid if Bit 1 (B2 Error Insert), within the "Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".

Table 137: Transmit STS-3 Transport – Transmit B2 Bit Error Mask Register – Byte 0 (Address Location= 0x192B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Transmit_B2_Error_Mask[7:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT Number	Name	Түре	DESCRIPTION
7 – 0	Transmit_B2_Error_Mask[7:0]	R/W	Transmit B2 Error Mask Byte:
			These READ/WRITE bit-fields permit the user to specify exact which bits, within the "selected" B2 byte (within the outbound STS-3 signal) will be erred.
		du	If the user configures the Transmit STS-3 TOH Processor block to transmit one or more erred B2 bytes, then the Transmit STS-3 TOH Processor block will perform an XOR operation of the contents of the B2 byte (within the "selected" STS-1 Channel) and the contents of this register. The results of this calculation will be written back into the "B2 byte" position within the "selected" STS-1 Channel, prior to transmission to the remote terminal. The user can select which STS-1 channels (within the outbound STS-3 signal) will contain the "erred" B2 byte, by writing the appropriate data into the "Transmit STS-3 Transport – Transmit B2 Byte Error Mask Register – Bytes 1 and 0 (Address Location = 0x1927).
	, los	or or	Note: This bit-field is only valid if Bit 1 (B2 Error Insert), within the "Transmit STS-3 Transport – SONET Transmit Control Register – Byte 0 (Address Location= 0x1903) to "1".
	The product of and may	notbe	

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 138: Transmit STS-3 Transport - K1K2 (APS) Value Register - Byte 1 (Address Location= 0x192E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit_K2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit_K2_Byte_Value[7:0]	R/W	Transmit K2 Byte Value:
			If the appropriate "K1K2 Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the K2 byte, within the "outbound" STS-3 signal. If Bit 1 (K1K2 Insert Method) within the Transmit STS-3 Transport – SONET Transmit Control Register – Byte 1 (Address Location = 0x1902) is set to "1", then the Transmit STS-3 TOH Processor block will load the contents of this register into the "K2" byte-field, within each outbound STS-3 frame. Note: These register bits are ignored if Bit 1 (K1K2 Insert Method) is set to "0".

Table 139: Transmit STS-3 Transport - K1K2 (APS) Value Register - Byte 0 (Address Location= 0x192F)

Віт 7	Віт 6	Віт 5	В(т 4	Вп 3	Віт 2	Віт 1	Віт 0	
	Transmit_K1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	1800	0	0	0	0	

BIT Number	NAME TYPE	DESCRIPTION
7 – 0	Transmit_K1_Byte_Value[7:0] R/W	Transmit K1 Byte Value:
	diand	If the appropriate "K1K2 Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the K1 byte, within the "outbound" STS-3 signal.
		If Bit 1 (K1K2 Insert Method) within the Transmit STS-3 Transport – SONET Transmit Control Register – Byte 1 (Address Location= 0x1902) is set to "1", then the Transmit STS-3 TOH Processor block will load the contents of this register into the "K1" byte-field, within each outbound STS-3 frame.
		Note: These register bits are ignored if Bit 1 (K1K2 Insert Method) is set to "0".

Table 140: Transmit STS-3 Transport – RDI-L Control Register (Address Location= 0x1933)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused				External RDI- L Enable	Transmit RDI-L upon AIS-L	Transmit RDI- L upon LOF	Transmit RDI- L upon LOS
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 4	Unused	R/O	
3	External RDI-L Enable	R/W	External RDI-L Insertion Enable:
			This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor to accept data via the "TxTOH" input pin, when transmitting the RDI-L indicator to the remote terminal equipment.
			0 - Configures the Transmit STS-3 TOH Processor block to internally generate the RDI-L indicator, when appropriate.
			1 - Configure the Transmit STS-3 TOH Processor block accept data via the "TxTOH" input pin, when transmitting the RDI-L indicator:
2	Transmit RDI-L upon AIS-L	R/W	Transmit Line Remote Defect Indicator (RDI-L) upon Detection of AIS-L:
	(০)	produ	This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to automatically transmit a RDI-L indicator to the remote terminal anytime (and for the duration) that the corresponding Receive STS-3 TOH Processor is declaring the Line AIS (AIS-L) defect condition.
	Transmit RDI-L upon LOF	not be	0 – Configures the Transmit STS-3 TOH Processor block to NOT automatically transmit the RDI-L indicator, whenever (and for the duration that) the corresponding Receive STS-3 TOH Processor block is declaring the AIS-L defect condition.
	The Prash nay		1 – Configures the Transmit STS-3 TOH Processor block to automatically transmit the RDI-L indicator, whenever (and for the duration that) the corresponding Receive STS-3 TOH Processor block declares the AIS-L defect condition.
1	Transmit RDI-L upon LOF	R/W	Transmit Line Remote Defect Indicator (RDI-L) upon Detection of LOF:
			This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to automatically transmit a RDI-L indicator to the remote terminal anytime (and for the duration) that the corresponding Receive STS-3 TOH Processor block is declaring the LOF defect.
			0 – Configures the Transmit STS-3 TOH Processor to NOT automatically transmit the RDI-L indicator, whenever the corresponding Receive STS-3 TOH Processor block declares the LOF defect.
			1 – Configures the Transmit STS-3 TOH Processor block to automatically transmit the RDI-L indicator, whenever (and for the duration that) the corresponding Receive STS-3 TOH Processor block declares the LOF defect.

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

	T		1
0	Transmit RDI-L upon LOS	R/W	Transmit Line Remote Defect Indicator (RDI-L) upon Detection of LOS:
			This READ/WRITE bit-field permits the user to configure the Transmit STS-3 TOH Processor block to automatically transmit the RDI-L indicator to the remote terminal anytime (and for the duration) that the corresponding Receive STS-3 TOH Processor block is declaring the LOS defect.
			0 – Configures the Transmit STS-3 TOH Processor block to NOT automatically transmit the RDI-L indicator, whenever the corresponding Receive STS-3 TOH Processor block declares the LOS defect.
			1 – Configures the Transmit STS-3 TOH Processor block to automatically transmit the RDI-L indicator, whenever (and for the duration that) the corresponding Receive STS-3 TOH Processor block declares the LOS defect.
	The product	orpries	duration that) the corresponding Receive STS-3 TOH Processor block declares the LOS defect.

Table 141: Transmit STS-3 Transport - M0M1 Byte Value Register (Address Location= 0x1937)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Transmit_M0M1_Byte_Value[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	NAME Transmit_M0M1_Byte_Value [7:0]	TYPE R/W	Transmit M0M1 Byte Value: If the appropriate "M0M1 Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the M0M1 byte, within the "outbound" STS-3 signal. If Bit 0 (M0M1 Insert Method – Bit 1) within the Transmit STS-3 Transport – SONET Transmit Control Register – Byte 1 (Address Location= 0x1902) and Bit 7 (M0M1 Insert Method –
			Bit 0) within the Transmit STS-3 Transport – SONET Transmit Control Register—Byte 0 (Address Location=0x1903) is set to "0, 1", then the Transmit STS-3 TOH Processor block will load the contents of this register into the "M0M1" byte-field, within each outbound STS-3 frame. Note: These register bits are ignored if the M0M1 Insert Method[1:0] bits are set to any value other than "0, 1"

Table 142: Transmit STS-3 Transport – S1 Byte Value Register (Address Location= 0x193B)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit_S1_Byte_Value[7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION
7-0	Transmit_S1_Byte_Value[7:0]	R/W	Transmit S1 Byte Value: If the appropriate "S1 Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the S1 byte, within the "outbound" STS-3 signal. If Bit 2 (S1 Insert Method) within the Transmit STS-3 Transport – SONET Transmit Control Register – Byte 1 (Address Location= 0x1902) is set to "1", then the Transmit STS-3 TOH Processor block will load the contents of this register into the "S1" byte-field, within each outbound STS-3 frame. Note: These register bits are ignored if Bit 2 (S1 Insert Method) is set to "0".

EXAR

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 143: Transmit STS-3 Transport – F1 Byte Value Register (Address Location= 0x193F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Transmit_F1_Byte_Value[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit_F1_Byte_Value[7:0]	R/W	Transmit F1 Byte Value:
			If the appropriate "F1 Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the F1 byte, within the "outbound" STS-3 signal. If Bit 3 (F1 Insert Method) within the Transmit STS-3 Transport – SONET Transmit Control Register – Byte 1 (Address Location= 0x1902) is set to "1", then the Transmit STS-3 TOH Processor block will load the contents of this register into the "F1" byte-field, within each outbound STS-3 frame. Note: These register bits are ignored if Bit 3 (F1 Insert Method) is set to "0".

Table 144: Transmit STS-3 Transport – E1 Byte Value Register (Address Location= 0x1943)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 2	Віт 1	Віт 0	
Transmit_E1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W R/W	R/W	R/W	R/W	
0	0	0	0 0 0	0	0	0	

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Transmit_E1_Byte_Value[7:0]	R/W	Transmit E1 Byte Value:
	the proshe	124/10	If the appropriate "E1 Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the E1 byte, within the "outbound" STS-3 signal.
	Ti datind		If Bit 4 (E1 Insert Method) within the Transmit STS-3 Transport – SONET Transmit Control Register – Byte 1 (Address Location= 0x1902) is set to "1", then the Transmit STS-3 TOH Processor block will load the contents of this register into the "E1" byte-field, within each outbound STS-3 frame.
			Note: These register bits are ignored if Bit 4 (E1 Insert Method) is set to "0".

Table 145: Transmit STS-3 Transport – E2 Byte Control Register (Address Location= 0x1944)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Enable All STS-1s				Unused			
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7	Enable All STS-1s	R/W	Enable All STS-1s:
			This READ/WRITE bit-field permits the user to implement either of the following configurations options for software control of the E2 byte value, within the outbound STS-3 signal.
			0 – Configures the Transmit STS-3 TOH Processor block to read out the contents o the "Transmit STS-3 Transport – E2 Byte Value" register and load that value into the E2 byte (within STS-1 # 1) within the outbound STS-3 signal.
			1 – Configures the Transmit STS-3 TOH Processor block to read out the contents of the 3 "shadow" registers, and to load these values into the E2 byte positions, within each corresponding STS-1 signal; within the outbound STS-3 signal.
			Note: This register bit is ignored if Bit 5 (E2 Insert Method) within the "Transmit STS-3 Transport – SONET Transmit Control Register – Byte 1" (Address Location= 0x1902) is set to "0".
6 - 0	Unused	R/O	ad ad ad
	Thepro	duct of sheat	Pyte 1" (Address Location= 0x1902) is set to "0".

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 146: Transmit STS-3 Transport – E2 Pointer Register (Address Location= 0x1946)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused						nter[1:0]
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

NAME	Түре	DESCRIPTION
Unused	R/O	
E2_Pointer[1:0]	R/W	E2 Pointer[3:0]:
		These READ/WRITE bit-fields permit the user to uniquely identify one of the 3 STS-1 E2 byte "shadow" registers, when performing read or write operations to these registers.
		If the user has set Bit 7 (Enable All STS-1s), within this register to "1", then the contents of these four register bits, act as a pointer to a given "shadow" register. Once the user specifies this pointer value; then he/she completes the read or write operation (to or from the "shadow" register) by performing a read or write to the "Transmit STS-3 Transport – E2 Byte Value" register (Address Location= 0x1947).
		Valid "shadow" pointer values range from "0x00" to "0x02" (where the pointer value of "0x00" corresponds to the E2 "shadow" register, corresponding to STS-1 # 1; and so on).
		Note: This register bit is ignored if Bit 7 (Enable All STS-1s) is set to "1"; or if Bit 5 (E2 Insert Method) within the "Transmit STS-3 Transport - SONET Transmit Control Register - Byte 1" (Address Location= 0x1902) is set to "0".
the	ata dict	et are no ore
	Unused E2_Pointer[1:0]	Unused R/O

Table 147: Transmit STS-3 Transport – E2 Byte Value Register (Address Location=0x1947)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Transmit_E2_Byte_Value[7:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit_E2_Byte_Value[7:0]	R/W	Transmit E2 Byte Value:
			The exact function of these register bits depends upon whether Bit 7 (Enable All STS-1s) within the "Transmit STS-3 Transport – E2 Byte Control" Register (Address Location= 0x1944) has been set to "0" or "1"; as described below.
			If "Enable All STS-1s" is set to "0"
			If the appropriate "E2 Insert Method" is selected, then these READ/WRITE bit-fields will permit the user to specify the contents of the E2 byte, within the "outbound" STS-3 signal. More specifically, this value will be loaded into the E2 byte position, within STS-1 # 1 (within the outbound STS-3 signal).
		د بر	If Bit-5 (E2 Insert Method) within the Transmit STS-3 Transport – SONET Transmit Control Register – Byte 1 (Address Location= 0x1902) is set to "1", then the Transmit STS-3 TOH Processor block will load the contents of this register into the "E2" byte-field, within each outbound STS-3 frame.
		All	Enable All STS-1s" is set to "1"
		1000	In this mode, these register bit permit the user to have direct READ/WRITE access of the "STS-1 E2 Byte shadow" register; that is being pointed at by the "E2 Pointer[1:0]" value.
	ict of	100	These register bits are ignored if Bit 5 (E2 Insert Method) is set to "0".
	The product of and may no	o ^t	

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 148: Transmit STS-3 Transport – J0 Byte Value Register (Address Location= 0x194B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit_J0_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit_J0_Value[7:0]	R/W	Transmit J0 Value Byte:
			These READ/WRITE bits permit a user to specify the value of the J0 byte, that will be transmitted via the Transport Overhead, within the very next STS-3 Frame.
			Note: This register is only valid if the Transmit STS-3 TOH Processor block is configured to read out the contents
			from this register and insert it into the J0 byte-field within each outbound ST\$ 3 frame. The user accomplishes
			this by setting Bits 1 and 0 (J0_TYPE), within the
			Transmit STS-3 Transport – J0 Byte Control Register (Address Location= 0x194F) to "1, 0".
	The data	sheet are	(Address Location= 0x194F) to "1, 0".

Table 149: Transmit STS-3 Transport – Transmitter J0 Control Register (Address Location= 0x194F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unu	sed		MSG_L	ENGTH	J0_T	YPE
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	1	1	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 4	Unused	R/O	
3 – 2	MSG_LENGTH[1:0]	R/W	Message Length[1:0]:
			These two READ/WRITE bit-fields permit the user to specify the length of the message that is to be repetitively transmitted via the J0 byte, as depicted below.
			MSG_LENGTH[1:0] Corresponding Message Length (Bytes)
			00 Byte
			01 Bytes
			10 or 11 64 Bytes
1 – 0	J0_TYPE[1:0]	R/W	Transmit J0 Source[1:0]:
			These two READ/WRITE bit-fields permit the user to specify the source of the message that will be transported via the J0 byte/message, within the outbound STS-3 data-stream, as depicted below.
			J0_TXPE[1:0] Corresponding Source of J0 Byte/Message.
		lor	Automatically set the J0 Byte, in each "outbound" STS-3 frame to "0x01".
		CV o	The "Transmit Section Trace Message Buffer".
	prod	neet	The "Transmit STS-3 Trace Buffer" Memory is located at Address Location 0x1B00 through 0x1B3F.
	No xo	Wo.	10 From the "Transmit J0 Value[7:0]" Register.
	The prod	6	In this setting, the Transmit STS-3 TOH Processor block will read out the contents of the "Transmit J0 Value[7:0]" Register (Address Location= 0x194B), and will insert this value into the J0 byte of each outbound STS-3 frame.
			11 From the "TxTOH" Input pin (pin F8).

EXARExperience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 150: Transmit STS-3 Transport – Serial Port Control Register (Address Location= 0x1953)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused				TxTOH_CLOCK_SPEED[7:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

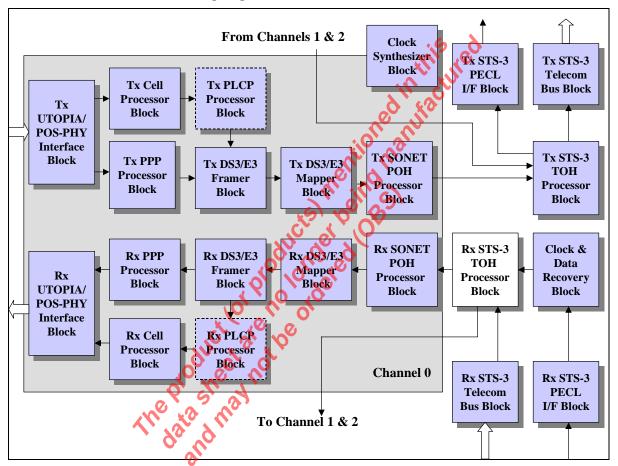
BIT NUMBER	Name	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3 - 0	TxTOH_CLOCK_SPEED[7:0]	R/W	TxTOHClk Output Clock Signal Speed:
			These READ/WRITE bit-fields permits the user to specify the frequency of the "TxTOHCIk output clock signal. The formula that relates the contents of these register bits to the "TxTOHCIk" frequency is presented below.
			FREQ = 19.44 /[2 *(TxTOH_CLOCK_SPEED + 1)
			Note: For STS-3/STM-1 applications, the frequency of the
	The product	orprot	TXTOHCIIk output signal must be in the range of 0.6075MHz to 9.72MHz

1.7 REDUNDANT RECEIVE STS-3 TOH PROCESSOR BLOCK

The register map for the Redundant Receive STS-3 TOH Processor Block is presented in the Table below. Additionally, a detailed description of each of the "Redundant Receive STS-3 TOH Processor" Block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33, with the "Redundant Receive STS-3 TOH Processor Block "highlighted" is presented below in Figure 6

Figure 8: Illustration of the Functional Block Diagram of the XRT94L33, with the Redundant Receive STS-3 TOH Processor Block "High-lighted".





1.7.1 REDUNDANT RECEIVE STS-3 TOH PROCESSOR BLOCK REGISTER

Table 151: Redundant Receive STS-3 TOH Processor Block Control Register – Address Map

INDIVIDUAL REGISTER ADDRESS	Address Location	REGISTER NAME	DEFAULT VALUES
0x00 - 0x02	0x1600 - 0x1702	Reserved	
0x03	0x1703	Redundant Receive STS-3 Transport Control Register – Byte 0	0x00
0x04 - 0x05	0x1704 - 0x1705	Reserved	0x00
0x06	0x1706	Redundant Receive STS-3 Transport Status Register – Byte 1	0x00
0x07	0x1707	Redundant Receive STS-3 Transport Status Register – Byte 0	0x02
0x08	0x1708	Reserved	0x00
0x09	0x1709	Redundant Receive STS-3 Transport Interrupt Status Register – Byte 2	0x00
0x0A	0x170A	Redundant Receive STS-3 Transport Interrupt Status Register – Byte 1	0x00
0x0B	0x170B	Redundant Receive STS-3 Transport Interrupt Status Register – Byte 0	0x00
0x0C	0x170C	Reserved	0x00
0x0D	0x170D	Redundant Receive STS-3 Transport Interrupt Enable Register – Byte 2	0x00
0x0E	0x170E	Redundant Receive STS-3 Transport Interrupt Enable Register Byte 1	0x00
0x0F	0x170F	Redundant Receive STS-3 Transport Interrupt Enable Register – Byte 0	0x00
0x10	0x1710	Redundant Receive STS-3 Transport B1 Error Count – Byte	0x00
0x11	0x1711	Redundant Receive STS-3 Transport B1 Error Count – Byte 2	0x00
0x12	0x1712	Redundant Receive STS-3 Transport B1 Error Count – Byte 1	0x00
0x13	0x1713	Redundant Receive STS-3 Transport B1 Error Count – Byte 0	0x00
0x14	0x1714	Redundant Receive STS-3 Transport B2 Error Count – Byte 3	0x00
0x15	0x1715	Redundant Receive STS-3 Transport B2 Error Count – Byte 2	0x00
0x16	0x1716	Redundant Receive STS-3 Transport B2 Error Count – Byte 1	0x00

INDIVIDUAL REGISTER ADDRESS	Address Location	REGISTER NAME	DEFAULT VALUES
0x17	0x1717	Redundant Receive STS-3 Transport B2 Error Count – Byte 0	0x00
0x18	0x1718	Redundant Receive STS-3 Transport REI-L Error Count – Byte 3	0x00
0x19	0x1719	Redundant Receive STS-3 Transport REI-L Error Count – Byte 2	0x00
0x1A	0x171A	Redundant Receive STS-3 Transport REI-L Error Count – Byte 1	0x00
0x1B	0x171B	Redundant Receive STS-3 Transport REI-L Error Count – Byte 0	0x00
0x1C	0x171C	Reserved	0x00
0x1D - 0x1E	0x171D - 0x171E	Reserved	0x00
0x1F	0x171F	Redundant Receive STS-3 Transport K1 Byte Value	0x00
0x20 - 0x22	0x1720 - 0x1722	Reserved	0x00
0x23	0x1723	Redundant Receive STS-3 Transport K2 Byte Value	0x00
0x24 - 0x26	0x1724 – 0x1726	Reserved	0x00
0x27	0x1727	Redundant Receive STS-3 Transport S1 Byte Value	0x00
0x28 – 0x2A	0x1728 – 0x172A	Reserved	0x00
0x2B	0x172B	Redundant Receive STS-3 Transport – In-Sync Threshold Value	0x00
0x2C, 0x2D	0x172C, 0x172D	Reserved	0x00
0x2E	0x172E	Redundant Receive STS-3 Transport – LOS Threshold Value MSB	0xFF
0x2F	0x1725	Redundant Receive STS-3 Transport – LOS Threshold Value – LSB	0xFF
0x30	0x1730	Reserved	0x00
0x31	0x1731	Redundant Receive STS-3 Transport – SF Set Monitor Interval – Byte 2	0x00
0x32	0x1732	Redundant Receive STS-3 Transport – SF Set Monitor Interval – Byte 1	0x00
0x33	0x1733	Redundant Receive STS-3 Transport – SF Set Monitor Interval – Byte 0	0x00
0x34, 0x35	0x1734 - 0x1735	Reserved	0x00
0x36	0x1736	Redundant Receive STS-3 Transport – SF Set Threshold – Byte 1	0x00
0x37	0x1737	Redundant Receive STS-3 Transport – SF Set Threshold – Byte 0	0x00

XRT94L33



Rev 2.0.0

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

DEFAULT VALUES INDIVIDUAL ADDRESS REGISTER NAME REGISTER LOCATION **A**DDRESS 0x38, 0x39 0x1738, 0x1739 0x00 Reserved 0x173A 0x3A 00x0Redundant Receive STS-3 Transport - SF Clear Threshold Byte 1 0x3B 0x173B 0x00 Redundant Receive STS-3 Transport - SF Clear Threshold - Byte 0 0x3C 0x173C 0x00 Reserved 0x173D 0x00 0x3D Redundant Receive STS-3 Transport - SD Set Monitor Interval - Byte 2 0x3E 0x173E Redundant Receive STS-3 Transport - SD Set Monitor 0x00 Interval – Byte 1 Redundant Receive STS-3 Transport 0x3F 0x173F SD Set Monitor 0x00 Interval – Byte 0 0x40, 0x41 0x1740, 0x1741 0x00 Reserved 0x42 0x1742 Redundant Receive STS-3 Transport SD Set Threshold -0x00 Byte 1 0x43 0x1743 Redundant Receive STS-3 Transport - SD Set Threshold -0x00 0x44, 0x45 0x1744, 0x1745 0x00 Reserved 0x46 0x1746 Redundant Receive STS-3 Transport - SD Clear Threshold 0x00 - Byte 1 0x1747 0x47 Redundant Receive STS-3 Transport - SD Clear Threshold 0x00 - Byte 0 0x48 - 0x4A0x1748 - 0x174A 0x00 Reserved 0x4B 0x174B 0x00 Redundant Receive STS-3 Transport - Force SEF Condition 0x4C, 0x4E 0x174C, 0x174E 0x00 Reserved 0x174F 0x4F Redundant Receive STS-3 Transport - Receive J0 Trace 0x00 **Buffer Control** 0x50, 0x51 0x1750, 0x1751 0x00 Reserved 0x52 0x1752 0x00 Redundant Receive STS-3 Transport - SD Burst Error Count Tolerance - Byte 1 0x53 0x1753 Redundant Receive STS-3 Transport - SD Burst Error 0x00 Count Tolerance - Byte 0 0x54, 0x55 0x1754, 0x1755 0x00 Reserved 0x1756 0x00 0x56 Redundant Receive STS-3 Transport - SF Burst Error Count Tolerance - Byte 1 Redundant Receive STS-3 Transport - SF Burst Error 0x57 0x1757 0x00 Count Tolerance - Byte 0

INDIVIDUAL REGISTER ADDRESS	Address Location	REGISTER NAME	DEFAULT VALUES
0x58	0x1758	Reserved	0x00
0x59	0x1759	Redundant Receive STS-3 Transport –Receive SD Clear Monitor Interval – Byte 2	0xFF
0x5A	0x175A	Redundant Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 1	0xFF
0x5B	0x175B	Redundant Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 0	0xFF
0x5C	0x175C	Reserved	0x00
0x5D	0x175D	Redundant Receive STS-3 Transport Receive SF Clear Monitor Interval – Byte 2	0xFF
0x5E	0x175E	Redundant Receive STS-3 Transport - Receive SF Clear Monitor Interval - Byte 1	0xFF
0x5F	0x175F	Redundant Receive STS-3 Transport - Receive SF Clear Monitor - Byte 0	0xFF
0x60 - 0x62	0x1760 - 0x1762	Reserved	0x00
0x63	0x1763	Redundant Receive STS 3 Transport – Auto AIS Control Register	0x00
0x64 - 0x66	0x1764 - 0x1766	Reserved	0x00
0x67	0x1767	Redundant Receive STS-3 Transport – Serial Port Control Register	0x00
0x68 – 0x6A	0x1768 - 0x176A	Reserved	0x00
0x6B	0x176B	Redundant Receive STS-3 Transport – Auto AIS (in Downstream STS-1s) Control Register	0x00
0x6C - 0x79	0x176C - 0x1779	Reserved	0x00
0x7A	0x117A	Redundant Receive STS-3 Transport – TOH Capture Indirect Address	0x00
0x7B	0x117B	Redundant Receive STS-3 Transport – TOH Capture Indirect Address	0x00
0x7C	0x117C	Redundant Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x7D	0x117D	Redundant Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x7E	0x117E	Redundant Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x7F	0x117F	Redundant Receive STS-3 Transport – TOH Capture Indirect Data	0x00
0x80 – 0xFF	0x1780 – 0x17FF	Reserved	0x00



1.7.2 REDUNDANT RECEIVE STS-3 TOH PROCESSOR BLOCK REGISTER DESCRIPTION

Table 152: Redundant Receive STS-3 Transport Control Register – Byte 0 (Address Location= 0x1703)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
STS-N OH Extract	SF Detect Enable	SD Detect Enable	Descramble Disable	SDH/ SONET*	REI-L Error Type	B2 Error Type	B1 Error Type
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	STS-N OH	R/W	STS-N Overhead Extract (Revision C Silicon Only):
	Extract		This READ/WRITE bit-field permits the user to configure the RxTOH output port to output the TOH for all lower-tributary STS-1s within the incoming STS-3 signal.
			0 - Disables this feature. In this mode, the RxTOH output port will only output the TOH for the first STS-1 within the incoming STS-3 signal.
			1 – Enables this feature.
6	SF Detect	R/W	Signal Failure (SF) Detect Enable:
	Enable		This READ/WRITE bit-field permits the user to enable or disable SF Detection by the Redundant Receive STS-3 TOH Processor Block.
			0 – SF Detection is disabled.
			1 – SF Detection is enabled:
5	SD Detect	R/W	Signal Degrade (SD) Detect Enable:
	Enable		This READ/WRITE bit-field permits the user to enable or disable SD Detection by the Redundant Receive STS-3 TOH Processor Block.
		111	0 – SD Detection is disabled.
		400	1 – SD Detection is enabled.
4	Descramble	R/W	De-Scramble Disable:
	Disable	sto d	This READ/WRITE bit-field permits the user to either enable or disable descrambling by the Redundant Receive STS-3 TOH Processor block.
	'	o Wile	0 - De-Scrambling is enabled.
			1 – De-Scrambling is disabled.
3	SDH/SONET*	R/W	SDH/SONET Select:
			This READ/WRITE bit-field permits the user to configure the Redundant Receiver to operate in either the SONET or SDH Mode.
			0 - Configures the Redundant Receiver to operate in the SONET Mode.
			1 – Configures the Redundant Receiver to operate in the SDH Mode.
2	REI-L Error	R/W	REI-L (Line – Remote Error Indicator) Error Type:
	Type		This READ/WRITE bit-field permits the user to specify how the "Redundant Receive Transport REI-L Error Count" register is incremented.
			0 - Configures the Redundant Receive STS-3 TOH Processor block to count REI-L Bit Errors.

			In this case the "Redundant Receive Transport REI-L Error Count" register will be incremented by the value of the lower nibble within the M0/M1 byte.
			1 – Configures the Redundant Receive STS-3 TOH Processor block to count REI-L Frame Errors.
			In this case the "Redundant Receive Transport REI-L Error Count" register will be incremented each time the STS-3 Redundant Receiver receives a "non-zero" M0/M1 byte.
1	B2 Error Type	R/W	B2 Error Type:
			This READ/WRITE bit-field permits the user to specify how the "Redundant Receive Transport B2 Error Count" register is incremented.
			0 - Configures the Redundant Receive STS-3 TOH Processor block to count B2 bit errors.
			In this case, the "Redundant Receive Transport B2 Error Count" register will be incremented by the number of bits, within the B2 value, that is in error.
			1 – Configures the Redundant Receive STS-3 TOH Processor block to count B2 frame errors.
			In this case, the "Redundant Receive Transport B2 Error Count" register will be incremented by the number of erred STS-3 frames.
0	B1 Error Type	R/W	B1 Error Type:
			This READ/WRITE bit-field permits the user to specify how the "Redundant Receive Transport B1 Error Count" register is incremented.
			0 - Configures the Redundant Receive STS-3 TOH Processor block to count B1 bit errors.
			In this case, the "Redundant Receive Transport B1 Error Count" register will be incremented by the number of bits, within the B1 value, that is in error.
		, (0	1 - Configures the Redundant Receive STS-3 TOH Processor block to count B2 bit errors.
		duck	In this case, the "Redundant Receive Transport B1 Error Count" register will be incremented by the number of erred STS-3 frames.
	Thebri	andma	
		// N	



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 153: Redundant Receive STS-3 Transport Status Register – Byte 1 (Address Location= 0x1706)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Unused			J0 Message	J0 Message	AIS_L Defect
					Mismatch Defect Declared	Unstable Defect Declared	Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 3	Unused	R/O	6
2	J0 Message Mismatch Defect Declared	R/O	J0 – Section Trace Mismatch Indicator: This READ-ONLY bit-field indicates whether or not the Redundant Receive STS-3 TOH Processor block is currently declaring the Section Trace Mismatch condition. The Redundant Receive STS-3 TOH Processor block will declare a J0 (Section Trace) Mismatch condition, whenever it accepts a J0 Message that differs from the "Expected J0 Message". 0 – Section Trace Mismatch Condition is NOT declared. 1 – Section Trace Mismatch Condition is currently declared.
1	J0 Message Unstable Defect Declared	R/O	J0 – Section Trace Unstable Indicator: This READ-ONLY bit-field indicates whether or not the Redundant Receive STS-3 TOH Processor block is currently declaring the Section Trace Instability condition. The Redundant Receive STS-3 TOH Processor block will declare a J0 (Section Trace) Unstable condition, whenever the "J0 Unstable" counter reaches the value 8. The "J0 Unstable" counter will be incremented for each time that it receives a J0 message that differs from the "Expected J0 Message". The "J0 Unstable" counter is cleared to "0" whenever the Redundant Receive STS-3 TOH Processor block has received a given J0 Message 3 (or 5) consecutive times. Note: Receiving a given J0 Message 3 (or 5) consecutive times also sets this bit-field to "0". 0 — Section Trace Instability condition is NOT declared.
0	AIS_L Defect Declared	R/O	AIS-L (Line AIS) State: This READ-ONLY bit-field indicates whether or not the Redundant Receive STS-3 TOH Processor block is currently detecting an AIS-L (Line AIS) pattern in the incoming STS-3 data stream. AIS-L is declared if bits 6, 7 and 8 (e.g., the Least Significant Bits, within the K2 byte) value the value "1, 1, 1" for five consecutive STS-1 frames. 0 – AIS-L is NOT currently declared. 1 – AIS-L is currently being declared.

Table 154: Redundant Receive STS-3 Transport Status Register – Byte 0 (Address Location= 0x1707)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
RDI-L Defect Declared	S1 Byte Unstable Defect Declared	(K1, K2) APS Byte Unstable	SF Defect Declared	SD Defect Declared	LOF Defect Declared	SEF Defect Declared	LOS Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	RDI-L Defect	R/O	RDI-L (Line Remote Defect Indicator) Defect Declared:
	Declared		This READ-ONLY bit-field indicates whether or not the Redundant Receive STS-3 TOH Processor block is currently declaring a Line-Remote Defect Indicator (RDI-L), in the incoming STS-3 signal. RDI-L is declared when bits 6, 7 and 8 (e.g., the three least significant bits) of the K2 byte contains the "1, 1, 0" pattern in 5 consecutive STS-3 frames.
			0 – RDI-L is NOT being declared.
			1 – RDI-L is currently being declared.
6	S1 Byte	R/O	S1 Byte Unstable Defect Declared Condition:
	Unstable Defect Declared		This READ-ONLY bit-field indicates whether or not the Redundant Receive STS-3 TOH Processor block is currently declaring the "S1 Byte Instability" condition. The Redundant Receive STS-3 TOH Processor block will declare an "S1 Byte Instability" condition whenever the "S1 Byte Unstable Counter" reaches the value 32. The "S1 Byte Unstable Counter" is incremented for each time that the Redundant Receive STS-3 TOH Processor block receives an S1 byte that differs from the previously received S1 byte. The "S1 Byte Unstable Counter" is cleared to "0" when the same S1 byte is received for 8 consecutive STS-3 frames.
			Note: Receiving a given S1 byte, in 8 consecutive STS-3 frames also sets this bit-field to "0".
		, c	0 – \$1 Instability Condition is NOT declared.
		9/1	1- S1 Instability Condition is currently declared.
5	(K1, K2) APS Byte Unstable	R/O	APS (K1, K2 Byte) Unstable Condition:
	the	and	This READ-ONLY bit-field indicates whether or not the Redundant Receive STS-3 TOH Processor block is currently declaring the "K1, K2 Byte Unstable" condition. The Redundant Receive STS-3 TOH Processor block will declare a "K1, K2 Byte Unstable" condition whenever the Redundant Receive STS-3 TOH Processor block fails to receive the same set of K1, K2 bytes, in 12 consecutive STS-3 frames. The "K1, K2 Byte Unstable" condition is cleared whenever the Redundant Receive STS-3 TOH Processor block receives a given set of K1, K2 byte values in three consecutive STS-3 frames.
			0 – K1, K2 Unstable Condition is NOT currently declared.
			1 – K1, K2 Unstable Condition is currently declared.
4	SF Defect Declared	R/O	SF (Signal Failure) Defect Declared:
	Declared		This READ-ONLY bit-field indicates whether or not the Redundant Receive STS-3 TOH Processor block is currently declaring the SF defect. The SF defect is declared when the number of B2 errors observed over a given time interval exceeds a certain threshold.
			0 – SF Defect is NOT being declared.
			This bit is set to "0" when the number of B2 errors (accumulated over a given

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			interval of time) does not exceed the "SF Declaration" threshold.
			1 – SF Defect is being declared.
			This bit is set to "1" when the number of B2 errors (accumulated over a given interval of time) does exceed the "SF Declaration" threshold.
3	SD Defect	R/O	SD (Signal Degrade) Defect Declared:
	Declared		This READ-ONLY bit-field indicates whether or not the Redundant Receive STS-3 TOH Processor block is currently declaring the SD defect. The SD defect is declared when the number of B2 errors observed over a given time interval exceeds a certain threshold.
			0 – SD Defect is NOT being declared.
			This bit is set to "0" when the number of B2 errors (accumulated over a given interval of time) does not exceed the "SD Declaration" threshold.
			1 – SD Defect is being declared.
			This bit is set to "1" when the number of B2 errors (accumulated over a given interval of time) does exceed the "SD Declaration" threshold.
2	LOF	R/O	LOF (Loss of Frame) Defect Declared:
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Redundant Receive STS-3 TOH Processor block is currently declaring an LOF defect condition. The Redundant Receive STS-3 TOH Processor block will declare an LOF defect condition, if continues to declare the SEF (Severely Errored Frame) condition for 3ms (or 24 SONET frame periods). 0 – LOF is NOT being declared.
			1 – LOF is currently being declared.
1	SEF Defect Declared	R/O	SEF (Severely Errored Frame) Defect Declared: This READ ONLY bit-field indicates whether or not the Redundant Receive STS-3 TOH Processor block is currently declaring an SEF condition. The SEF condition is declared, if the "SEF Declaration Criteria"; per the settings of the FRPATOUT[1:0] bits, within the Redundant Receive STS-3 Transport – In-Sync Threshold Value Register (Address Location= 0x172B). 0 – SEF condition is NOT being declared. 1 – SEF condition is currently being declared.
0	LOS	R/O	LOS (Loss of Signal) Indicator:
	Defect Declared	y data	This READ-ONLY bit-field indicates whether or not the Redundant Receive STS-3 TOH Processor block is currently declaring an LOS (Loss of Signal) defect condition. The Redundant Receive STS-3 TOH Processor block will declare an LOS defect condition if it detects "LOS_THRESHOLD[15:0]" consecutive "All Zero" bytes in the incoming STS-3 data stream.
			Note: The user can set the "LOS_THRESHOLD[15:0]" value by writing the appropriate data into the "Redundant Receive STS-3 Transport – LOS Threshold Value" Register (Address Location= 0x172E and 0x172F).
			$\rm 0-Indicates$ that the Redundant Receive STS-3 TOH Processor block is NOT currently declaring an LOS defect condition.
			1 – Indicates that the Redundant Receive STS-3 TOH Processor block is currently declaring an LOS defect condition.

Table 155: Redundant Receive STS-3 Transport Interrupt Status Register – Byte 2 (Address Location= 0x1709)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Change of AIS-L Condition Interrupt Status	Change of RDI-L Condition Interrupt Status				
R/O	R/O	R/O	R/O	R/O	R/O	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 2	Unused	R/O	:6 &
1	Change of AIS-L Condition Interrupt Status	RUR	Change of AIS-L (Line AIS) Condition Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change of AIS-L Condition" interrupt has occurred since the last read of this register. 0 – The "Change of AIS-L Condition" interrupt has not occurred since the last read of this register. 1 – The "Change of AIS-L Condition" interrupt has occurred since the last read of this register. Note: The user can obtain the current state of AIS-L by reading the contents of Bit 0 (AIS-L Defect Declared) within the "Redundant Receive STS-3 Transport Status Register – Byte 1" (Address Location= 0x1706).
0	Change of RDI-L Condition Interrupt Status	RUR	Change of RDI-L (Line - Remote Defect Indicator) Condition Interrupt Status: This RESET upon-READ bit-field indicates whether or not the "Change of RDI-L Condition" interrupt has occurred since the last read of this register. Of The "Change of RDI-L Condition" interrupt has not occurred since the last read of this register. 1 - The "Change of RDI-L Condition" interrupt has occurred since the last read of this register. Note: The user can obtain the current state of RDI-L by reading out the state of Bit 7 (RDI-L Declared) within the "Redundant Receive STS-3 Transport Status Register - Byte 0" (Address Location = 0x1707).



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 156: Redundant Receive STS-3 Transport Interrupt Status Register – Byte 1 (Address Location= 0x170A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
New S1 Byte Interrupt Status	Change in S1 Unstable State Interrupt Status	Change in J0 Message Unstable State Interrupt Status	New J0 Message Interrupt Status	Change in J0 Mismatch Condition Interrupt Status	Receive TOH CAP DONE Interrupt Status	Change in (K1, K2) APS Bytes Unstable State Interrupt Status	NEW K1K2 Byte Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

			35.8
BIT NUMBER	NAME	Түре	DESCRIPTION
7	New S1 Byte Value Interrupt Status	RUR	New S1 Byte Value Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "New S1 Byte
			Value" Interrupt has occurred since the last read of this register. 0 – Indicates that the "New S1 Byte Value" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the New \$1 Byte Value" interrupt has occurred since the last read of this register.
			Note: The user can obtain the value for this most recently accepted value of the S1 byte by reading the "Redundant Receive STS-3 Transport S1 Value" register (Address Location= 0x1727).
6	Change in S1	RUR	Change in S1 Byte Unstable State – Interrupt Status:
	Byte Unstable State Interrupt Status		This RESET-upon READ bit-field indicates whether or not the "Change in \$1 Byte Unstable State" Interrupt has occurred since the last read of this register.
		produ	0 – indicates that the "Change in S1 Byte Unstable State" Interrupt has occurred since the last read of this register.
			— Indicates that the "Change in S1 Byte Unstable State" Interrupt has not occurred since the last read of this register.
	1/1º		The user can obtain the current "S1 Unstable" state by reading the contents of Bit 6 (S1 Unstable) within the "Redundant Receive STS-3 Transport Status Register – Byte 0" (Address Location= 0x1707).
5	Change in J0 Message	RUR	Change of J0 (Section Trace) Message Unstable condition – Interrupt Status:
	Interrupt Status	Jnstable State nterrupt Status	This RESET-upon-READ bit-field indicates whether or not the "Change of J0 (Section Trace) Message Instability" condition interrupt has occurred since the last read of this register.
			0 – Indicates that the "Change of J0 (Section Trace) Message Instability" condition interrupt has not occurred since the last read of this register.
			1 – Indicates that the "Change of J0 (Section Trace) Message Instability" condition interrupt has occurred since the last read of this register.
4	New J0 Message	RUR	New J0 Trace Message Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "New J0 Trace Message" interrupt has occurred since the last read of this register.

		1	
			0 – Indicates that the "New J0 Trace Message Interrupt" has not occurred since the last read of this register.
			$1-\mbox{Indicates}$ that the "New J0 Trace Message Interrupt" has occurred since the last read of this register.
			Note: The user can read out the contents of the "Receive J0 Trace Buffer", which is located at Address location 0x1300 through 0x133F.
3	Change in J0	RUR	Change in J0 – Section Trace Mismatch Condition" Interrupt Status:
	Mismatch Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in J0 – Section Trace Mismatch Condition" interrupt has occurred since the last read of this register.
			0 - Indicates that the "Change in J0 - Section Trace Mismatch Condition" interrupt has not occurred since the last read of this register.
			1 – Indicates that the "Change in 10 – Section Trace Mismatch Condition" interrupt has occurred since the last read of this register.
			Note: The user can determine whether the "J0 – Section Trace Mismatch" condition is "cleared" or "declared" by reading the state of Bit 2 (J0_MIS) within the "Redundant Receive STS-3 Transport Status Register – Byte 1 (Address Location= 0x1706).
2	Receive TOH	RUR	Receive TOH Capture DONE – Interrupt Status:
	CAP DONE Interrupt Status		This RESET-upon READ bit-field indicates whether the "Receive TOH Data Capture" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Redundant Receive STS-3 TOH Processor block will generate an interrupt anytime it has captured the last TOH byte into the Capture Buffer.
			Note: Once the TOH (of a given STS-3 frame) has been captured and loaded into the "Receive TOH Capture" buffer, it will remain there for one SONET frame period.
			0 - Indicates that the "Receive TOH Data Capture" Interrupt has NOT occurred since the last read of this register.
		duce	 Indicates that the "Receive TOH Data Capture" Interrupt has occurred since the last read of this register.
1	Change in APS	RUR	Change of APS (K1, K2 Byte) Unstable Condition – Interrupt Status:
	(K1, K2 Byte) Unstable Status Interrupt Status	9 W	This RESET-upon-READ bit-field indicates whether or not the "Change of APS (K1, K2 Byte) Instability Condition" interrupt has occurred since the last read of this register.
			0 – Indicates that the "Change of APS (K1, K2 Byte) Instability Condition" interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change of APS (K1, K2 Byte) Instability Condition" interrupt has occurred since the last read of this register.
			Note: The user can determine whether the "K1, K2 Unstable Condition" is being declared or cleared by reading out the contents of Bit 5 (APS Unstable), within the "Redundant Receive STS-3 Transport Status Register – Byte 0" (Address Location = 0x1707).
0	NEW K1K2 Byte	RUR	New K1, K2 Byte Value Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "New K1, K2 Byte Value" Interrupt has occurred since the last read of this register.
			0 – Indicates that the "New K1, K2 Byte Value" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "New K1, K2 Byte Value" Interrupt has occurred since

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

the last read of this register.			
Note: The user can obtain the contents of the new K1 byte by reading out the contents of the "Redundant Receive STS-3 Transport K1 Value" Register (Address Location= 0x171F). Further, the user can also obtain the contents of the new K2 byte by reading out the contents of the "Redundant Receive STS-3 Transport K2 Value" Register (Address Location= 0x1723).			

The product are no longered (OBS)

The product are no longered (OBS)

The product are no longered (OBS)

Table 157: Redundant Receive STS-3 Transport Interrupt Status Register – Byte 0 (Address Location= 0x170B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Change in SF Condition Interrupt Status	Change in SD Condition Interrupt Status	Detection of REI-L Error Interrupt Status	Detection of B2 Error Interrupt Status	Detection of B1 Error Interrupt Status	Change of LOF Condition Interrupt Status	Change of SEF Condition Interrupt Status	Change of LOS Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Change in SF	RUR	Change of Signal Failure (SF) Condition Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of SF Condition Interrupt" has occurred since the last read of this register.
			0 - The "Change of SF condition Interrupt" has NOT occurred since the last read of this register
			1 – The "Change of SF Condition Interrupt" has occurred since the last read of this register.
			Note: The user can determine the current "SF" condition by reading out the state of Bit 4 (SF Declared) within the "Redundant Receive STS-3 Transport Status Register – Byte 0 (Address Location= 0x1707).
6	Change of SD	RUR	Charge of Signal Degrade (SD) Condition Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of SD Condition interrupt" has occurred since the last read of this register.
			0 - The 'Change of SD Condition Interrupt" has NOT occurred since the last read of this register.
		ducer	The "Change of SD Condition Interrupt" has occurred since the last read of this register.
	The br	Sho	Note: The user can determine the current "SD" condition by reading out the state of Bit 3 (SD Declared) within the "Redundant Receive STS-3 Transport Status Register – Byte 0 (Address Location= 0x1707).
5	Detection of REI-	RUR	Detection of Line – Remote Error Indicator Interrupt Status:
	L Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Declaration of Line – Remote Error Indicator" Interrupt has occurred since the last read of this register.
			$\bf 0$ - The "Declaration of Line - Remote Error Indicator" Interrupt has NOT occurred since the last read of this register.
			1- The "Declaration of Line $-$ Remote Error Indicator" Interrupt has occurred since the last read of this register.
4	Detection of B2	RUR	Detection of B2 Error Interrupt Status:
	Error Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of B2 Error Interrupt" has occurred since the last read of this register.
			${\bf 0}$ - The "Detection of B2 Error Interrupt" has NOT occurred since the last read of this register.
			1 - The "Detection of B2 Error Interrupt" has occurred since the last read of

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			this register.
3	Detection of B1	RUR	Detection of B1 Error Interrupt Status:
	Error Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of B1 Error Interrupt" has occurred since the last read of this register.
			0 - The "Detection of B1 Error Interrupt" has NOT occurred since the last read of this register.
			1 – The "Detection of B1 Error Interrupt" has occurred since the last read of this register
2	Change of LOF	RUR	Change of Loss of Frame (LOF) Condition Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of LOF Condition" interrupt has occurred since the last read of this register.
			0 - The "Change of LOF Condition" interrupt has NOT occurred since the last read of this register.
			1 – The "Change of LOF Condition" interrupt has occurred since the last read of this register.
			Note: The user can determine the current "LOF" condition by reading out the state of Bit 2 (LOF Defect Declared) within the "Redundant Receive STS-3 Transport Status Register – Byte 0 (Address Location= 0x1707).
1	Change of SEF	RUR	Change of SEF Condition Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of SEF" Condition Interrupt has occurred since the last read of this register.
			0 - The "Change of SEF Condition" Interrupt has NOT occurred since the last read of this register.
			1 - The 'Change of SEF Condition" Interrupt has occurred since the last read of this register.
		AUG	Note: The user can determine the current "SEF" condition by reading out the state of Bit 1 (SEF Defect Declared) within the "Redundant Receive STS-3 Transport Status Register – Byte 0 (Address Location= 0x1707).
0	Change of LOS	RUR	Change of Loss of Signal (LOS) Condition Interrupt Status:
	Condition Interrupt Status	6, 9,	This RESET-upon-READ bit-field indicates whether or not the "Change of LOS Condition" interrupt has occurred since the last read of this register.
		garad	0 - The "Change of LOS Condition" Interrupt has NOT occurred since the last read of this register.
		**	1 - The "Change of LOS Condition" Interrupt has occurred since the last read of this register.
			Note: The user can determine the current "LOS" status by reading out the contents of Bit 0 (LOS Defect Declared) within the Redundant Receive STS-3 Transport Status Register – Byte 0 (Address Location= 0x1707).

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 158: Redundant Receive STS-3 Transport Interrupt Enable Register – Byte 2 (Address Location= 0x170D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Change of AIS-L Condition Interrupt Enable	Change of RDI-L Condition Interrupt Enable				
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 2	Unused	R/O	.6.
1	Change of AIS-L Condition Interrupt Enable	R/W	Change of AIS-L (Line AIS) Condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change of AIS-L Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions. • When the Redundant Receive STS-3 TOH Processor block declares the "AIS-L" condition. • When the Redundant Receive STS-3 TOH Processor block clears the "AIS-L" condition. 0 – Disables the "Change of AIS-L Condition" Interrupt. 1 – Enables the "Change of AIS-L Condition" Interrupt. Note The user can determine the current "AIS-L" condition by reading out the state of Bit 0 (AIS-L) within the "Redundant Receive STS-3 Transport Status Register – Byte 1" (Address Location= 0x1706).
0	Change of RDI-L Condition Interrupt Enable	RW	Change of RDI-L (Line Remote Defect Indicator) Condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change of RDI-L Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions. • When the Redundant Receive STS-3 TOH Processor block declares the "RDI-L" condition. • When the Redundant Receive STS-3 TOH Processor block clears the "RDI-L" condition. 0 – Disables the "Change of RDI-L Condition" Interrupt. 1 – Enables the "Change of RDI-L Condition" Interrupt.



Table 159: Redundant Receive STS-3 Transport Interrupt Enable Register – Byte 1 (Address Location= 0x170E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
New S1 Byte Interrupt Enable	Change in S1 Byte Unstable State Interrupt Enable	Change in J0 Message Unstable State Interrupt Enable	New J0 Message Interrupt Enable	J0 Mismatch Interrupt Enable	Receive TOH CAP DONE Interrupt Enable	Change in APS Unstable State Interrupt Enable	NEW K1K2 Byte Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

-	_							
			nis ed					
BIT NUMBER	NAME	TYPE	DESCRIPTION					
7	New S1 Byte Value Interrupt Enable	R/W	New S1 Byte Value Interrupt Enable: This READ/WRITE bit-field permits the user to enable or disable the "New S7 Byte Value" Interrupt. If the user enables this interrupt, then the Redundan Receive STS-3 TOH Processor block will generate this interrupt anytime is receives and accepts a new S1 byte value. The Redundant Receive STS-3 TOH Processor block will accept a new S1 byte after it has received it for 8 consecutive STS-3 frames. 0 – Disables the "New S1 Byte Value" Interrupt. 1 – Enables the "New S1 Byte Value" Interrupt.					
6	Change in S1 Unstable State Interrupt Enable	R/W	Change in S1 Byte Unstable State Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change in S1 Byte Unstable State" Interrupt. If the user enables this bit-field, then the Redundant Receive STS-3 TOH Processor block will generate an interrupt in response to either of the following conditions. When the Redundant Receive STS-3 TOH Processor block declares the "S1 Byte Instability" condition. When the Redundant Receive STS-3 TOH Processor block clears the "S1 Byte Instability" condition. Disables the "Change in S1 Byte Unstable State" Interrupt.					
5	Change in J0 Message Unstable State Interrupt Enable	R/W	 Change of J0 (Section Trace) Message Instability condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change of J0 Message Instability Condition" Interrupt. If the user enables this interrupt, then the Redundant Receive STS-3 TOH Processor block will generate an interrupt in response to either of the following conditions. Whenever the Redundant Receive STS-3 TOH Processor block declares the "J0 Message Instability" condition. Whenever the Redundant Receive STS-3 TOH Processor block clears the "J0 Message Instability" condition. Disable the "Change of J0 Message Instability" Interrupt. Enables the "Change of J0 Message Instability" Interrupt. 					
4	New J0 Message	R/W	New J0 Trace Message Interrupt Enable:					

	Interrupt		This DEADAMOITE hit field permits the user to enable or disable the "New 10
	Interrupt Enable		This READ/WRITE bit-field permits the user to enable or disable the "New J0 Trace Message" interrupt. If the user enables this interrupt, then the Redundant Receive STS-3 TOH Processor block will generate this interrupt anytime it receives and accepts a new J0 Trace Message. The Redundant Receive STS-3 TOH Processor block will accept a new J0 Trace Message after it has received it 3 (or 5) consecutive times.
			0 – Disables the "New J0 Trace Message" Interrupt.
			1 – Enables the "New J0 Trace Message" Interrupt.
3	J0 Mismatch	R/W	Change in "J0 – Section Trace Mismatch Condition" interrupt enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in J0 – Section Trace Mismatch condition" interrupt. If the user enables this interrupt, then the Redundant Receive STS-3 TOH Processor block will generate an interrupt in response to either of the following events.
			 The Redundant Receive STS-3 TOH Processor block declares a "J0 – Section Trace Mismatch" condition.
			 The Redundant Receive STS-3 TOH Processor block clears the "J0 – Section Trace Mismatch" condition.
			Note: The user can determine whether the "J0 – Section Trace Mismatch" condition is "cleared or "declared" by reading the state of Bit 2 (J0 Message Mismatch Defect Declared) within the "Redundant Receive STS-3 Transport Status Register – Byte 1 (Address Location= 0x1706).
2	Receive TOH	R/W	Receive TOH Capture DONE - Interrupt Enable:
	CAP DONE Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Receive TOH Data Capture" interrupt, within the Redundant Receive STS-3 TOH Processor Block
			If this interrupt is enabled, then the Redundant Receive STS-3 TOH Processor block will generate an interrupt anytime it has captured the last TOH byte into the Capture Buffer.
		1110	Note: Once the TOH (of a given STS-3 frame) has been captured and loaded into the "Receive TOH Capture" buffer, it will remain there for one SONET frame period.
		200	0 - Disables the "Receive TOH Capture" Interrupt.
			1+ Enables the "Receive TOH Capture" Interrupt.
1	Change in APS Unstable	R/W	Change of APS (K1, K2 Byte) Instability Condition - Interrupt Enable:
	State Interrupt Enable	and	This READ/WRITE bit-field permits the user to either enable or disable the "Change of APS (K1, K2 Byte) Instability condition" interrupt. If the user enables this interrupt, then the Redundant Receive STS-3 TOH Processor block will generate an Interrupt in response to either of the following events.
			• If the Redundant Receive STS-3 TOH Processor block declares a "K1, K2 Instability" condition.
			• If the Redundant Receive STS-3 TOH Processor block clears the "K1, K2 Instability" condition.
0	-		New K1, K2 Byte Value Interrupt Enable:
	Byte Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "New K1, K2 Byte Value" Interrupt. If the user enables this interrupt, then the Redundant Receive STS-3 TOH Processor block will generate this interrupt anytime it receives and accepts a new K1, K2 byte value. The Redundant Receive STS-3 TOH Processor block will accept a new K1, K2 byte value, after it has received it within 3 (or 5) consecutive STS-3 frames.

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

rience	Our Connectivity.	
	Rev 2.0.0	

0 – Disables the "New K1, K2 Byte Value" Interrupt.
1 – Enables the "New K1, K2 Byte Value" Interrupt.

The product are no ordered (OBS)

Table 160: Redundant Receive STS-3 Transport Interrupt Status Register - Byte 0 (Address Location= 0x170F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Change of SF Condition Interrupt Enable	Change of SD Condition Interrupt Enable	Detection of REI-L Error Interrupt Enable	Detection of B2 Error Interrupt Enable	Detection of B1 Error Interrupt Enable	Change of LOF Condition Interrupt Enable	Change of SEF Condition Interrupt Enable	Change of LOS Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

	1	1	35.0				
BIT NUMBER	NAME	Түре	DESCRIPTION				
7	Change of SF	R/W	Change of Signal Failure (SF) Condition Interrupt Enable:				
	Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of Signal Failure (SF) Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Redundant Receive STS-3 TOH Processor block either declares or clears the SF defect.				
			0 - Disables the "Change of SF Condition Interrupt".				
			1 – Enables the "Change of SF Condition Interrupt".				
6	Change of SD	R/W	Change of Signal Degrade (SD) Condition Interrupt Enable:				
	Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of Signal Degrade (SD) Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Redundant Receive STS-3 TOH Processor block either declares or clears the SD defect.				
			0 Disables the "Change of SD Condition Interrupt".				
		All S	1 Enables the "Change of SD Condition Interrupt".				
5	Detection of REI-L Interrupt	R/W	Detection of Line – Remote Error Indicator Interrupt Enable:				
	Enable	SOM	This READ/WRITE bit-field permits the user to either enable or disable the "Declaration of Line – Remote Error Indicator" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Redundant Receive STS-3 TOH Processor block declares the "REI-L" defect.				
		0	0 – Disables the "Line - Remote Error Indicator" Interrupt.				
			1 – Enables the "Line – Remote Error Indicator" Interrupt.				
4	Detection of B2	R/W	Detection of B2 Error Interrupt Enable:				
	Error Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B2 Error" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt anytime the Redundant Receive STS-3 TOH Processor block detects a B2 error.				
			0 – Disables the "Detection of B2 Error Interrupt".				
			1 – Enables the "Detection of B2 Error Interrupt".				
3	Detection of B1	R/W	Detection of B1 Error Interrupt Enable:				
	Error Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B1 Error" Interrupt. If the user enables this interrupt, then the				

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			XRT94L33 will generate an interrupt anytime the Redundant Receive STS-3 TOH Processor block detects a B1 error. 0 – Disables the "Detection of B1 Error Interrupt". 1 – Enables the "Detection of B1 Error Interrupt".
2	Change of LOF Condition Interrupt Enable	R/W	Change of Loss of Frame (LOF) Condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change of LOF Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions. • When the Redundant Receive STS-3 TOH Processor block declares the "LOF" condition. • When the Redundant Receive STS-3 TOH Processor clears the "LOF" condition. 0 – Disables the "Change of LOF Condition Interrupt. 1 – Enables the "Change of LOF Condition" Interrupt.
1	Change of SEF Condition Interrupt Enable	R/W	Change of SEF Condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change of SEF Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions. • When the Redundant Receive STS-3 TOH Processor block declares the "SEF" condition. • When the Redundant Receive STS-3 TOH Processor block clears the "SEF" condition. 0 – Disables the "Change of SEF Condition Interrupt". 1 – Enables the "Change of SEF Condition Interrupt".
0	Change of LOS Condition Interrupt Enable	R/W Drodi	Change of Loss of Signal (LOS) Condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change of LOF Condition" interrupt. If the user enables this interrupt, then the XRT94L33 will generate an interrupt in response to either of the following conditions. When the Redundant Receive STS-3 TOH Processor block declares the "LOF" condition. When the Redundant Receive STS-3 TOH Processor block clears the "LOF" condition. Disables the "Change of LOF Condition Interrupt. 1 — Enables the "Change of LOF Condition" Interrupt.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 161: Redundant Receive STS-3 Transport – B1 Error Count Register – Byte 3 (Address Location= 0x1710)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	B1_Error_Count[31:24]						
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT Number	NAME	Түре	DESCRIPTION
7 - 0	B1_Error_Count [31:24]	RUR	B1 Error Count – MSB: This RESET-upon-READ register, along with "Redundant Receive Transport – B1 Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STS-3 TOH Processor block detects a B1 byte error. Note: 1. If the B1 Error Type is configured to be "bit errors", then the Redundant Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of bits, within the B1 value that are in error. 2. If the B1 Error Type is configured to be "frame errors", then the Redundant Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B1 bytes.

Table 162: Redundant Receive STS-3 Transport – B1 Error Count Register – Byte 2 (Address Location= 0x1711)

Віт 7	Віт 6	Віт 5	Віт 3	Віт 2	Віт 1	Віт 0
		B1 Erro	r_Count[23:16]			
RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	000000	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B1_Error_Count	RUR	B1 Error Count (Bits 23 through 16):
	[23:16]	0	This RESET-upon-READ register, along with "Redundant Receive Transport – B1 Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STS-3 TOH Processor block detects a B1 byte error.
			Note:
			1. If the B1 Error Type is configured to be "bit errors", then the Redundant Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of bits, within the B1 value that are in error.
			2. If the B1 Error Type is configured to be "frame errors", then the Redundant Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B1 bytes.

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 163: Redundant Receive STS-3 Transport – B1 Error Count Register – Byte 1 (Address Location= 0x1712)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	B1_Error_Count[15:8]						
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	NAME B1_Error_Count [15:8]	RUR	DESCRIPTION B1 Error Count – (Bits 15 through 8) This RESET-upon-READ register, along with "Redundant Receive Transport – B1 Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STS-3 TOH Processor block detects a B1 byte error Note:
			 If the B1 Error Type is configured to be "bit errors", then the Redundant Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of bits, within the B1 value that are in error. If the B1 Error Type is configured to be "frame errors", then the Redundant Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B1 bytes.

Table 164: Redundant Receive STS-3 Transport - B1 Error Count Register - Byte 0 (Address Location= 0x1713)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0
			B1_Error_C	ount[7:0]			
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	1600	0	0	0	0

B1_Error_Count [7:0] B1_Error_Count RUR [7:0] This RESET-upon-READ register, along with "Redundant Receive – B1 Error Count Register – Bytes 3 through 1; function as a 32 b which is incremented anytime the Redundant Receive ST Processor block detects a B1 byte error. Note: 1. If the B1 Error Type is configured to be "bit errors", then the Receive STS-3 TOH Processor block will increment this 32 bit of the number of bits, within the B1 value that are in error. 2. If the B1 Error Type is configured to be "frame errors", Redundant Receive STS-3 TOH Processor block will increment counter by the number of frames that contain erred B1 bytes.	Redundant counter by

Table 165: Redundant Receive STS-3 Transport – B2 Error Count Register – Byte 3 (Address Location= 0x1714)

Віт 7 Віт	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
-----------	-------	-------	-------	-------	-------	-------

3-CHANNEL	DS3/E3/STS-1 To	O STS-3/STM-1	MAPPER -	ATM REGISTERS
3-CRANNEL	DONENOIO-III	0313-33114-1	WAFFER -	AIMKEGISTERS

	B2_Error_Count[31:24]									
RUR RUR RUR RUR RUR RUR RUR										
0	0	0	0	0	0	0	0			

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	B2_Error_Count	RUR	B2 Error Count – MSB:
	[31:24]		This RESET-upon-READ register, along with "Redundant Receive STS-3 Transport – B2 Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STS-3 TOH Processor block detects a B2 byte error.
			Note:
			1. If the B2 Error Type is configured to be "bit errors", then the Redundant Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of bits, within the B2 value that are in error.
			2. If the B2 Error Type is configured to be "frame errors", then the
			Redundant Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B2 bytes.

Table 166: Redundant Receive STS-3 Transport – B2 Error Count Register – Byte 2 Address Location= 0x1715)

Віт 7	Віт 6	Віт 5	Віт 4.6	Віт 2	Віт 1	Віт 0				
B2_Error_Count[23:16]										
RUR	RUR	RUR	RUR	RUR	RUR	RUR				
0	0	0	0 00	0	0	0				
or Pro orde										

BIT NUMBER	Name	TYPE	DESCRIPTION
7 - 0	B2_Error_Count [23:16]	drive and mark	B2 Error Count (Bits 23 through 16): This RESET-upon-READ register, along with "Redundant Receive STS-3 Transport – B2 Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STS-3 TOH Processor block detects a B2 byte error. Note: 1. If the B2 Error Type is configured to be "bit errors", then the Redundant Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of bits, within the B2 value that are in error. 2. If the B2 Error Type is configured to be "frame errors", then the Redundant Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B2 bytes.

Table 167: Redundant Receive STS-3 Transport - B2 Error Count Register - Byte 1 (Address Location= 0x1716)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	B2_Error_Count[15:8]								
RUR RUR RUR RUR RUR RUR RUR									

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

^	^			^		^	
()	()	()	()	()	()	()	. ()
•	•			•		•	

BIT NUMBER	Name	Түре	DESCRIPTION			
7 - 0	B2_Error_Count [15:8]	RUR	B2 Error Count – (Bits 15 through 8) This RESET-upon-READ register, along with "Redundant Receive STS-3 Transport – B2 Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STS-3 TOH			
			1. If the B2 Error Type is configured to be "bit errors", then the Redundant Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of bits, within the B2 value that are in error.			
			2. If the B2 Error Type is configured to be "frame errors", then the Redundant Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B2 bytes.			

Table 168: Redundant Receive STS-3 Transport – B2 Error Count Register – Byte 0 (Address Location= 0x1717)

Віт 7	Віт 6	Віт 5	Віт 4	B IT 3	Віт 2	Віт 1	Віт 0
			B2_Error_	Count[7:0]			
RUR	RUR	RUR	RUR 🙀	S RUR	RUR	RUR	RUR
0	0	0	0 0	0 0	0	0	0

BIT NUMBER	Name	TYPE	DESCRIPTION
7 - 0	B2_Error_Count[7:0]	RUR	B2 Error Count – LSB:
	The	ta did no	This RESET-upon-READ register, along with "Redundant Receive Transport – B2 Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Redundant Receive STS-3 TOH Processor block detects a B2 byte error. Note: 1. If the B2 Error Type is configured to be "bit errors", then the Redundant Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of bits, within the B2 value that are in error. 2. If the B2 Error Type is configured to be "frame errors", then the Redundant Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B2 bytes.

Table 169: Redundant Receive STS-3 Transport – REI-L Error Count Register – Byte 3 (Address Location= 0x1718)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
REI_L_Error_Count[31:24]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	REI_L_Error_Count	RUR	REI-L Error Count – MSB:
	[31:24]		This RESET-upon-READ register, along with "Redundant Receive Transport – REI-L Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STS-3 TOH Processor block detects a Line - Remote Error Indicator.
			Note:
			1. If the REI-L Error Type is configured to be "bit errors", then the Redundant Receive STS-3 TOH Processor block will increment this 32 bit counter by the value within the REI-L fields of the M1 byte.
			2. If the REI-L Error Type is configured to be "frame errors", then the Redundant Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of frames that contain non-zero REI-L values.

Table 170: Redundant Receive STS-3 Transport – RELL Error Count Register – Byte 2 (Address Location= 0x1719)

Віт 7	Віт 6	Віт 5	Віт 4	Ø Bi73	Віт 2	Віт 1	Віт 0
			REI_L_Error	Count[23:16]			
RUR	RUR	RUR	RUR 6	RUR	RUR	RUR	RUR
0	0	0	00	(0)	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	REI_L_Error_Count	RUR	REI-L Error Count (Bits 23 through 16):
	[23:16]	oot of	This RESET-upon-READ register, along with "Redundant Receive Transport – REI-L Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STS-3 TOH Processor block detects a Line – Remote Error Indicator.
	6, 8,	1	Note:
	Theata	Mor	1. If the REI-L Error Type is configured to be "bit errors", then the Redundant Receive STS-3 TOH Processor block will increment this 32 bit counter by the value within the REI-L fields of the M1 byte.
	8		2. If the REI-L Error Type is configured to be "frame errors", then the Redundant Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of frames that contain non-zero REI-L values.

Table 171: Redundant Receive STS-3 Transport – REI_L Error Count Register – Byte 1 (Address Location= 0x171A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
REI_L_Error_Count[15:8]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	REI_L_Error_Count[15:8]	RUR	REI-L Error Count – (Bits 15 through 8)
			This RESET-upon-READ register, along with "Redundant Receive Transport – REI-L Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Redundant Receive STS-3 TOH Processor block detects a Line –Remote Error Indicator.
			Note:
			1. If the REI-L Error Type is configured to be "bit errors", then the Redundant Receive STS-3 TOH Processor block will increment this 32 bit counter by the value within the REI-L fields of the M1 byte.
			2. If the REI-L Error Type is configured to be "frame errors", then the Redundant Receive STS-3 TOH Processor block will increment this 32 bit counter by the number of frames that contain non-zero REI-L values.

Table 172: Redundant Receive STS-3 Transport – REI_L Error Count Register – Byte 0 (Address Location= 0x171B)

Віт 7	Віт 6	Віт 5	Віт 4	Bif 3	Віт 2	Віт 1	Віт 0
			REI_L_Erro	r_Count[7:0]			
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0		0	0	0
adulgead							

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	REI_L_Error_Count	RUR	REI-L Error Count – LSB:
	[7:0]	and in	This RESET-upon-READ register, along with "Redundant Receive Transport – REI-L Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Redundant Receive STS-3 TOH Processor block detects a Line – Remote Error Indicator. Note: 1. If the REI-L Error Type is configured to be "bit errors", then the Redundant Receive STS-3 TOH Processor block will increment this 32 bit counter by the value within the REI-L fields of the M1 byte. 2. If the REI-L Error Type is configured to be "frame errors", then the Redundant Receive STS-3 TOH Processor block will increment this 32 bit Redundant Receive STS-3 TOH Processor block will increment this 32 bit
			counter by the number of frames that contain non-zero REI-L values.

Table 173: Redundant Receive STS-3 Transport K1 Value (Address Location= 0x171F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Filtered_K1_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION		
7 – 0	Filtered_K1_Value[7:0]	R/O	Filtered/Accepted K1 Value:		
			These READ-ONLY bit-fields contain the value of the most recently		

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

"filtered" K1 value, that the Redundant Receive STS-3 TOH Processor block has received. These bit-fields are valid if the K1/K2 pair (to which it belongs) has been received for 3 consecutive STS-3 frames. This register should be polled by Software in order to determine various
APS codes.

Table 174: Redundant Receive STS-3 Transport K2 Value (Address Location= 0x1723)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			Filtered_K2	_Value[7:0]			
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Filtered_K2_Value [7:0]	R/O	Filtered/Accepted K2 Value: These READ-ONLY bit-fields contain the value of the most recently "filtered" K2 value, that the Redundant Receive STS-3 TOH Processor block has received. These bit-fields are valid if the K1/K2 pair (to which it belongs) has been received for 3 consecutive STS-3 frames. This register should be polled by Software in order to determine various APS codes.

Table 175: Redundant Receive STS-3 Transport S1 Value (Address Location= 0x1727)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0
			Filtered_S1	Value[7:0]			
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0.0	0 0	0	0	0	0

BIT NUMBER	NAME N	TYPE	DESCRIPTION
7 – 0	Filtered_S1_Value[7:0]	R/O	Filtered/Accepted S1 Value:
	The president	May	These READ-ONLY bit-fields contain the value of the most recently "filtered" S1 value that the Redundant Receive STS-3 TOH Processor block has received. These bit-fields are valid if it has been received for 8 consecutive STS-3 frames.

Table 176: Redundant Receive STS-3 Transport – In-Sync Threshold Value (Address Location=0x172B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		FRPATO	OUT[1:0] FRPA		IN[1:0]	Unused
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 5	Unused	R/O	
4 – 3	FRPATOUT[1:0]	R/W	Framing Pattern – SEF Declaration Criteria:
			These two READ/WRITE bit-fields permit the user to define the SEF

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			The relationship bety	or the Redundant Receive STS-3 TOH Processor block. ween the state of these bit-fields and the corresponding eria are presented below.
			FRPATOUT[1:0]	SEF Declaration Criteria
			00 01	The Redundant Receive STS-3 TOH Processor block will declare an SEF condition if either of the following conditions are true for four consecutive SONET frame periods.
				If the last (of the 3) A1 bytes, in the STS-3 data stream is erred, or
				If the first (of the 3) A2 bytes, in the STS-3 data stream, is erred.
				Hence, for this selection, a total of 16 bits are evaluated for SEF declaration.
			10	The Redundant Receive STS-3 TOH Processor block will declare an SEF condition if either of the following conditions are true for four consecutive SONET frame periods.
				If the last two (of the 3) A1 bytes, in the STS-3 data stream, are erred, or
				If the first two (of the 3) A2 bytes, in the STS-3 data stream, are erred.
			C.S.	Herice, for this selection, a total of 32 bits are evaluated for SEF declaration.
			11 Production of the control of the	The Redundant Receive STS-3 TOH Processor block will declare an SEF condition if either of the following conditions are true for four consecutive SONET frame periods.
			(0, 6,00)	If the last three (of the 3) A1 bytes, in the STS-3 data stream, are erred, or
		60	et ot	If the first three (of the 3) A2 bytes, in the STS-3 data stream, are erred.
		Pla	Cay!	Hence, for this selection, a total of 48 bits are evaluated for SEF declaration.
2 - 1	FRPATIN[1:0]	R/W	Framing Pattern – S	EF Clearance Criteria:
		o all	These two READ/M Clearance" criteria fo The relationship betw	/RITE bit-fields permit the user to define the "SEF in the Redundant Receive STS-3 TOH Processor block, ween the state of these bit-fields and the corresponding ria are presented below.
			FRPATIN[1:0]	SEF Clearance Criteria
			00	The Redundant Receive STS-3 TOH Processor

			11	evaluated for SEF clearance. The Redundant Receive STS-3 TOH Processor block will clear the SEF condition if both of the following conditions are true for two consecutive SONET frame periods. If the last two (of the 3) A1 bytes, in the STS-3 data stream, are un-erred, and If the first two (of the 3) A2 bytes, in the STS-3 data stream, are un-erred. Hence, for this selection, a total of 32 bits/frame are evaluated for SEF clearance. The Redundant Receive STS-3 TOH Processor block will clear the SEF condition if both of the following conditions are true for two consecutive SONET frame periods. If the last three (of the 3) A1 bytes, in the STS-3 data-stream, are un-erred, and If the first three (of the 3) A2 bytes, in the STS-3 data stream, are un-erred. Hence, for this selection, a total of 48 bits/frame are evaluated for SEF declaration.
0	Unused	R/O	15 M	eins
	Thepla	andin	or products) ne	



Table 177: Redundant Receive STS-3 Transport – LOS Threshold Value - MSB (Address Location= 0x172E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			LOS_THRES	SHOLD[15:8]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	LOS_THRESHOLD[15:8]	R/W	LOS Threshold Value – MSB:
			These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – LOS Threshold Value – LSB" register specify the number of consecutive (All Zero) bytes that the Redundant Receive STS-3 TOH Processor block must detect before it can declare an LOS condition.

Table 178: Redundant Receive STS-3 Transport – LOS Threshold Value - LSB (Address Location= 0x172F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			LOS_THRE	SHOLD[7:0]			
R/W	R/W	R/W	R/W	⊘R/W	R/W	R/W	R/W
1	1	1	1,0	00	1	1	1

These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – LOS Threshold Value – MSB" register specify the number of consecutive (All Zero) bytes that the Redundant Receive STS-3 TOH Processor block must detect before it can declare an LOS condition.	BIT NUMBER	NAME	TYRE		DESCRIPTION
	7 - 0	LOS_THRESHOLD[7:0]	RAW	These RE Receive S specify the Receive S	AD/WRITE bits, along the contents of the "Redundant STS-3 Transport – LOS Threshold Value – MSB" register a number of consecutive (All Zero) bytes that the Redundant TS-3 TOH Processor block must detect before it can declare

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 179: Redundant Receive STS-3 Transport –Receive SF SET Monitor Interval – Byte 2 (Address Location= 0x1731)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	SF_SET_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SF_SET_MONITOR_ WINDOW [23:16]	R/W	SF_SET_MONITOR_INTERVAL – MSB: These READ/WRITE bits along the contents of the "Redundant Receive STS-3 Transport – SF SET Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the number of STS-3 Frame periods that will constitute a SET Sub-Interval for SF (Signal Failure). When the Redundant Receive STS-3 TOH Processor block is checking for SF, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors exceeds that of programmed into the "Redundant Receive STS-3 Transport SF SET Threshold" register, then an SF condition will be declared.

Table 180: Redundant Receive STS-3 Transport - Receive SF SET Monitor Interval - Byte 1 (Address Location= 0x1732)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
SF_SET_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W 🤎	R/W	R/W	R/W	R/W	R/W
1	1	10	(1	1	1	1

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SF_SET_MONITOR_WINDOW	R/W	SF_SET_MONITOR_INTERVAL (Bits 15 through 8):
	M5:8 0 0 10 0 10 0 10 0 10 0 10 0 10 0 10		These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SF SET Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the number of STS-3 Frame periods that will constitute a SET Sub-Interval for SF (Signal Failure).
			When the Redundant Receive STS-3 TOH Processor block is checking for SF, it will accumulate B2 bit errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 bit errors exceeds that of programmed into the "Redundant Receive STS-3 Transport SF SET Threshold" register, then an SF condition will be declared.



Table 181: Redundant Receive STS-3 Transport – Receive SF SET Monitor Interval – Byte 0 (Address Location= 0x1733)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	SF_SET_MONITOR_WINDOW[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SF_SET_MONITOR_WINDOW[7:0]	R/W	SF_SET_MONITOR_INTERVAL - LSB:
		e to	These READ/WRITE bits along the contents of the "Redundant Receive STS-3 Transport — SF SET Monitor Interval — Byte 2 and Byte 1" registers permit the user to specify the number of STS-3 Frame periods that will constitute a SET Sub-Interval for SF (Signal Failure). When the Redundant Receive STS-3 TOH Processor block is checking for SF, it will accumulate B2 bit errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 bit errors exceeds that of programmed into the "Redundant Receive STS-3 Transport SF SET Threshold" register, then an SF condition will be declared.

Table 182: Redundant Receive STS-3 Transport - Receive SF SET Threshold - Byte 1 (Address Location= 0x1736)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
SF_SET_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	10	O N	1	1	1	1

06.21.21

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SF_SET_THRESHOLD(15:8]	R/W	SF_SET_THRESHOLD - MSB:
			These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SF SET Threshold – Byte 0" registers permit the user to specify the number of B2 bit errors that will cause the Redundant Receive STS-3 TOH Processor block to declare an SF (Signal Failure) condition.
			When the Redundant Receive STS-3 TOH Processor block is checking for SF, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors exceeds that of programmed into this and the "Redundant Receive STS-3 Transport SF SET Threshold – Byte 0" register, then an SF condition will be declared.

Table 183: Redundant Receive STS-3 Transport – Receive SF SET Threshold – Byte 0 Address Location= 0x1737)



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	SF_SET_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SF_SET_THRESHOLD[7: 0]	R/W	SF_SET_THRESHOLD – LSB: These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SF SET Threshold – Byte 1" registers permit the user to specify the number of B2 bit errors that will cause the Redundant Receive STS-3 TOH Processor block to declare an SF (Signal Failure) condition. When the Redundant Receive STS-3 TOH Processor block is
			checking for SF, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors exceeds that of programmed into this and the "Redundant Receive STS-3 Transport SF SET Threshold – Byte 1" register, then an SF condition will be declared.

Table 184: Redundant Receive STS-3 Transport - Receive SF CLEAR Threshold - Byte 1 (Address Location= 0x173A)

Віт 7	Віт 6	Віт 5	Bit 4 Bit 3	Віт 2	Віт 1	Віт 0		
	SF_CLEAR_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W R/W	R/W	R/W	R/W		
1	1	1	10,01	1	1	1		

BIT NUMBER	NAME T	YPE	DESCRIPTION
7 - 0	SF_CLEAR_THRESHOLD	₹/W	SF_CLEAR_THRESHOLD - MSB: These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport - SF CLEAR Threshold - Byte 0" registers permit the user to specify the upper limit for the number of B2 bit errors that will cause the Redundant
	11 daind 1		Receive STS-3 TOH Processor block to clear the SF (Signal Failure) condition. When the Redundant Receive STS-3 TOH Processor block is checking for clearing SF, it will accumulate B2 errors for a total of 8 CLEAR Sub-Interval periods. If the number of accumulated B2 errors is less than that programmed into this and the "Redundant Receive STS-3 Transport SF CLEAR Threshold – Byte 0" register, then an SF condition will be cleared.

Table 185: Redundant Receive STS-3 Transport – Receive SF CLEAR Threshold – Byte 0 (Address Location= 0x173B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
SF_CLEAR_THRESHOLD[7:0]									
R/W R/W R/W R/W R/W R/W R/W									

Experience Our Connect

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

1	1	1	1	1	1	1	1
	=				-	=	=

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SF_CLEAR_THRESHOLD	R/W	SF_CLEAR_THRESHOLD - LSB:
	[7:0]		These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SF CLEAR Threshold – Byte 1" registers permit the user to specify the upper limit for the number of B2 bit errors that will cause the Redundant Receive STS-3 TOH Processor block to clear the SF (Signal Failure) condition.
			When the Redundant Receive STS-3 TOH Processor block is checking for clearing SF, it will accumulate B2 errors for a total of 8 CLEAR Sub-Interval periods. If the number of accumulated B2 errors is less than that programmed into this and the "Redundant Receive STS-3 Transport SF CLEAR Threshold – Byte 1" register, then an SF condition will be cleared.

Table 186: Redundant Receive STS-3 Transport – Receive SD Set Monitor Interval – Byte 2 (Address Location= 0x173D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
SD_SET_MONITOR_WINDOW[23:16]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0.0	0	0	0	
40 off red								

BIT NUMBER	Name	Түрб	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW [23:16]	R/W	SF_SET_MONITOR_INTERVAL – MSB: These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SF SET Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the number of STS-3 Frame periods that will constitute a SET Sub-Interval for SD (Signal Degrade) declaration. When the Redundant Receive STS-3 TOH Processor block is checking for SD, it will accumulate B2 bit errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 bit errors exceeds that of programmed into the "Redundant Receive STS-3 Transport SD SET Threshold" register, then an SD condition will be declared.

Table 187: Redundant Receive STS-3 Transport – Receive SD Set Monitor Interval – Byte 1 (Address Location= 0x173E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
SD_SET_MONITOR_WINDOW[15:8]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

BIT NUMBER	Name	Түре	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW[15:8]	R/W	SD_SET_MONITOR_INTERVAL - Bits 15 through 8:
			These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SD SET Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the number of STS-3 Frame periods that will constitute a SET Sub-Interval for SD (Signal Degrade) declaration.
			When the Redundant Receive STS-3 TOH Processor block is checking for SD, it will accumulate B2 bit errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 bit errors exceeds that of programmed into the "Redundant Receive STS-3 Transport SD SET Threshold" register, then an SD condition will be declared.

Table 188: Redundant Receive STS-3 Transport – Receive SD Set Monitor Interval – Byte 0 (Address Location= 0x173F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
SD_SET_MONITOR_WINDOW[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	10 W	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW[7:0]	VO	SD_SET_MONITOR_INTERVAL – LSB: These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SD SET Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the number of STS-3 Frame periods that will constitute a SET Sub-Interval for SD (Signal Degrade) declaration. When the Redundant Receive STS-3 TOH Processor block is checking for SD, it will accumulate B2 bit errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 bit errors exceeds that of programmed into the "Redundant Receive STS-3 Transport SD SET
			Threshold" register, then an SD condition will be declared.

Table 189: Redundant Receive STS-3 Transport – Receive SD SET Threshold – Byte 1 (Address Location= 0x1742)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SD_SET_THRESHOLD[15:8]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	Name	Түре	DESCRIPTION

EXARExperience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

7 - 0	SD_SET_THRESHOLD[15:8]	R/W	SD_SET_THRESHOLD - MSB:
			These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SD SET Threshold – Byte 0" registers permit the user to specify the number of B2 bit errors that will cause the Redundant Receive STS-3 TOH Processor block to declare an SD (Signal Degrade) condition.
			When the Redundant Receive STS-3 TOH Processor block is checking for SD, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors exceeds that of programmed into this and the "Redundant Receive STS-3 Transport SD SET Threshold – Byte 0" register, then an SD condition will be declared.

Table 190: Redundant Receive STS-3 Transport – Receive SD SET Threshold – Byte 0 (Address Location= 0x1743)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
SD_SET_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	10	1	1

BIT NUMBER	Nаме	TYPE	DESCRIPTION
7 - 0	SD_SET_THRESHOLD[7:0]	R/W	SD_SET_THRESHOLD - LSB:
	product	or production	These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SD SET Threshold – Byte 1" registers permit the user to specify the number of B2 bit errors that will cause the Redundant Receive STS-3 TOH Processor block to declare an SD (Signal Degrade) condition. When the Redundant Receive STS-3 TOH Processor block is checking for SD, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors exceeds that of programmed into this and the "Redundant Receive STS-3 Transport SD SET Threshold – Byte 1" register, then an SD condition will be declared.

Table 191: Redundant Receive STS-3 Transport – Receive SD CLEAR Threshold – Byte 1 (Address Location= 0x1746)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SD_CLEAR_THRESHOLD[15:8]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SD_CLEAR_THRESHOLD[15:8]	R/W	SD_CLEAR_THRESHOLD - MSB:
		(S)	These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SD CLEAR Threshold – Byte 0" registers permit the user to specify the upper limit for the number of B2 bit errors that will cause the Redundant Receive STS-3 TOH Processor block to clear the SD (Signal Degrade) condition. When the Redundant Receive STS-3 TOH Processor block is checking for clearing SD, it will accumulate B2 errors for a total of 8 CLEAR Sub-Interval periods. If the number of accumulated B2 errors is less than that programmed into this and the "Redundant Receive STS-3 Transport SD CLEAR Threshold – Byte 0" register, then an SD condition will be cleared.

Table 192: Redundant Receive STS-3 Transport - Receive SD CLEAR Threshold - Byte 1 (Address Location= 0x1747)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
SD_CLEAR_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1010	1	1	1	1	1

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SD_CLEAR_THRESHOLD[7:0]	R/W	SD_CLEAR_THRESHOLD - LSB:
	***		These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SD CLEAR Threshold – Byte 1" registers permit the user to specify the upper limit for the number of B2 bit errors that will cause the Redundant Receive STS-3 TOH Processor block to clear the SD (Signal Degrade) condition.
			When the Redundant Receive STS-3 TOH Processor block is checking for clearing SD, it will accumulate B2 errors for a total of 8 CLEAR Sub-Interval periods. If the number of accumulated B2 errors is less than that programmed into this and the "Redundant Receive STS-3 Transport SD CLEAR Threshold – Byte 1" register, then an SD condition will be cleared.

Table 193: Redundant Receive STS-3 Transport – Force SEF Condition Register (Address Location= 0x174B)



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	SEF FORCE							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 1	Unused	R/O	
0	SEF FORCE	R/W	SEF Force:
			This READ/WRITE bit-field permits the user to force the Redundant Receive STS-3 TOH Processor block to declare an SEF defect. The Redundant Receive STS-3 TOH Processor block will then attempt to reacquire framing. Writing a "1" into this bit-field configures the Redundant Receive STS-3 TOH Processor block to declare the SEF defect. The Redundant Receive STS-3 TOH Processor block will automatically set this bit-field to "0" once it has reacquired framing (e.g., has detected two consecutive STS-3 frames with the correct A1 and A2 bytes).

Table 194: Redundant Receive STS-3 Transport – Receive 10 Trace Buffer Control Register (Address Location= 0x174F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
	Unused		READ SEL	ACCEPT THRD	MSG TYPE	MSG LI	ENGTH				
R/O	R/O	R/O	R/W	OR/W	R/W	R/W	R/W				
0	0	0	0	0 0	0	0	0				
	1000										

DIT NUMBER	BIT NUMBER NAME TYPE DESCRIPTION								
BII NUMBER	NAME	TYPE	DESCRIPTION						
7 – 5	Unused	R/O							
4	READ SEL	R/W	Receive Section Trace (J0) Message Buffer Read Selection:						
	\n'	Yata	This READ/WRITE bit-field permits a user to specify which of the following buffer segments to read.						
		0	k. Valid Message Buffer						
			I. Expected Message Buffer						
			0- Executing a READ to the Receive Section Trace (J0) Message Buffer, will return contents within the "Valid Message" buffer.						
			1 – Executing a READ to the Receive Section Trace (J0) Message Buffer, will return contents within the "Expected Message Buffer".						
			Note: In the case of the Redundant Receive STS-3 TOH Processor block, the "Receive J0 Trace Buffer" is located at Address location 0x1300 through 0x133F.						
3	ACCEPT THRD	R/W	Message Accept Threshold:						
			This READ/WRITE bit-field permits a user to select the number of consecutive times that the Redundant Receive STS-3 TOH Processor block must receive a given Section Trace Message, before it is accepted, as described below.						

			MSG LENGTH Resulting J0 Trace Message Length 00 1 Byte 01 16 Bytes 10/11 64 Bytes				
1 - 0	MSG LENGTH	R/W	Jo Message Length: These READ/WRITE bit-fields permit the user to specify the length of the Jo Trace Message that the Redundant Receive STS-3 TOH Processor block will receive. The relationship between the content of these bit-fields and the corresponding Jo Trace Message Length is presented below.				
			 0 – The Section Trace Message boundary is indicated by "Line Feed". 1 – The Section Trace Message boundary is indicated by the presence of a "1" in the MSB of the first byte (within the J0 Trace Message). 				
2	MSG TYPE	R/W	Message Alignment Type: This READ/WRITE bit-field permits a user to specify how the Redundant Receive STS-3 TOH Processor block will locate the boundary of the incoming Section Trace Message, as indicated below.				
			 0 – The Redundant Receive STS-3 TOH Processor block accepts the Section Message after it has received it the third time in succession. 1 – The Redundant Receive STS-3 TOH Processor block accepts the Section Message after it has received in the fifth time in succession. 				

Table 195: Redundant Receive STS-3 Transport Receive SD Burst Error Tolerance – Byte 1 (Address Location= 0x1752)

Віт 7	Віт 6	Віт 5	BIT 4	Віт 3	Віт 2	Віт 1	Віт 0			
SD_BURST_TOLERANCE[15:8]										
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
1	1	1,33	11	1	1	1	1			

BIT NUMBER	NAME (TYPE	DESCRIPTION			
7 - 0	SD_BURST TOLERANCE [15:8]	R/W	SD_BURST_TOLERANCE – MSB: These READ/WRITE bits, along with the contents of the "Redundant Receive STS-3 Transport – SD BURST Tolerance – Byte 0" registers permit the user to specify the maximum number of B2 bit errors that the Redundant Receive STS-3 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-3 frame period), when determining whether or not to declare an SD (Signal Degrade) defect condition.			
			not to declare an SD (Signal Degrade) defect condition. Note: The purpose of this feature is to permit the user to provide some level of B2 error burst filtering, when the Redundant Receive STS-3 TOH Processor block is accumulating B2 byte errors in order to declare the SD defect condition. The user can implement this feature in order to configure the Redundant Receive STS-3 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SD defect condition.			

Table 196: Redundant Receive STS-3 Transport – Receive SD Burst Error Tolerance – Byte 0 (Address Location= 0x1753)

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
SD_BURST_TOLERANCE[7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SD_BURST_ TOLERANCE [7:0]	R/W	SD_BURST_TOLERANCE – LSB: These READ/WRITE bits, along with the contents of the "Redundant Receive STS-3 Transport – SD BURST Tolerance – Byte 1" registers permit the user to specify the maximum number of B2 bit errors that the Redundant Receive STS-3 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-3 frame period), when determining whether or not to declare an SD (Signal Degrade) defect condition. Note: The purpose of this feature is to permit the user to provide some level of B2 error burst filtering, when the Redundant Receive STS-3 TOH Processor block is accumulating B2 byte errors in order to declare the SD defect condition. The user can implement this feature in order to configure the Redundant Receive STS-3 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SD defect condition.

Table 197: Redundant Receive STS-3 Transport – Receive SF Burst Error Tolerance – Byte 1 (Address Location= 0x1756)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 2	Віт 1	Віт 0			
SF_BURST_TOLERANCE[15:8]									
R/W	R/W	R/W	R/W R/W	R/W	R/W	R/W			
1	1	1	1	1	1	1			

BIT NUMBER	NAME	TYPE	10	DESCRIPTION
7 - 0	SF_BURST_ TOLERANCE [15:8]	R/WO	Thes STS spec STS perio	BURST_TOLERANCE – MSB: se READ/WRITE bits, along with the contents of the "Redundant Receive 3 Transport – SF BURST Tolerance – Byte 0" registers permit the user to be 1 the maximum number of B2 bit errors that the Redundant Receive 3 TOH Processor block can accumulate during a single Sub-Interval od (e.g., an STS-3 frame period), when determining whether or not to are an SF (Signal Failure) defect condition. e: The purpose of this feature is to permit the user to provide some level of B2 error burst filtering, when the Redundant Receive STS-3 TOH Processor block is accumulating B2 byte errors in order to declare the SF defect condition. The user can implement this feature in order to configure the Redundant Receive STS-3 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SF defect condition.

Table 198: Redundant Receive STS-3 Transport – Receive SF Burst Error Tolerance – Byte 0 (Address Location= 0x1757)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			SF_BURST_TC	DLERANCE[7:0]			



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

| R/W |
|-----|-----|-----|-----|-----|-----|-----|-----|
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

BIT NUMBER	NAME	Түре	DESCRIPTION	
7 - 0	SF_BURST_ TOLERANCE [7:0]	R/W	SF_BURST_TOLERANCE – LSB: These READ/WRITE bits, along with the contents of the "Redundant Receiv STS-3 Transport – SF BURST Tolerance – Byte 1" registers permit the user t specify the maximum number of B2 bit errors that the Redundant Receiv STS-3 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-3 frame period), when determining whether or not the declare an SF (Signal Failure) defect condition.	
			Note: The purpose of this feature is to permit the user to provide some level of B2 error burst filtering, when the Redundant Receive STS-3 TOH Processor block is accumulating B2 byte errors in order to declare the SF defect condition. The user can implement this feature in order to configure the Redundant Receive STS-3 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SF defect condition.	

Table 199: Redundant Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 2 (Address Location= 0x1759)

	, , , , , , , , , , , , , , , , , , , ,				,		
Віт 7	Віт 6	Віт 5	Віт 4	⊘В іт 3	Віт 2	Віт 1	Віт 0
		SD_C	CLEAR_MONIT	OR_WINDOW[23:16]		
R/W	R/W	R/W	RAW	R/W	R/W	R/W	R/W
1	1	1	1012	1	1	1	1
18,010 40,							

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW[23:	R/W	SD_CLEAR_MONITOR_INTERVAL - MSB:
	The progress not		These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SD Clear Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the number of STS-3 Frame periods that will constitute a CLEAR Sub-Interval for SD (Signal Degrade).
	G afte		When the Redundant Receive STS-3 TOH Processor block is checking for clearing the SD defect, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors is less than that of programmed into the "Redundant Receive STS-3 Transport SD Clear Threshold" register, then the SD defect will be cleared.

Table 200: Redundant Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 1 (Address Location= 0x175A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SD_CLEAR_MONITOR_WINDOW[15:8]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW[15:8]	R/W	SD_CLEAR_MONITOR_INTERVAL - Bits 15 through 8:
			These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SD Clear Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the number of STS-3 Frame periods that will constitute a CLEAR Sub-Interval for SD (Signal Degrade).
			When the Redundant Receive STS-3 TOH Processor block is checking for clearing the SD defect, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors is less than that of programmed into the "Redundant Receive STS-3 Transport SD Clear Threshold" register, then the SD defect will be cleared.

and and the death of the ordered and the orde

Table 201: Redundant Receive STS-3 Transport – Receive SD Clear Monitor Interval – Byte 0 (Address Location= 0x175B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	SD_CLEAR_MONITOR_WINDOW[7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
1	1	1	1	1	1	1	1			

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW[R/W	SD_CLEAR_MONITOR_INTERVAL - LSB:
	7:0]	ST	These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SD Clear Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the number of STS-3 Frame periods that will constitute a CLEAR Sub-Interval for SD (Signal Degrade). When the Redundant Receive STS-3 TOH Processor block is checking for clearing the SD defect, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors is less than that of programmed into the "Redundant Receive STS-3 Transport SD Clear Threshold" register, then the SD defect will be cleared.

Table 202: Redundant Receive STS-3 Transport Receive SF Clear Monitor Interval – Byte 2 (Address Location= 0x175D)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0			
	SF_CLEAR_MONITOR_WINDOW[23:16]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
1	1	10	e 50°	1	1	1	1			
	bighe 1 h									

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDO W [23:16]	R/W	SF_CLEAR_MONITOR_INTERVAL – MSB: These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SF Clear Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the number of STS-3 Frame periods that will constitute a CLEAR Sub-Interval for SF (Signal Failure). When the Redundant Receive STS-3 TOH Processor block is checking for clearing the SF defect, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors is less than that of programmed into the "Redundant Receive STS-3 Transport SF Clear Threshold" register, then the SF defect will be cleared.

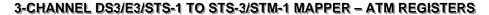




Table 203: Redundant Receive STS-3 Transport – Receive SF Clear Monitor Interval – Byte 1 (Address Location= 0x175E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	SF_CLEAR_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDOW [15:8]	R/W	SF_CLEAR_MONITOR_INTERVAL - Bits 15 through 8: These READ_WRITE bits, along the contents of the "Redundant Receive STS-3 Transport - SF Clear Monitor Interval - Byte 2 and Byte 0" registers permit the user to specify the number of STS-3 Frame periods that will constitute a CLEAR Sub-Interval for SF (Signal Failure). When the Redundant Receive STS-3 TOH Processor block is checking for clearing the SF defect, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors is less than that of programmed into the "Redundant Receive STS-3 Transport SF Clear Threshold" register, then the SF defect will be cleared.

Table 204: Redundant Receive STS-3 Transport - Receive SF Clear Monitor Interval - Byte 0 (Address Location= 0x175F)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0
SF_CLEAR_MONITOR_WINDOW[7:0]							
R/W	R/W	R/W	RW	R/W	R/W	R/W	R/W
1	1	0) (1)	J 1	1	1	1	1

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDOW	R/W	SF_CLEAR_MONITOR_INTERVAL - LSB:
	[7:0]		These READ/WRITE bits, along the contents of the "Redundant Receive STS-3 Transport – SF Clear Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the number of STS-3 Frame periods that will constitute a CLEAR Sub-Interval for SF (Signal Failure).
			When the Redundant Receive STS-3 TOH Processor block is checking for clearing the SF defect, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors is less than that of programmed into the "Redundant Receive STS-3 Transport SF Clear Threshold" register, then the SF defect will be cleared.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 205: Redundant Receive STS-3 Transport – Auto AIS Control Register (Address Location= 0x1763)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit AIS-P	Transmit AIS-P	Transmit AIS-P	Transmit AIS-P	Transmit AIS-P	Transmit AIS-P	Transmit AIS-P	Transmit AIS-P
(Down- stream) Upon J0 Message Unstable	(Down- stream) Upon J0 Message Mismatch	(Down- stream) Upon SF	(Down- stream) Upon SD	(Down- stream) upon Loss of Optical Carrier AIS	(Down- stream) upon LOF	(Down- stream) upon LOS	(Down- stream) Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

D.= M	N	T	35.0
BIT NUMBER	NAME	Түре	DESCRIPTION
7	Transmit AIS-P	R/W	Transmit Path AIS upon Detection of Unstable Section Trace (J0):
	(Down-stream) upon J0 Message Unstable		This READ/WRITE bit-field permits the user to configure the Redundant Receive STS-3 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive SONET POH Processor blocks), anytime it detects an Unstable Section Trace (JD) condition in the "incoming" STS-3 data-stream.
			0 – Does not configure the Redundant Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects an "Unstable Section Trace" condition.
			1 – Configures the Redundant Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects an "Unstable Section Trace" condition.
		Cor	Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Redundant Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
6	Transmit AIS-P (Down-stream)	R/W	Transmit Path AIS (AIS-P) upon Detection of Section Trace (J0) Message Mismatch:
	Upon J0 Message Mismatch	May	This READ/WRITE bit-field permits the user to configure the Redundant Receive STS-3 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive SONET POH Processor blocks), anytime it detects a Section Trace (J0) Message Mismatch condition in the "incoming" STS-3 data stream.
	all all		0 – Does not configure the Redundant Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects a "Section Trace Message Mismatch" condition.
			1 – Configures the Redundant Receive STS-3 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects a "Section Trace Message Mismatch" condition.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Redundant Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
5	Transmit AIS-P	R/W	Transmit Path AIS upon Signal Failure (SF):
	(Down-stream) upon SF		This READ/WRITE bit-field permits the user to configure the Redundant Receive STS-3 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			SONET POH Processor blocks), anytime it declares an SF condition.
			0 - Does not configure the Redundant Receive STS-3 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the SF defect.
			1 - Configures the Redundant Receive STS-3 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the SF defect.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Redundant Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
4	Transmit AIS-P	R/W	Transmit Path AIS upon Signal Degrade (SD):
	(Down-stream) upon SD		This READ/WRITE bit-field permits the user to configure the Redundant Receive STS-3 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive SONET POH Processor blocks), anytime it declares an SD condition.
			0 – Does not configure the Redundant Receive STS-3 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the SD defect.
			1 – Configures the Redundant Receive STS-3 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the SD defect.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Redundant Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
3	Transmit AIS-P	R/W	Transmit Path AIS upon Loss of Optical Carrier condition:
	(Down-stream) upon Loss of Optical Carrier	, ct	This READ/WRITE bit-field permits the user to configure the Redundant Receive STS-3 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive SONET POH Processor blocks), anytime it detects a "Loss of Optical Carrier" condition.
	or	odive	0 – Does not configure the Redundant Receive STS-3 TOH Processor block to transmit the AIS-P indicator upon detection of a "Loss of Optical Carrier" condition.
	The	SOM	Configures the Redundant Receive STS-3 TOH Processor block to transmit the AIS-P indicator upon detection of a "Loss of Optical Carrier" condition.
		ØI.	Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Redundant Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.

	T T		
2	Transmit AIS-P (Down-stream) upon	R/W	Transmit Path AIS upon Loss of Frame (LOF):
	LOF		This READ/WRITE bit-field permits the user to configure the Redundant Receive STS-3 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive SONET POH Processor block), anytime it declares an LOF condition.
			0 – Does not configure the Redundant Receive STS-3 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the LOF defect.
			1 - Configures the Redundant Receive STS-3 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the LOF defect.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Redundant Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
1	Transmit AIS-P	R/W	Transmit Path AIS upon Loss of Signal (LOS):
	(Down-stream) upon LOS		This READ/WRITE bit-field permits the user to configure the Redundant Receive STS-3 TOB Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive SONET POH Processor block), anytime it declares an LOS condition.
			0 – Does not configure the Redundant Receive STS-3 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) anytime it declares the LOS defect.
			1 - Configures the Redundant Receive STS-3 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) anytime it declares the LOS defect.
		ct or	Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Redundant Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
0	Transmit AIS-P	R/W	Automatic Transmission of AIS-P Enable:
	(Down-stream) Enable	\O(This READ/WRITE bit-field serves two purposes.
	Thedatas	May	It permits the user to configure the Redundant Receive STS-3 TOH Processor block to automatically transmit the Path AIS (AIS-P) indicator, via the down-stream traffic (e.g., towards the Receive SONET POH Processor blocks), upon detection of an SF, SD, Section Trace Mismatch, Section Trace Unstable, LOF, LOS or Loss of Optical Carrier conditions.
			It also permits the user to configure the Redundant Receive STS-3 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive SONET POH Processor blocks) anytime it detects an AIS-L condition in the "incoming " STS-3 data-stream.
			0 - Configures the Redundant Receive STS-3 TOH Processor block to NOT automatically transmit the AIS-P indicator (via the "downstream" traffic) upon detection of the AIS-L or any of the "above-mentioned" conditions.
			1 – Configures the Redundant Receive STS-3 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) upon detection of any of the "above-mentioned" condition.
			Note: The user must also set the corresponding bit-fields (within this

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

	register) to "1" in order to configure the Redundant Receive STS-3 TOH Processor block to automatically transmit the AIS-P
	indicator upon detection of a given alarm/defect condition.

Table 206: Redundant Receive STS-3 Transport – Serial Port Control Register (Address Location= 0x1767)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused				RxTOH_CLOCK_SPEED[7:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

7 - 4 Unused R/O 3 - 0 RxTOH_CLOCK_SPEED[7:0] R/W RxTOHClk Output Clock Signal Speed: These READ/WRITE bit-fields permit the user to specify the frequency of the "RxTOHClk output clock signal. The formula that relates the contents of these register bits to the "RxTOHClk" frequency is presented below. FREQ = 19.44 /[2 * (RxTOH_CLOCK_SPEED + 1)	BIT NUMBER	NAME	Түре	DESCRIPTION
These READ/WRITE bit-fields permit the user to specify the frequency of the "RxTOHCIk output clock signal. The formula that relates the contents of these register bits to the "RxTOHCIk" frequency is presented below. FREQ = 19.44/[2 * (RxTOH_CLOCK_SPEED + 1)		Unused	R/O	athir tree
RXTOPICIK output signal must be in the range of 0.6075MHz to 9.72MHz	3 - 0			These READ/WRITE bit fields permit the user to specify the frequency of the "RxTOHClk output clock signal. The formula that relates the contents of these register bits to the "RxTOHClk" frequency is presented below. FREQ = 19.44 /[2* (RxTOH_CLOCK_SPEED + 1)

Table 207: Redundant Receive STS-3 Transport – Auto AIS (in Downstream STS-1s) Control Register (Address Location= 0x176B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Unused	Transmit AIS-P (via Downstream STS-1s) upon LOS	Transmit AIS-P (via Downstream STS-1s) upon LOF	Transmit AIS-P (via Downstream STS-1s) upon SD	Transmit AIS-P (via Downstream STS-1s) upon SF	AIS-L Output Enable	Transmit AIS-P (via Downstream STS-1s) Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

		T	49 0
BIT Number	Name	TYPE	DESCRIPTION
7 - 6	Unused	R/O	dillact
5	Transmit AIS-P (via Downstream STS-1s) upon LOS	R/W	Transmit AIS-P (via Downstream STS-1s) upon LOS (Loss of Signal): This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor blocks (in each channel) to automatically transmit the AIS-P (Rath AIS) Indicator via the "downstream" STS-1 signals, anytime the Redundant Receive STS-3 TOH Processor block declares the LOS defect. 0 - Does not configure all "activated" Transmit STS-1 POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Redundant Receive STS-3 TOH Processor block declares the LOS defect. 1 Configures all "activated" Transmit STS-1POH Processor block declares the LOS defect. 1 Configures all "activated" Transmit STS-1POH Processor block declares the LOS defect. Note: 1. In the "long-run" the function of this bit-field is exactly the same as that of Bit 1 (Transmit AIS-P Down-stream - Upon LOS), within the Redundant Receive STS-3 Transport - Auto AIS Control Register (Address Location= 0x1763). The only difference is that this register bit will cause each of the "downstream" Transmit STS-1 POH Processor blocks to IIMMEDIATELY begin to transmit the AIS-P condition whenever the Redundant Receive STS-3 TOH Processor block declares the LOS defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the NE declaring the LOS defect. 2. In the case of Bit 1 (Transmit AIS-P Downstream - Upon LOS), several SONET frame periods are required (after the Redundant Receive STS-3 TOH Processor block has declared the LOS defect), before the Transmit STS-1 POH Processor blocks will begin the process of transmitting the AIS-P indicators. 3. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STS-1s Enable) within this register, in order enable this feature.
4	Transmit AIS-P (via Downstream STS-1s) upon LOF	R/W	Transmit AIS-P (via Downstream STS-1s) upon LOF (Loss of Frame):

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

	This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor blocks (in each channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signals, anytime the Redundant Receive STS-3 TOH Processor block declares the LOF defect.
	 0 – Does not configures all "activated" Transmit STS-1 POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Redundant Receive STS-3 TOH Processor block declares the LOF defect.
	1 – Configures all "activated" Transmit STS-1POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Redundant Receive STS-3 TOH Processor block declares the LOF defect.
	Note:
	1. In the "long-run" the function of this bit-field is exactly the same as that of Bit 2 (Transmit AIS-P Down-stream – Upon LOF), within the Redundant Receive STS-3 Transport – Auto AIS Control Register (Address Location= 0x1763). The only difference is that this register bit will cause each of the "downstream" Transmit STS-1 POH Processor blocks to IMMEDIATELY begin to transmit the AIS-P condition whenever the Redundant Receive STS-3 TOH Processor block declares the LOF defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the NE declaring the LOF defect.
	2. In the case of Bit 2 (Transmit AIS-P Downstream – Upon LOF), several SONET frame periods are required (after the Redundant Receive STS-3 TOH Processor block has declared the LOS defect), before the Transmit STS-1 POH Processor blocks will begin the process of transmitting the AIS-P indicators.
	3. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STS-1s Enable) within this register, in order enable this feature.
3 Transmit AIS-P (v	
Downstream STS- upon SD	This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor blocks (in each channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signals, anytime the Redundant Receive STS-3 TOH Processor block declares the SD defect.
	0 – Does not configures all "activated" Transmit STS-1 POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Redundant Receive STS-3 TOH Processor block declares the SD defect.
	1 – Configures all "activated" Transmit STS-1POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Redundant Receive STS-3 TOH Processor block declares the SD defect.
	Note:
	1.In the "long-run" the function of this bit-field is exactly the same as that of Bit 4 (Transmit AIS-P Down-stream – Upon SD), within the Redundant Receive STS-3 Transport – Auto AIS Control Register (Address Location= 0x1763). The only difference is that this register bit will cause each of the "downstream" Transmit STS-1 POH Processor blocks to IMMEDIATELY begin to transmit the AIS-P condition whenever the Redundant Receive STS-3 TOH Processor block declares the SD defect. This will permit the user to easily comply with the Telcordia GR-253-
	CORE requirements of an NE transmitting the AIS-P indicator

			downstream within 125us of the NE declaring the LOS defect.
			2. In the case of Bit 1 (Transmit AIS-P Downstream – Upon LOF), several SONET frame periods are required (after the Redundant Receive STS-3 TOH Processor block has declared the SD defect), before the Transmit STS-1 POH Processor blocks will begin the process of transmitting the AIS-P indicators.
			3. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STS-1s Enable) within this register, in order enable this feature.
2	Transmit AIS-P (via	R/W	Transmit AIS-P (via Downstream STS-1s) upon Signal Failure (SF):
	Downstream STS-1s) upon SF		This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor blocks (in each channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signals, anytime the Redundant Receive STS-3 TOH Processor block declares an SF condition.
			0 – Does not configures all "activated" Transmit STS-1 POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Redundant Receive STS-3 TOH Processor block declares the SF defect.
			1 – Configures all "activated" Transmit STS-1POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Redundant Receive STS-3 TOH Processor block declares the SP defect.
			Note:
		10,00	1. In the "long-run" the function of this bit-field is exactly the same as that of Bit 5 (Transmit AIS-P Down-stream – Upon SF), within the Redundant Receive STS-3 Transport – Auto AIS Control Register (Address Location= 0x1763). The only difference is that this register bit will cause each of the "downstream" Transmit STS-1 POH Processor blocks to IMMEDIATELY begin transmit the AIS-P condition whenever the Redundant Receive STS-3 TOH Processor block declares the SF defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the NE declaring the SF defect.
	The process	W TRAY	2 In the case of Bit 5 (Transmit AIS-P Downstream – Upon SF), several SONET frame periods are required (after the Redundant Receive STS-3 TOH Processor block has declared the SF defect), before the Transmit STS-1 POH Processor blocks will begin the process of transmitting the AIS-P indicators.
	, go suc		3. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STS-1s Enable) within this register, in order enable this feature.
1	AIS-L Output Enable	R/W	AIS-L Output Enable:
			This READ/WRITE bit-field, along with Bits 7 (8kHz or STUFF Out Enable) within the "Operation Output Control Register – Byte 1" (Address Location= 0x0150) permit the user to configure the "AIS-L" indicator to be output via the "LOF" output pin (pin AD11).
			If Bit 7 (within the "Operation Output Control Register – Byte 1") is set to "0", then setting this bit-field to "1" configures pin AD11 to function as the AIS-L output indicator.
			If Bit 7 (within the "Operation Output Control Register – Byte 1") is set to "0", then setting this bit-field to "0" configures pin AD11 to function as the LOF output indicator.
			If Bit 7 (within the "Operation Output Control Register – Byte 1) is set to

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			"1", then this register bit is ignored.
0	Downstream STS-1s)	Downstream STS-1s)	Automatic Transmission of AIS-P (via the downstream STS-1s) Enable:
	Enable		This READ/WRITE bit-field permits the user to configure all "activated" Transmit STS-1 POH Processor blocks to automatically transmit the AIS-P indicator, via its "outbound" STS-1 signals, upon detection of an SF, SD, LOS and LOF condition.
			0 – Does not configure the "activated" Transmit STS-1 POH Processor blocks to automatically transmit the AIS-P indicator, whenever the Redundant Receive STS-3 TOH Processor block declares either the LOS, LOF, SD or SF defects.
			1 – Configures the "activated" Transmit STS-1 POH Processor blocks to automatically transmit the AIS-P indicator, whenever the Redundant Receive STS-3 TOH Processor block declares either the LOS, LOF, SD or SF defects.

mit indice indic

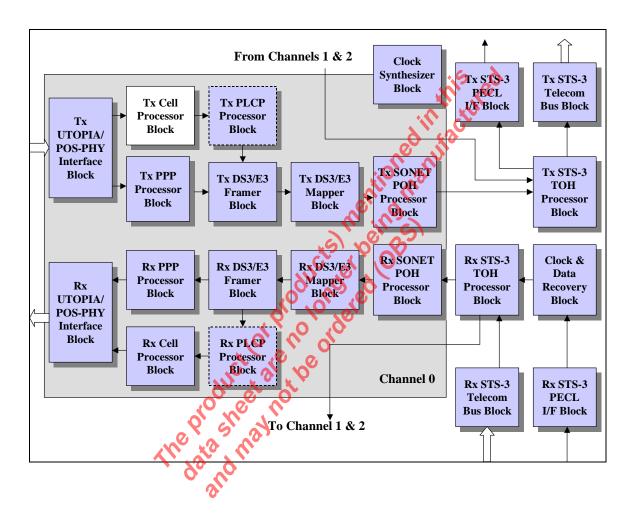
1.8 TRANSMIT ATM CELL PROCESSOR BLOCK

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

The register map for the Transmit ATM Cell Processor Block is presented in the Table below. Additionally, a detailed description of each of the "Transmit ATM Cell Processor" block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33 device, with the "Transmit ATM Cell Processor Blocks "highlighted" is presented below in Figure 9.

Figure 9: Illustration of the Functional Block Diagram of the XRT94L33 device, with the Transmit ATM Cell Processor Block "High-lighted".



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS



1.8.1 TRANSMIT ATM CELL PROCESSOR BLOCK REGISTER

Table 208: Transmit ATM Cell Processor Block Register Address Map

	TRANSMIT ATM CELL PROCESSOR/ PPP PROCESSOR BLOCK REGISTERS						
Note: N repres	sents the "Channel Number" and ranges in value from 0x02 to 0x04						
0xNF00	Transmit ATM Cell Processor Control Register – Byte 3	0x00					
0xNF01	Transmit ATM Cell Processor Control Register – Byte 2 0x00						
0xNF02	Transmit ATM Cell Processor Control Register – Byte 1	0x00					
0xNF03	Transmit ATM Cell/PPP Processor Control Register – Byte 0	0x00					
0xNF04	Transmit ATM Status Register	0x00					
0xNF05 – 0xNF0A	Reserved	0x00					
0xNF0B	Transmit ATM Cell/PPP Processor Interrupt Status Register	0x00					
0xNF0C – 0xNF0E	Reserved	0x00					
0xNF0F	Transmit ATM Cell/PPP Processor Interrupt Enable Register	0x00					
0xNF10 – 0xNF12	Reserved	0x00					
0xNF13	Transmit ATM Cell Insertion/Extraction Memory Control Register	0x00					
0xNF14	Transmit ATM Cell Insertion/Extraction Memory - Byte 3	0x00					
0xNF15	Transmit ATM Cell Insertion/Extraction Memory – Byte 2	0x00					
0xNF16	Transmit ATM Cell Insertion/Extraction Memory – Byte 1	0x00					
0xNF17	Transmit ATM Cell Insertion/Extraction Memory – Byte 0	0x00					
0xNF18	Transmit ATM Cell Idle Cell Header Byte # 1 Register	0x00					
0xNF19	Transmit ATM Cell - Idle Cell Header Byte # 2 Register	0x00					
0xNF1A	Transmit ATM Cell - Idle Cell Header Byte # 3 Register	0x00					
0xNF1B	Transmit ATM Cell - Idle Cell Header Byte # 4 Register	0x00					
0xNF1C – 0xNF1E	Reserved	0x00					
0xNF1F	Transmit ATM Cell – Idle Cell Payload Byte Register	0x00					
0xNF20	Transmit ATM Cell – Test Cell Header Byte # 1 Register	0x00					
0xNF21	Transmit ATM Cell – Test Cell Header Byte # 2 Register	0x00					
0xNF22	Transmit ATM Cell – Test Cell Header Byte # 3 Register	0x00					
0xNF23	Transmit ATM Cell – Test Cell Header Byte # 4 Register	0x00					
0xNF24 – 0xNF27	Reserved	0x00					
0xNF28	Transmit ATM Cell – Cell Count Register – Byte 3	0x00					

0xNF29	Transmit ATM Cell – Cell Count Register – Byte 2	0x00
0xNF2A	Transmit ATM Cell – Cell Count Register – Byte 1	0x00
0xNF2B	Transmit ATM Cell – Cell Count Register – Byte 0	0x00
0xNF2C	Transmit ATM Cell – Discard Cell Count Register – Byte 3	0x00
0xNF2D	Transmit ATM Cell – Discard Cell Count Register – Byte 2	0x00
0xNF2E	Transmit ATM Cell – Discard Cell Count Register – Byte 1	0x00
0xNF2F	Transmit ATM Cell – Discard Cell Count Register – Byte 0	0x00
0xNF30	Transmit ATM Cell – HEC Byte Error Count Register – Byte 3	0x00
0xNF31	Transmit ATM Cell – HEC Byte Error Count Register – Byte 2	0x00
0xNF32	Transmit ATM Cell – HEC Byte Error Count Register – Byte 1	0x00
0xNF33	Transmit ATM Cell – HEC Byte Error Count Register - Byte 0	0x00
0xNF34	Transmit ATM Cell – Parity Error Count Register Byte	0x00
0xNF35	Transmit ATM Cell – Parity Error Count Register – Byte 2	0x00
0xNF36	Transmit ATM Cell – Parity Error Count Register – Byte 1	0x00
0xNF37	Transmit ATM Cell – Parity Error Count Register – Byte 0	0x00
0xNF38 – 0xNF42	Reserved	0x00
0xNF43	Transmit ATM Controller – Transmit ATM Filter # 0 Control Register	0x00
0xNF44	Transmit ATM Controller Transmit ATM Filter # 0 Pattern – Header Byte 1	0x00
0xNF45	Transmit ATM Controller - Transmit ATM Filter # 0 Pattern - Header Byte 2	0x00
0xNF46	Transmit ATM Controller - Transmit ATM Filter # 0 Pattern - Header Byte 3	0x00
0xNF47	Transmit ATM Controller - Transmit ATM Filter # 0 Pattern - Header Byte 4	0x00
0xNF48	Transmit ATM Controller - Transmit ATM Filter # 0 Check - Header Byte 1	0x00
0xNF49	Transmit ATM Controller – Transmit ATM Filter # 0 Check – Header Byte 2	0x00
0xNF4A	Transmit ATM Controller – Transmit ATM Filter # 0 Check – Header Byte 3	0x00
0xNF4B	Transmit ATM Controller – Transmit ATM Filter # 0 Check – Header Byte 4	0x00
0xNF4C	Transmit ATM Cell – Cell Count Register – Byte 3	0x00
0xNF4D	Transmit ATM Cell – Cell Count Register – Byte 2	0x00
0xNF4E	Transmit ATM Cell – Cell Count Register – Byte 1	0x00
0xNF4F	Transmit ATM Cell – Cell Count Register – Byte 0	0x00
0xNF50 – 0xNF52	Reserved	0x00
0xNF53	Transmit ATM Controller – Transmit ATM Filter # 1 Control Register	0x00
0xNF54	Transmit ATM Controller – Transmit ATM Filter # 1 Pattern – Header Byte 1	0x00

XRT94L33

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS



0xNF55	Transmit ATM Controller – Transmit ATM Filter # 1 Pattern – Header Byte 2	0x00
0xNF56	Transmit ATM Controller – Transmit ATM Filter # 1 Pattern – Header Byte 3	0x00
0xNF57	Transmit ATM Controller – Transmit ATM Filter # 1 Pattern – Header Byte 4	0x00
0xNF58	Transmit ATM Controller – Transmit ATM Filter # 1 Check – Header Byte 1	0x00
0xNF59	Transmit ATM Controller – Transmit ATM Filter # 1 Check – Header Byte 2	0x00
0xNF5A	Transmit ATM Controller – Transmit ATM Filter # 1 Check – Header Byte 3	0x00
0xNF5B	Transmit ATM Controller – Transmit ATM Filter # 1 Check – Header Byte 4	0x00
0xNF5C	Transmit ATM Cell – Cell Count Register - Byte 3	0x00
0xNF5D	Transmit ATM Cell – Cell Count Register – Byte 2	0x00
0xNF5E	Transmit ATM Cell – Cell Count Register – Byte 1	0x00
0xNF5F	Transmit ATM Cell – Cell Count Register – Byte 0	0x00
0xNF60 – 0xNF62	Reserved	0x00
0xNF63	Transmit ATM Controller – Transmit ATM Filter # 2 Control Register	0x00
0xNF64	Transmit ATM Controller – Transmit ATM Filter# 2 Pattern – Header Byte 1	0x00
0xNF65	Transmit ATM Controller – Transmit ATM Filter #2 Pattern – Header Byte 2	0x00
0xNF66	Transmit ATM Controller – Transmit ATM Filter # 2 Pattern – Header Byte 3	0x00
0xNF67	Transmit ATM Controller – Transmit ATM Filter # 2 Pattern – Header Byte 4	0x00
0xNF68	Transmit ATM Controller – Transmit ATM Filter # 2 Check – Header Byte 1	0x00
0xNF69	Transmit ATM Controller - Transmit ATM Filter # 2 Check - Header Byte 2	0x00
0xNF6A	Transmit ATM Controller - Transmit ATM Filter # 2 Check - Header Byte 3	0x00
0xNF6B	Transmit ATM Controller Transmit ATM Filter # 3 Check – Header Byte 4	0x00
0xNF6C	Transmit ATM cell - cell Count Register - Byte 3	0x00
0xNF6D	Transmit ATM Cell - Cell Count Register - Byte 2	0x00
0xNF6E	Transmit ATM cell - Cell Count Register - Byte 1	0x00
0xNF6F	Transmit ATM Cell- Cell Count Register – Byte 0	0x00
0xNF70 – 0xNF72	Reserved	0x00
0xNF73	Transmit ATM Controller – Transmit ATM Filter # 3 Control Register	0x00
0xNF74	Transmit ATM Controller – Transmit ATM Filter # 3 Pattern – Header Byte 1	0x00
0xNF75	Transmit ATM Controller – Transmit ATM Filter # 3 Pattern – Header Byte 2	0x00
0xNF76	Transmit ATM Controller – Transmit ATM Filter # 3 Pattern – Header Byte 3	0x00
0xNF77	Transmit ATM Controller – Transmit ATM Filter # 3 Pattern – Header Byte 4	0x00
0xNF78	Transmit ATM Controller – Transmit ATM Filter # 3 Check – Header Byte 1	0x00

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

0xNF79	Transmit ATM Controller – Transmit ATM Filter # 3 Check – Header Byte 2	0x00
0xNF7A	Transmit ATM Controller – Transmit ATM Filter # 3 Check – Header Byte 3	0x00
0xNF7B	Transmit ATM Controller – Transmit ATM Filter # 3 Check – Header Byte 4	0x00
0xNF7C	Transmit ATM Cell – Cell Count Register – Byte 3	0x00
0xNF7D	Transmit ATM Cell – Cell Count Register – Byte 2	0x00
0xNF7E	Transmit ATM Cell – Cell Count Register – Byte 1	0x00
0xNF7F	Transmit ATM Cell – Cell Count Register – Byte 0	0x00
0xNF80 – 0xN102	Reserved	0x00

The product are no ordered (OBS)

The product are no be ordered (OBS)



1.8.2 TRANSMIT ATM CELL PROCESSOR BLOCK REGISTER DESCRIPTION

Table 209: Transmit ATM Cell Processor Block – Transmit ATM Control Register – Byte 3 (Address = 0xNF00)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unt	used						

Table 210: Transmit ATM Cell Processor Block – Transmit ATM Control Register – Byte 2 (Address = 0xNF01)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт1	Віт 0
	Unused					ctill	Transmit ATM Cell Processor Enable
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	(0)	0	0
					All Vo.		

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 1	Unused	R/O	mein's)
0	Transmit ATM Cell Processor Enable	R/W	Transmit ATM Cell Processor Block Enable: This READ/WRITE bit-field permits the user to either enable or disable the Transmit ATM Cell Processor block. If the user wishes to operate a given Channel in the ATM Mode, then he/she must enable the Transmit ATM Cell Processor Block. 0 – Disables the Transmit ATM Cell Processor Block 1 Enables the Transmit ATM Cell Processor Block Note: The user must set this bit-field to "1" before he/she begins to write ATM cell data into the Transmit UTOPIA Interface block.
	7	>	

Table 211: Transmit ATM Cell Processor Block – Transmit ATM Control Register – Byte 1 (Address = 0xNF02)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Test Cell Transmit Mode Enable	ONE SHOT MODE	GFC Insertion Enable - Bit 3	GFC Insertion Enable – Bit 2	GFC Insertion Enable – Bit 1	GFC Insertion Enable – Bit 0	COSET Polynomial Addition	Regenerate HEC Byte Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Test Cell Transmit Mode Enable	R/W	Test Cell Transmit Mode Enable: This READ/WRITE bit-field permits the user to enable the Test Cell Transmitter (within the Transmit ATM Cell Processor Block). The user must implement this configuration option in order to perform diagnostic operations with Test Cells: 0 – Disables the Test Cell Transmitter. 1 – Enables the Test Cell Transmitter. Notes: For normal operation, the user should set this bit-field to "1".
6	One Shot Mode	R/W	One Shot Mode: If the user has enabled the Test Cell Transmitter, then this READ/WRITE bit-field permits the user to either configure the Test Cell Transmitter into the "One-Shot" or in the "Continuous" Mode. If the user configures the Test Cell Transmitter into the "One-Shot" Mode, then (whenever the user implements a "0 to 1" transition within Bit Y [Test Cell Transmit Mode Enable] of this register) then the Test Cell Transmitter will generate and transmit 1024 test cells. Afterwards, the Test Cell Transmitter will halt its transmission of Test Cells until the user implements another "0 to 1 transition" within Bit 7 (Test Cell Transmit Mode Enable) within this register. If the user configures the Test Cell Transmitter into the "Continuous" Mode, then the Test Cell Transmitter will continuously generate and transmit test cells for the duration that Bit 7(Test Cell Transmit Mode Enable) is set to "1". 0 - Configures the Test Cell Transmitter to operate in the "Continuous" Mode. 1 - Configures the "Test Cell Transmitter" to operate in the "One-Shot" Mode.
5	GFC Insertion Enable – Bit 3	R/W	
4	GFC Insertion Enable – Bit 2	R/W	
3	GFC Insertion Enable – Bit 1	R/W	
2	GFC Insertion Enable – Bit 0	R/W	
1	COSET Polynomial Addition	R/W	COSET Polynomial Addition: This READ/WRITE bit-field permits the user to configure the Transmit ATM Cell Processor block to modulo-add the COSET Polynomial (e.g., x^6 + x^4 + x^2 + 1) to the HEC byte value, within each "outbound"

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			ATM cell.
			0 - Configures the Transmit ATM Cell Processor block to NOT modulo-add the COSET Polynomial to the HEC byte within each outbound ATM cell.
			1 – Configures the Transmit ATM Cell Processor block to modulo-add the COSET Polynomial to the HEC byte within each outbound ATM cell.
0	Regenerate HEC	R/W	Regenerate HEC Byte Enable:
	Byte Enable		This READ/WRITE bit-field permits the user to configure the Transmit ATM Cell Processor block to automatically re-compute and insert a new HEC byte into each ATM cell (that it receives from the Transmit UTOPIA Interface block) that contains an uncorrectable HEC byte.
			0 – Does not configure the Transmit ATM Cell Processor block to compute and insert a new HEC byte into ATM cells that contains an "uncorrectable" HEC Byte error.
			1 – Configures the Transmit ATM Cell Processor block to compute and insert a new HEC byte into ATM cells that contains an "uncorrectable" HEC Byte error.
	Thepa	oduct los and mai	insert a new HEC byte into ATM cells that contains an "uncorrectable" HEC Byte error.

Table 212: Transmit ATM Cell Processor Block – Transmit ATM Control – Byte 0 (Address = 0xNF03)

В	т 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
l l	C Byte vert	HEC Byte Check Enable	Transmit UTOPIA Parity Check Enable	Transmit UTOPIA Parity Error – Discard	Transmit UTOPIA – ODD Parity	Reserved		Scrambler Enable
R	R/W	R/W	R/W	R/W	R/W	R/O	R/O	R/W
	0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	Description
7	HEC Byte Invert	R/W	HEC Byte Invert:
6	HEC Byte Check Enable	R/W	HEC Byte Check Enable. This READ/WRITE bit-field permits the user to configure the Transmit ATM Cell Processor block to perform HEC byte checking of all ATM cells that it receives via the Transmit UTOPIA Interface block. 0 — Configures the Transmit ATM Cell Processor block to NOT perform HEC byte checking on all ATM cells that it receives via the Transmit UTOPIA Interface block. 1 — Configures the Transmit ATM Cell Processor block to perform HEC byte checking on all ATM cells that it receives via the Transmit UTOPIA Interface block.
5	Transmit UTOPIA Parity Check Enable	R/W die lo	Transmit UTOPIA Parity Check Enable: This READ/WRITE bit-field permits the user to either enable or disable "Transmit UTOPIA Interface" Parity checking. If the user enables "Transmit UTOPIA Interface" Parity Checking, then the Transmit ATM Cell Processor block will compute either the EVEN or ODD parity value (depending upon the setting of Bit 3 within this register) of each byte or 16-bit word that is input via the Transmit UTOPIA Data Bus input pins: (TxUData[15:0]). Afterwards, the Transmit ATM Cell Processor block will compare this "locally computed" parity value with that which the ATM Layer Processor has provided to the "TxUPrty" input pin. If the Transmit ATM Cell Processor detects any discrepancies between these two parity values (e.g., any parity errors) then it will take action based upon the user's settings for Bit 4 (Transmit UTOPIA Parity Error – Discard). 0 – Disables "Transmit UTOPIA Interface" Parity Checking.
4	Transmit UTOPIA Parity Error - Discard	R/W	Transmit UTOPIA Parity Error – Discard Cell: This READ/WRITE bit-field permits the user to configure the Transmit ATM Cell Processor block to either discard or retain (for further processing) any ATM cell that contains a "Transmit UTOPIA Interface" parity error. 0 – Configures the Transmit ATM Cell Processor block to retain (for further processing) all cells that contain "Transmit UTOPIA Interface" parity errors. 1 – Configures the Transmit ATM Cell Processor block to discard all cells that contain "Transmit UTOPIA Interface" parity errors.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			Notes: This bit-field is only valid if "Transmit UTOPIA Interface" Parity Checking has been enabled.					
3	Transmit UTOPIA – Odd Parity	R/W	Transmit UTOPIA Parity Value – ODD Parity: This READ/WRITE bit-field permits the user to configure the Transmit ATM Cell Processor block to compute either the EVEN or ODD parity value for each byte or 16-bit word within each cell that it processes. Each of these parity values will ultimately be compared with the value that is input via the "TxUPrty" input pin (on the Transmit UTOPIA Interface block) coincident to when ATM cell data is being applied to the "TxUData[15:0]" input pins. 0 – Configures the Transmit ATM Cell Processor block to compute and verify the EVEN Parity value of each byte (or 16-bit word) of ATM cell data that it processes. 1 – Configures the Transmit ATM Cell Processor block to compute and verify the ODD Parity value of each byte (or 16-bit word) of ATM cell data that it processes. Notes: This bit-field is only value if "Transmit UTOPIA Interface" Parity Checking has been enabled.					
2 - 1	Reserved	R/O	net nut					
0	Scrambler Enable	70	Cell Payload Scrambler Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Cell Payload Scrambler". If the user enables the "Cell Payload Scrambler" then the Transmit ATM Cell Processor will payload self-synchronous scrambling on all cell payloads bytes (within each outbound ATM cell) with the x^43+1 polynomial. O-Disables the Cell Payload Scrambler I - Enables the Cell Payload Scrambler					
	(within each outbound ATM cell) with the x*43+1 polynomial. 0 - Disables the Cell Payload Scrambler 1 - Enables the Cell Payload Scrambler							

Table 213: Transmit ATM Cell Processor Block – Transmit ATM Status Register (Address = 0xNF04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	One Shot DONE						
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 1	Unused	R/O	
0	One Shot DONE	R/O	One Shot DONE:
			This READ-ONLY bit-field indicates whether or not the Test Cell Transmitter has completed its transmission of 1024 test cells, following the instant that the user has commanded the Test Cell to transmit this burst of 1024 cells.
			0 - Indicates that the Test Cell Transmitter has NOT completed its transmission of 1024 test cells
			1 – Indicates that the Test Cell Transmitter has completed its transmission of 1024 test cells since the last "Transmit Test Cell – One Shot" command.
			Notes:
			 This bit-field is only valid if (1) the Test Cell Transmitter is active and (2) if the Test Cell Transmitter has been configured to operate in the "One-Shot" Mode. Once this bit-field has been set to "1", it will remain at "1" until the user executes another "Transmit Test Cell – One Shot" command.
	The production	ct or o	2. Once this bit-field has been set to "1", it will remain at "1" until the user executes another "Transmit Test Cell – One Shot" command.

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 214: Transmit ATM Cell Processor Block – Transmit ATM Interrupt Status Register (Address = 0xNF0B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused		Transmit Cell Extraction Interrupt Status	Transmit Cell Insertion Interrupt Status	Transmit Cell Extraction Memory Overflow Interrupt Status	Transmit Cell Insertion Memory Overflow Interrupt Status	Detection of HEC Byte Error Interrupt Status	Detection of Transmit UTOPIA Parity Error Interrupt Status
R/O	R/O	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 6	Unused	R/O	ath ure
5	Transmit Cell	RUR	Transmit Cell Extraction Interrupt Status:
	Extraction Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Transmit Cell Extraction" interrupt has occurred since the last read of this register.
			The Transmit ATM Cell Processor block will generate the "Transmit Cell Extraction" Interrupt anytime it receives an incoming ATM cell (from the TxFIFO) and loads an ATM cell into the "Extraction Memory" Buffer.
			0 - Indicates that the "Transmit Cell Extraction" Interrupt has NOT occurred since the last read of this register.
			1 - Indicates that the "Transmit Cell Extraction" Interrupt has occurred since the last read of this register.
4	Transmit Cell	RUR	Transmit Cell Insertion Interrupt
	Insertion Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Transmit Cell Insertion" interrupt has occurred since the last read of this register.
		odulee	The Transmit ATM Cell Processor block will generate the "Transmit Cell Insertion" Interrupt anytime a cell (residing in the Transmit Cell Insertion Buffer) is read out of the "Transmit Cell Insertion Buffer" and is loaded into the outbound ATM cell traffic.
	The	o Mi	0 – Indicates that the "Transmit Cell Insertion" Interrupt has NOT occurred since the last read of this register.
		diffe	1 – Indicates that the "Transmit Cell Insertion" Interrupt has occurred since the last read of this register.
3	Transmit Cell	RUR	Transmit Cell Extraction Memory Overflow Interrupt Status:
	Extraction Memory Overflow Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Transmit Cell Extraction Memory Overflow" Interrupt has occurred since the last read of this register.
			The Transmit ATM Cell Processor block will generate this interrupt anytime an overflow event has occurred in the "Transmit Cell Extraction Memory" Buffer.
			0 – Indicates that the Transmit ATM Cell Processor block has NOT declared the "Transmit Cell Extraction Memory Overflow" Interrupt since the last read of this register.
			1 – Indicates that the Transmit ATM Cell Processor block has declared the "Transmit Cell Extraction Memory Overflow" interrupt since the last

	T		road of this register
			read of this register.
2	Transmit Cell Insertion Memory	RUR	Transmit Cell Insertion Memory Overflow Interrupt Status:
	Overflow Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the Transmit Cell Insertion Memory Overflow" Interrupt has occurred since the last read of this register.
			The Transmit ATM Cell Processor block will generate this interrupt anytime an overflow event has occurred in the "Transmit Cell Insertion Memory" Buffer.
			0 – Indicates that the Transmit ATM Cell Processor block has NOT declared the "Transmit Cell Insertion Memory Overflow" interrupt since the last read of this register.
			1 – Indicates that the Transmit ATM Cell Processor block has declared the "Transmit Cell Insertion Memory Overflow" interrupt since the last read of this register.
1	Detection of HEC	RUR	Detection of HEC Byte Error Interrupt:
	Byte Error Interrupt		This RESET-upon-READ bit-field indicates whether or not the "Transmit ATM Cell Processor block" has declared the "Detection of HEC Byte Error" Interrupt since the last read of this register.
			The Transmit ATM Cell Processor block will generate this interrupt anytime it has received an ATM cell (from the TxFIFO) that contains a HEC byte error.
			0 - Indicates that the Transmit ATM Cell Processor block has NOT declared the "Detection of HEC Byte Error" Interrupt since the last read of this register.
			1 - Indicates that the Transmit ATM Cell Processor block has declared the "Detection of HEC Byte Error" Interrupt since the last read of this register.
0	Detection of Transmit	16	Detection of Transmit UTOPIA Parity Error Interrupt:
	UTOPIA Parity Error Interrupt	it ar	This RESET-upon-READ bit-field indicates whether or not the "Transmit ATM Cell Processor" block has declared the "Detection of Transmit UTOPIA Parity Error" Interrupt since the last read of this register.
	produ	les l	The Transmit ATM Cell Processor block will generate this interrupt anytime it has received an ATM cell byte or 16-bit word (from the Transmit UTOPIA Interface block) that contains a parity error.
	Theprod	Mich	0 – Indicates that the Transmit ATM Cell Processor block has NOT declared the "Detection of Transmit UTOPIA Parity Error" Interrupt since the last read of this register.
	***		1 – Indicates that the Transmit ATM Cell Processor block has declared the "Detection of Transmit UTOPIA Parity Error" Interrupt since the last read of this register.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS



Table 215: Transmit ATM Cell Processor Block – Transmit ATM Interrupt Enable Register (Address = 0xNF0F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unu	used	Transmit Cell Extraction Interrupt Enable	Transmit Cell Insertion Interrupt Enable	Transmit Cell Extraction Memory Overflow Interrupt Enable	Transmit Cell Insertion Memory Overflow Interrupt Enable	Detection of HEC Byte Error Interrupt Enable	Detection of Transmit UTOPIA Parity Error Interrupt Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 6	Unused		Att ruite
5	Transmit Cell	R/W	Transmit Cell Extraction Interrupt Enable:
	Extraction Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Transmit Cell Extraction" Interrupt.
			If the user enables this feature, then the Transmit ATM Cell Processor block will generate the "Transmit Cell Extraction" Interrupt anytime it receives an incoming ATM cell (from the TxFIFO) and loads this ATM cell into the "Transmit Extraction Memory" Buffer.
			0 – Disables the Transmit Cell Extraction" Interrupt.
			1 – Enables the "Transmit Cell Extraction" Interrupt
4	Transmit Cell	R/W	Transmit Cell Insertion Interrupt Enable:
	Insertion Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Transmit Cell Insertion" Interrupt.
		,odi	If the user enables this feature, then the Transmit ATM Cell Processor block will generate the "Transmit Cell Insertion" Interrupt anytime a cell (residing in the "Transmit Cell Insertion" Buffer) is read out of the "Transmit Cell Insertion" Buffer and is loaded into the "outbound" ATM cell traffic.
		01 3	0 – Disables the Transmit Cell Insertion Interrupt.
		O NO	1 Enables the Transmit Cell Insertion Interrupt.
3	Transmit Cell	R/W	Transmit Cell Extraction Memory Overflow Interrupt Enable:
	Extraction Memory Overflow	3/1	This READ/WRITE bit-field permits the user to either enable or disable the "Transmit Cell Extraction Memory Overflow" Interrupt.
	Interrupt Enable		If the user enables this interrupt, then the Transmit ATM Cell Processor block will generate an interrupt any time an overflow event has occurred in the "Transmit Cell Extraction Memory" buffer.
			0 – Disables the Transmit Cell Extraction Memory Overflow Interrupt.
			1 – Enables the Transmit Cell Extraction Memory Overflow Interrupt.
2	Transmit Cell	R/W	Transmit Cell Insertion Memory Overflow Interrupt Enable:
	Insertion Memory Overflow		This READ/WRITE bit-field permits the user to either enable or disable the "Transmit Cell Insertion Memory Overflow" Interrupt.
	Interrupt Enable		If the user enables this interrupt, then the Transmit ATM Cell Processor block will generate an interrupt any time an overflow event has occurred in the "Transmit Cell Insertion Memory" buffer.

			0 – Disables the Transmit Cell Insertion Memory Overflow Interrupt.					
			1 – Enables the Transmit Cell Insertion Memory Overflow Interrupt.					
			1 – Enables the Transmit Cell Insertion Memory Overflow Interrupt.					
1	Detection of HEC Byte Error	R/W	Detection of HEC Byte Error Interrupt Enable:					
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of HEC Byte Error Interrupt" within the Transmit ATM Cell Processor Block.					
			If the user enables this interrupt, then the Transmit ATM Cell Processor block will generate an interrupt each time it receives an ATM cell (from the TxFIFO) that contains a HEC Byte error.					
			0 – Disables the "Detection of HEC Byte Error" Interrupt.					
			1 – Enables the "Detection of HEC Byte Error" Interrupt					
0	Detection of		Detection of Transmit UTOPIA Parity Error Interrupt Enable:					
	Transmit UTOPIA Parity Error Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Transmit UTOPIA Parity Error" Interrupt within the Transmit ATM Cell Processor block.					
			If the user enables this interrupt, then the Transmit ATM Cell Processor be will generate an interrupt each time it receives an ATM cell byte or 10 word (from the TxFIFO) that contains a parity error.					
			0 – Disables the "Detection of Transmit UTOPIA Parity Error" Interrupt.					
			1 – Enables the "Detection of Transmit UTOPIA Parity Error" Interrupt.					

Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 216: Transmit ATM Cell Processor Block – Transmit ATM Cell Insertion/Extraction Memory Control Register (0xNF13)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		Transmit Cell Extraction Memory RESET*	Transmit Cell Extraction Memory CLAV	Transmit Cell Insertion Memory RESET*	Transmit Cell Insertion Memory ROOM	Transmit Cell Insertion Memory WSOC
R/O	R/O	R/O	R/W	R/O	R/W	R/O	W/O
0	0	0	1	0	1	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7-5	Unused		
4	Transmit Cell Extraction Memory RESET*	R/W	Transmit Cell Extraction Memory RESET*:
			This READ/WRITE bit-field permits the user to perform a REST operation to the Transmit Cell Extraction Memory.
			If the user writes a "1-to-0 transition" into this bit-field, then the following events will occur.
			All of the contents of the Transmit Cell Extraction Memory will be flushed.
			All READ and WRITE pointers will be reset to their default positions.
			Notes: Following this RESET event, the user must write the value "1" into this bit-field in order to enable normal operation within the Transmit Cell Extraction Memory.
3	Transmit Cell Extraction	R/O	Transmit Cell Extraction Memory – Cell Available Indicator:
	Memory CLAV	TO SO THE STATE OF	This READ-ONLY bit-field indicates whether or not there is at least ATM cell of data (residing within the Transmit Cell Extraction Memory) that needs to be read out via the Microprocessor Interface.
			0 - Indicates that the Transmit Cell Extraction Memory is empty and contains no ATM cell data.
	100 x 80		1 – Indicates that the Transmit Cell Extraction Memory contains at least one ATM cell of data that needs to be read out.
	Thatea		Notes: The user should validate each ATM cell that is being read out from the Transmit Cell Extraction memory by checking the state of this bit-field prior to reading out the contents of ATM cell data residing within the Transmit Cell Extraction Memory
2	Transmit Cell Insertion	R/W	Transmit Cell Insertion Memory RESET*:
Memory RESET*		This READ/WRITE bit-field permits the user to perform a RESET operation to the Transmit Cell Insertion Memory.	
			If the user writes a "1-to-0 transition" into this bit-field, then the following events will occur.
			All of the contents of the Transmit Cell Insertion Memory will be flushed.
			All READ and WRITE pointers will be reset to their default positions.
			Notes: Following this RESET event, the user must write the value "1" into this bit-field in order to enable normal

			operation of the Transmit Cell Insertion Memory.
1	Transmit Cell Insertion Memory ROOM	R/O	Transmit Cell Insertion Memory – ROOM Indicator:
			This READ-ONLY bit-field indicates whether or not there is room (e.g., empty space) available for the contents of another ATM cell to be written into the Transmit Cell Insertion Memory.
			0 - Indicates that the Transmit Cell Insertion Memory does not contain enough empty space to receive another ATM cell via the Microprocessor Interface.
			1 – Indicates that the Transmit Cell Insertion Memory does contain enough empty space to receive another ATM cell via the Microprocessor Interface.
			Notes: The user should verify that the Transmit Cell Insertion Memory has sufficient empty space to accept another ATM cell of data (via the Microprocessor Interface) by polling the state of this bit-field prior to writing each cell into the Transmit Cell Insertion Memory.
0	Transmit Cell Insertion	W/O	Transmit Cell Insertion Memory – Write SOC (Start of Cell):
	Memory WSOC		Whenever the user is writing the contents of an ATM cell into the Transmit Cell Insertion Memory, then he/she is suppose to identify/designate the very first byte of this ATM cell by setting this bit-field to "1". Whenever the user does this, then the Transmit Cell Insertion Memory will "know" that the next octet that is written into the "Transmit ATM Cell Processor Block — Transmit Cell Insertion/Extraction Memory Data Register — Byte 3 (Address = 0xNF14) is designated as the first byte of the ATM cell currently being written into the Transmit Cell Insertion Memory.
		, prod	This bit-field must be set to "0" during all other WRITE operations to the Transmit ATM Cell Processor – Transmit Cell Insertion/Extraction Memory Data Register
	The product of the pr	are the same of th	Se of C



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 217: Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory Data – Byte 3 (Address = 0xNF14)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3 Віт 2		Віт 1	Віт 0
Transmit Cell Insertion/Extraction Memory Data[31:24]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	Transmit Cell	R/W	Transmit Cell Insertion/Extraction Memory Data[31:24]:
Insertion/Extracti Memory Data[31:	Memory Data[31:24]		These READ/WRITE bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory Data – Bytes 2 through 0" support the following functions. • They function as the address location for the user to write the
			contents of an "outbound" ATM cell into the Transmit Cell Insertion Memory, via the Microprocessor Interface.
			They function as the address location, for which the user to read out the contents of an "inbound" ATM cell from the Receive Cell Extraction Memory, via the Microprocessor Interface.
			Notes:
			1. If the user performs a WRITE operation to this (and the other three address locations), then he/she is writing ATM cell data into the Transmit Cell Insertion Memory.
The production of the productio		Jot of	2. If the user performs a READ operation to this (and the other three address locations), then he/she is reading ATM cell data from the Transmit Cell Extraction Memory.
	N		3. READ and WRITE operations must be performed in a "32-bit" (4-byte "word") manner. Hence, whenever the user performs a READ/WRITE operation to these address locations, he/she must start by writing in or reading out the first byte (of this "4-byte" word) of a given ATM cell, into/from this performance.
	way	Next, the user must perform the READ/WRITE operation (with the second of this "4-byte" word) to the "Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory – Byte 2 register. Afterwards, the user must perform a READ/WRITE operation (with the third of this "4-byte" word) to the Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory –	
	· de anc		Byte 1 register. Finally, the user must perform a READ/WRITE operation (with the fourth of this "4-byte" word) to the Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory – Byte 0 register. When reading out (writing in) the next four bytes of a given ATM Cell, the user must repeat this process with a READ or WRITE operation, from/to this register location, and so on.
			4. Whenever the user is writing cell data into the Transmit Cell Insertion Memory, the size of the Cell is always 56 bytes.
			5. Whenever the user is reading cell data from the Transmit Cell Extraction Memory, the size of the Cell is always 56 bytes.

Table 218: Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory Data – Byte 2 (Address = 0xNF15)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit Cell Insertion/Extraction Memory Data[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	Transmit Cell	R/W	Transmit Cell Insertion/Extraction Memory Data[23:16]:
	Insertion/Extraction Memory Data[23:16]		These READ/WRITE bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory Data – Bytes 3, 1 and 6" support the following functions.
			They function as the address location for the user to write the contents of an "outbound" ATM cell into the Transmit Cell Insertion Memory, via the Microprocessor Interface.
			They function as the address location, for which the user to read out the contents of an "inbound" ATM cell from the Receive Cell Extraction Memory, via the Microprocessor Interface.
			Notes:
			If the user performs a WRITE operation to this (and the other three address locations), then he/she is writing ATM cell data into the Transmit Cell Insertion Memory.
		du	2. If the user performs a READ operation to this (and the other three address locations), then he/she is reading ATM cell data from the Transmit Cell Extraction Memory.
The product of the pr	Protection	3. READ and WRITE operations must be performed in a "32-bit" (4-byte "word") manner. Hence, whenever the user performs a READ/WRITE operation to these address locations, he/she must start by writing in or reading out the first byte (of this "4-byte" word) of a given ATM cell, into/from the Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory – Byte 3" register. Next, the user must perform the READ/WRITE operation (with the second of this "4-byte" word) to this particular address location. Afterwards, the user must perform a READ/WRITE operation (with the third of this "4-byte" word) to the Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory – Byte 1 register. Finally, the user must perform a READ/WRITE operation (with the fourth of this	
	'0		"4-byte" word) to the Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory – Byte 0 register. When reading out (writing in) the next four bytes of a given ATM Cell, the user must repeat this process with a READ or WRITE operation, from/to this register location, and so on.
			4. Whenever the user is writing cell data into the Transmit Cell Insertion Memory, the size of the Cell is always 56 bytes.
			5. Whenever the user is reading cell data from the Transmit Cell Extraction Memory, the size of the Cell is always 56 bytes.



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 219: Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory Data – Byte 1 (Address = 0xNF16)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit Cell Insertion/Extraction Memory Data[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	Transmit Cell Insertion/Extraction Memory Data[15:8]	R/W	Transmit Cell Insertion/Extraction Memory Data[15:8]: These READ/WRITE bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory Data – Bytes 3, 2 and 0" support the following functions. They function as the address location for the user to write the contents of an "outbound" ATM cell into the Transmit Cell Insertion Memory, via the Microprocessor Interface. They function as the address location, for which the user to read out the contents of an "inbound" ATM cell from the Receive Cell Extraction Memory, via the Microprocessor Interface. Notes: 1. If the user performs a WRITE operation to this (and the other three address locations), then he/she is writing ATM cell data into the Transmit Cell Insertion Memory. 2. If the user performs a READ operation to this (and the other three address locations), then he/she is reading ATM cell data from the Transmit Cell Extraction Memory.

Table 220: Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory Data – Byte 0 (Address = 0xNF17)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit Cell Insertion/Extraction Memory Data[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	Transmit Cell Insertion/Extraction Memory Data[7:0]	R/W	 Transmit Cell Insertion/Extraction Memory Data[7:0]: These READ/WRITE bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory Data – Bytes 3, through 1" support the following functions. They function as the address location for the user to write the contents of an "outbound" ATM cell into the Transmit Cell Insertion Memory, via the Microprocessor Interface. They function as the address location, for which the user to read out the contents of an "inbound" ATM cell from the Receive Cell Extraction Memory, via the Microprocessor Interface. Notes: 1. If the user performs a WRITE operation to this (and the other three address locations), then he/she is writing ATM cell data into the Transmit Cell Insertion Memory. 2. If the user performs a READ operation to this (and the other three address locations), then he/she is reading ATM cell data from
	The product	or production of the state of t	three address locations), then he'she is writing ATM cell data into the Transmit Cell Insertion Memory. 2. If the user performs a READ operation to this (and the other three address locations), then he'she is reading ATM cell data from the Transmit Cell Extraction Memory. 3. READ and WRITE operations must be performed in a "32-bit" (4-byte "word") manner. Hence, whenever the user performs a READ/WRITE operation to these address locations, he/she must start by writing in or reading out the first byte (of this "4-byte" word) of a given ATM cell, into/from the Transmit ATM Cell Processor Block — Transmit Cell Insertion/Extraction Memory — Byte 3 register. Next, the user must perform the READ/WRITE operation (with the second of this "4-byte" word) to the "Transmit ATM Cell Processor Block — Transmit Cell Insertion/Extraction Memory — Byte 2 register. Afterwards, the user must perform a READ/WRITE operation (with the third of this "4-byte" word) to the "Transmit ATM Cell Processor Block — Transmit Cell Insertion/Extraction Memory — Byte 1" register. Finally, the user must perform a READ/WRITE operation (with the fourth of this "4-byte" word) to this particular register location. When reading out (writing in) the next four bytes of a given ATM Cell, the user must repeat this process with a READ or WRITE operation, from/to this register location, and so on.
			4. Whenever the user is writing cell data into the Transmit Cell Insertion Memory, the size of the Cell is always 56 bytes.
			5. Whenever the user is reading cell data from the Transmit Cell Extraction Memory, the size of the Cell is always 56 bytes.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 221: Transmit ATM Cell Processor Block – Transmit ATM Idle Cell Header Byte 1 (Address = 0xNF18)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit Idle Cell Header Byte 1 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit Idle Cell	R/W	Transmit Idle Cell Header Byte – 1[7:0]:
	Header Byte – 1 [7:0]		These READ/WRITE register bits, along with that in "Transmit ATM Cell Processor Block – Transmit ATM Idle Cell Header Byte 2 through Byte 4" registers permit the user to define the header byte pattern of all Idle Cells that are generated by the Transmit ATM Cell Processor block. This register permits the user to define/specify the value of Header Byte # 1 within each Idle Cell that is generated and transmitted by the Transmit ATM Cell Processor block.

Table 222: Transmit ATM Cell Processor Block – Transmit ATM Idle Cell Header Byte 2 (Address = 0xNF19)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 2	Віт 1	Віт 0	
Transmit Idle Cell Header Byte 2 [7:0]							
R/W	R/W	R/W	R/W R/W	R/W	R/W	R/W	
0	0	0	90	0	0	0	

BIT NUMBER	Name	TYPE	DESCRIPTION
7-0	Transmit Idle Cell Header Byte – 2 [7:0]	RAW	Transmit Idle Cell Header Byte – 2[7:0]: These READ/WRITE register bits, along with that in "Transmit ATM Cell Processor Block – Transmit ATM Idle Cell Header Bytes 1, 3 and 4" registers permit the user to define the header byte pattern of all Idle Cells that are generated by the Transmit ATM Cell Processor block. This register permits the user to define/specify the value of Header Byte # 2 within each Idle Cell that is generated and transmitted by the Transmit ATM Cell Processor block.
	and the second s)	

Table 223: Transmit ATM Cell Processor Block – Transmit ATM Idle Cell Header Byte 3 (Address = 0xNF1A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit Idle Cell Header Byte 3 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit Idle Cell Header Byte – 3 [7:0]	R/W	Transmit Idle Cell Header Byte – 3[7:0]: These READ/WRITE register bits, along with that in "Transmit ATM Cell Processor Block – Transmit ATM Idle Cell Header Bytes 1, 2 and 4" registers permit the user to define the header byte pattern of all Idle Cells that are generated by the Transmit ATM Cell Processor block. This register permits the user to define/specify the value of Header Byte # 3 within each Idle Cell that is generated and transmitted by the
			Transmit ATM Cell Processor block.

Table 224: Transmit ATM Cell Processor Block – Transmit ATM Idle Cell Header Byte 4 (Address = 0xNF1B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit Idle Cell Header Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	79, 0	0	0	0	0

BIT NUMBER	Name	TYPE	DESCRIPTION
7 – 0	Transmit Idle Cell Header Byte – 4 [7:0]	RW	Transmit Idle Cell Header Byte – 4[7:0]: These READ/WRITE register bits, along with that in "Transmit ATM Cell Processor Block – Transmit ATM Idle Cell Header Byte 1 through Byte 3" registers permit the user to define the header byte pattern of all Idle Cells that are generated by the Transmit ATM Cell Processor block. This register permits the user to define/specify the value of Header Byte # 4 within each Idle Cell that is generated and transmitted by the Transmit ATM Cell Processor block.
	%		

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 225: Transmit ATM Cell Processor Block – Transmit ATM Idle Cell Payload Register (Address = 0xNF1F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Transmit Idle Cell Payload Byte[7:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	Transmit Idle Cell Payload Byte[7:0]	R/W	Transmit Idle Cell Payload Byte [7:0]: These READ/WRITE register bits permit the user to define the value of the payload bytes of all Idle Cells that are generated and transmitted by the Transmit ATM Cell Processor block.
			Notes: Each of the 48 payload bytes (within each outbound Idle Cell) will be assigned the value that is written into this register.

Table 226: Transmit ATM Cell Processor Block – Transmit Test Cell Header Byte – Byte 1 (Address = 0xNF20)

Віт 7	Віт 6	Віт 5	Віт 4	Bit 3	Віт 2	Віт 1	Віт 0
Transmit Test Cell Header By					[7:0]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0		0	0	0

BIT NUMBER	Name	TYPE	DESCRIPTION
7 – 0	Transmit Test Cell Header Byte	R/W	Receive Test Cell Header Byte 1:
	1[7:0]	le he	These READ/WRITE register bits along with that in the Transmit ATM Cell Processor Block – Transmit Cell Header Byte – Bytes 2 through 4" permit the user to define the headers of test cells that the Transmit Test Cell Generator will generate.
	opioshe at	0	This particular register byte permits the user to define the contents of Header Byte # 1.
	The data dinic		Notes: These register bits are only active if the Transmit Test Cell Generator has been enabled.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 227: Transmit ATM Cell Processor Block – Transmit Test Cell Header Byte – Byte 2 (Address = 0xNF21)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit Test Cell Header Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit Test Cell Header Byte 2[7:0]	R/W	Receive Test Cell Header Byte 2: These READ/WRITE register bits along with that in the "Transmit ATM Cell Processor Block – Transmit Cell Header Byte – Bytes 1, 3 and 4" permit the user to define the headers of test cells that the Transmit Test Cell Generator will generate. This particular register byte permits the user to define the contents of Header Byte # 2. Notes: These register bits are only active if the Transmit Test Cell Generator has been enabled.

Table 228: Transmit ATM Cell Processor Block – Transmit Test Cell Header Byte – Byte 3 (Address = 0xNF22)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit Test Cell Header Byte 3 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0, 9, %	0	0	0	0	
	101 100 AV							

BIT NUMBER	Name V	Type	DESCRIPTION
7 – 0	Transmit Test Cell Header Byte 3[7:0]	R/W	Receive Test Cell Header Byte 3: These READ/WRITE register bits along with that in the "Transmit ATM Cell Processor Block – Transmit Cell Header Byte – Bytes 1, 2 and 4" permit the user to define the headers of test cells that the Transmit Test Cell Generator will generate. This particular register byte permits the user to define the contents of Header Byte # 3. Notes: These register bits are only active if the Transmit Test Cell Generator has been enabled.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 229: Transmit ATM Cell Processor Block – Transmit Test Cell Header Byte – Byte 4 (Address = 0xNF23)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Transmit Test Cell Header Byte 4 [7:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit Test Cell	R/W	Receive Test Cell Header Byte 4:
	Header Byte 4[7:0]		These READ/WRITE register bits along with that in the "Transmit ATM Cell Processor Block – Transmit Cell Header Byte – Bytes 1 through 3" permit the user to define the headers of test cells that the Transmit Test Cell Generator will generate. This particular register byte permits the user to define the contents of Header Byte # 4. Notes: These register bits are only active if the Transmit Test Cell Generator has been enabled.

Table 230: Transmit ATM Cell Processor Block – Transmit ATM Cell Counter (Address = 0xNF28)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 2	Віт 1	Віт 0		
Transmit ATM Cell Count[31:24]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0,00	0	0	0		
	Vio 101 sie							

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit ATM Cell Count[31:24]	RUR	Transmit ATM Cell Count – Byte 3[31:24]: This RESET-upon-READ register, along with the "Transmit ATM Cell Count – Bytes 2 through 0" registers; contain a 32-bit value for the number of User/Valid cells that have been transmitted by the Transmit ATM Cell Processor block. This particular register contains the MSB (Most Significant Byte) value for this 32-bit expression. Notes: 1. The contents within these registers include all of the following: All ATM cells that have been read out from the TxFIFO, or the Transmit Cell Insertion Buffer. 2. The contents of these registers do not include the number of Idle Cells that have been generated by the Transmit ATM Cell Processor block. 3. If the number of Cells reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x000000000").

Table 231: Transmit ATM Cell Processor Block – Transmit ATM Cell Counter (Address = 0xNF29)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit ATM Cell Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	Transmit ATM Cell	RUR	Transmit ATM Cell Count – Byte 2[23:16]:
	Count[23:16]	This RESET-upon-READ register, along with the "Transmit ATM Cell Count – Bytes 3, 1 and 0" registers; contain a 32-bit value for the number of User/Valid cells that have been transmitted by the Transmit ATM Cell Processor block.	
			Notes:
		The contents within these registers include all of the following: All ATM cells that have been read out from the TxFIFO, or the Transmit Cell Insertion Buffer.	
			2. The contents of these registers do not include the number of Idle Cells that have been generated by the Transmit ATM Cell Processor block.
			3. If the number of Cells reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").

Table 232: Transmit ATM Cell Processor Block – Transmit ATM Cell Counter (Address = 0xNF2A)

			7, 0					
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit ATM Cell Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0 *	.0 8	0	0	0	0	

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit ATM Cell Count[15:8]	RUR	Transmit ATM Cell Count – Byte 1[15:8]: This RESET-upon-READ register, along with the "Transmit ATM Cell Count – Bytes 3, 2 and 0" registers; contain a 32-bit value for the number of User/Valid cells that have been transmitted by the Transmit ATM Cell Processor block. Notes: 1. The contents within these registers include all of the following: All ATM cells that have been read out from the TxFIFO, or the Transmit Cell Insertion Buffer. 2. The contents of these registers do not include the number of Idle Cells that have been generated by the Transmit ATM Cell Processor block.
			3. If the number of Cells reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 233: Transmit ATM Cell Processor Block – Transmit ATM Cell Counter (Address = 0xNF2B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit ATM Cell Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	Transmit ATM	RUR	Transmit ATM Cell Count – Byte 0[7:0]:
	Cell Count[7:0]	 Bytes 3 through 1" register User/Valid cells that have Processor block. This particular register contact this 32-bit expression. Notes: 1. The contents within these in the second process. 	This particular register contains the LSB (Least Significant Byte) value for this 32-bit expression.
			Buffer.
		2. The contents of these registers do not include the number of Idle Cells that have been generated by the Transmit ATM Cell Processor block.	
			3. If the number of Cells reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").
	The	or odu	3. If the number of Cells reaches the value "DXFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 234: Transmit ATM Cell Processor Block – Transmit ATM Cell Discard Cell Count – Byte 3 (Address = 0xNF2C)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit – Discard Cell Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	NAME Transmit – Discard Cell Count[31:24]	TYPE RUR	Transmit – Discard Cell Count – Byte 3[7:0]: This RESET-upon-READ register, along with the "Transmit ATM Cell Processor Block – Transmit ATM Cell Discard Cell Count – Bytes 2 through 0" registers; contain a 32-bit value for the number of ATM cells that have been discarded by the Transmit ATM Cell Processor block. This particular register contains the MSB (Most Significant Byte) value of this 32-bit expression. Notes:
			1. The contents within these register includes all ATM cells that contain either a HEC Byte error or a "Transmit UTOPIA Parity" error. 2. If the number of Cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").

Table 235: Transmit ATM Cell Processor Block — Transmit ATM Cell Discard Cell Count – Byte 2 (Address = 0xNF2D)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit - Discard Cell Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	
	100 00 100 100 100 100 100 100 100 100							

BIT NUMBER	NAME O	Түре	DESCRIPTION
7 - 0	Transmit – Discard	RUR	Transmit – Discard Cell Count – Byte 2[7:0]:
	Cell Count[23:16]		This RESET-upon-READ register, along with the "Transmit ATM Cell Processor Block – Transmit ATM Cell Discard Cell Count – Bytes 3, 1 and 0" registers; contain a 32-bit value for the number of ATM cells that have been discarded by the Transmit ATM Cell Processor block.
			Notes:
			The contents within these register includes all ATM cells that contain either a HEC Byte error or a "Transmit UTOPIA Parity" error.
			2. If the number of Cells reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 236: Transmit ATM Cell Processor Block – Transmit ATM Cell Discard Cell Count – Byte 1 (Address = 0xNF2E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit – Discard Cell Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	Transmit – Discard Cell Count[15:8]	RUR	Transmit – Discard Cell Count – Byte 1[7:0]: This RESET-upon-READ register, along with the "Transmit ATM Cell Processor Block – Transmit ATM Cell Discard Cell Count – Bytes 3, 2 and 0" registers; contain a 32-bit value for the number of ATM cells that have been discarded by the Transmit ATM Cell Processor block. Notes: 1. The contents within these register includes all ATM cells that contain either a HEC Byte error or a "Transmit UTOPIA Parity" error. 2. If the number of Cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x000000000").

Table 237: Transmit ATM Cell Processor Block Transmit ATM Cell Discard Cell Count – Byte 0 (Address = 0xNF2F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit - Discard Cell Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0, 0,	0	0	0	0

BIT NUMBER	Name	TYPE	DESCRIPTION
7 - 0	Transmit – Discard Cell Count[7:0]	RUR	Transmit – Discard Cell Count – Byte 0[7:0]: This RESET-upon-READ register, along with the "Transmit ATM Cell Processor Block – Transmit ATM Cell Discard Cell Count – Bytes 3 through 1" registers; contain a 32-bit value for the number of ATM cells that have been discarded by the Transmit ATM Cell Processor block. This particular register contains the LSB (Least Significant Byte) value of this 32-bit expression. Notes: 1. The contents within these register includes all ATM cells that contain either a HEC Byte error or a "Transmit UTOPIA Parity" error. 2. If the number of Cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 238: Transmit ATM Cell Processor Block – Transmit ATM HEC Byte Error Count Register – Byte 3 (Address = 0xNF30)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit – HEC Byte Error Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit – HEC Byte	RUR	Transmit – HEC Byte Error Count – Byte 3[7:0]:
	Error Count[31:24]		This RESET-upon-READ register, along with the "Transmit ATM Cell Processor Block — Transmit ATM HEC Byte Error Count Register — Bytes 2 through 0" register; contain a 32-bit value for the number of ATM cells that contain HEC byte errors (as detected by the Transmit ATM Cell Processor block). This particular register functions as the MSB (Most Significant Byte) for this 32-bit expression. Notes: 1. This register is valid if the Transmit ATM Cell Processor block has been configured to compute and verify the HEC byte of each ATM cell that it receives from the TxFIFO or the "Transmit Cell Insertion Buffer". 2. If the number of cells reaches the value "0xFFFFFFFF", then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").

Table 239: Transmit ATM Cell Processor Block Transmit ATM HEC Byte Error Count Register – Byte 2 (Address = 0xNF31)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Transmit - HEC Byte Error Count[23:16]						
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME 0	TYPE	DESCRIPTION
BIT NUMBER 7 - 0	NAME Transmit - HEC Byte Error Count[23:16]	RUR	Transmit – HEC Byte Error Count – Byte 2[7:0]: This RESET-upon-READ register, along with the "Transmit ATM Cell Processor Block – Transmit ATM HEC Byte Error Count Register – Bytes 3, 1 and 0" register; contain a 32-bit value for the number of ATM cells that contain HEC byte errors (as detected by the Transmit ATM Cell Processor block). Notes: 1. This register is valid if the Transmit ATM Cell Processor block has been configured to compute and verify the HEC byte of each ATM cell that it receives from the TxFIFO or the "Transmit Cell Insertion Buffer". 2. If the number of cells reaches the value "0xFFFFFFFF", then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 240: Transmit ATM Cell Processor Block – Transmit ATM HEC Byte Error Count Register – Byte 1 (Address = 0xNF32)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit – HEC Byte Error Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit – HEC Byte	RUR	Transmit – HEC Byte Error Count – Byte 1[7:0]:
	Error Count[15:8]		This RESET-upon-READ register, along with the "Transmit ATM Cell Processor Block – Transmit ATM HEC Byte Error Count Register – Bytes 3, 2 and 0" register; contain a 32-bit value for the number of ATM cells that contain HEC byte errors (as detected by the Transmit ATM Cell Processor block). **Notes:** 1. This register is valid if the Transmit ATM Cell Processor block has been configured to compute and verify the HEC byte of each ATM cell that it receives from the TxFIFO or the "Transmit Cell Insertion Buffer". 2. If the number of cells reaches the value "0xFFFFFFFF", then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x000000000").

Table 241: Transmit ATM Cell Processor Block — Transmit ATM HEC Byte Error Count Register – Byte 0 (Address = 0xNF33)

0 () (- J			10 (
Віт 7	Віт 6	Віт 5	Віт 4	BIT 3	Віт 2	Віт 1	Віт 0
	Transmit HEC Byte Error Count[7:0]						
RUR	RUR	RUR	RURO	RUR	RUR	RUR	RUR
0	0	0		0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit – HEC Byte Error Count[7:0]	RUR	Transmit – HEC Byte Error Count – Byte 0[7:0]: This RESET-upon-READ register, along with the "Transmit ATM Cell Processor Block – Transmit ATM HEC Byte Error Count Register – Bytes 3 through 1" register; contain a 32-bit value for the number of ATM cells that contain HEC byte errors (as detected by the Transmit ATM Cell Processor block). This particular register functions as the LSB (Least Significant Byte) for this 32-bit expression. Notes: 1. This register is valid if the Transmit ATM Cell Processor block has been configured to compute and verify the HEC byte of each ATM cell that it receives from the TxFIFO or the "Transmit Cell Insertion Buffer". 2. If the number of cells reaches the value "0xFFFFFFF", then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x000000000").

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 242: Transmit ATM Cell Processor Block – Transmit UTOPIA Parity Error Count Register – Byte 3 (Address = 0xNF34)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Transm	nit UTOPIA – Pa	arity Error Coun	t[31:24]		
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	Transmit UTOPIA – Parity Error Count[31:24]	RUR	Transmit UTOPIA Parity Error Count – Byte 3[7:0]: This RESET-upon-READ register, along with the "Transmit ATM Cell Processor Block – Transmit UTOPIA Parity Error Count Register – Bytes 2 through 0" registers; contains a 32-bit value for the number of ATM cells that contain "Transmit UTOPIA" Parity (byte or word) errors (as detected by the Transmit ATM Cell Processor block). This particular register functions as the MSB (Most Significant Byte) for this 32-bit expression. Notes: if the number of cells reaches the value "0xFFFFFFFF", then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x000000000").

Table 243: Transmit ATM Cell Processor Block - Transmit UTOPIA Parity Error Count Register – Byte 2 (Address = 0xNF35)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0			
		Transm	nit UTOPIA - Par	ty Error Coun	t[23:16]					
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR			
0	0	0	,00,0	0	0	0	0			

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit UTOPIA Parity Error Count[23:16]	BUR O Inay	Transmit UTOPIA Parity Error Count – Byte 2[7:0]: This RESET-upon-READ register, along with the "Transmit ATM Cell Processor Block – Transmit UTOPIA Parity Error Count Register – Bytes 3, 1 and 0" registers; contains a 32-bit value for the number of ATM cells that contain "Transmit UTOPIA" Parity (byte or word) errors (as detected by the Transmit ATM Cell Processor block). Notes: if the number of cells reaches the value "0xFFFFFFFF", then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x000000000").

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 244: Transmit ATM Cell Processor Block – Transmit UTOPIA Parity Error Count Register – Byte 1 (Address = 0xNF36)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Transr	nit UTOPIA – P	arity Error Cour	nt[15:8]		
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	Transmit UTOPIA – Parity Error Count[15:8]	RUR	Transmit UTOPIA Parity Error Count – Byte 1[7:0]: This RESET-upon-READ register, along with the "Transmit ATM Cell Processor Block – Transmit UTOPIA Parity Error Count Register – Bytes 3, 2 and 0" registers; contains a 32-bit value for the number of ATM cells that contain "Transmit UTOPIA Parity (byte or word) errors (as detected by the Transmit ATM Cell Processor block). Notes: if the number of cells reaches the value "0xFFFFFFFF", then these registers will saturate to and remain at this value (e.g.,
			it will NOT overflow to "0x0000000").

Table 245: Transmit ATM Cell Processor Block – Transmit UTOPIA Parity Error Count Register – Byte 0 (Address = 0xNF37)

Віт 7	Віт 6	Віт 5	Віт 4	ВітЗ	🔰 Віт 2	Віт 1	Віт 0
		Trans	mit UTOPIA – P	arity Error Cou	nt[7:0]		
RUR	RUR	RUR	RUR	V RUR	RUR	RUR	RUR
0	0	0	90	100	0	0	0

BIT NUMBER	N AME	TYPE	1,70	DESCRIPTION
7 - 0	Transmit UTOPIA – Parity Error Count[7:0]	Sylve !	This RESE Processor Bytes 3 thr ATM cells (as detecte This particulation of the cells) this 32-bit of the cells	TOPIA Parity Error Count – Byte 0[7:0]: ET-upon-READ register, along with the "Transmit ATM Cell Block – Transmit UTOPIA Parity Error Count Register – rough 1" registers; contains a 32-bit value for the number of that contain "Transmit UTOPIA" Parity (byte or word) errors d by the Transmit ATM Cell Processor block). Callar register functions as the LSB (Least Significant Byte) for expression. Et the number of cells reaches the value "0xFFFFFFFF", then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x000000000").

Table 246: Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Filter 0 (Address = 0xNF43)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused			Transmit User Cell Filter # 0 Enable	Copy Cell Enable	Discard Cell Enable	Filter if Pattern Match
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3	Transmit User Cell Filter # 0	R/W	Transmit User Cell Filter #0 – Enable:
	Enable		This READ/WRITE bit-field permits the user to either enable or disable Transmit User Cell Filter # 0.
			If the user enables Transmit User Cell Filter # 0, then Transmit User Cell Filter # 0 will function per the configuration settings in Bits 2 through 0, within this register.
			If the user disables Transmit User Cell Filter # 0, then Transmit User Cell Filter # 0 then all cells that are applied to the input of Transmit User Cell Filter # 0 will pass through to the output of Transmit User Cell Filter # 0.
			0 - Disables Transmit User Cell Filter # 0. 1- Enables Transmit User Cell Filter # 0.
2	Copy Cell Enable	R/W	Copy Cell Enable – Transmit User Cell Filter # 0:
	Copy Cell Enable The Product are and the standard the st	the of	This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 0 (within the Transmit ATM Cell Processor Block) to copy all cells that have header byte patterns that comply with the "user-defined" criteria, per Transmit User Cell Filter # 0, or to NOT copy any of these cells. If the user configures Transmit User Cell Filter # 0 to copy all
	the presheat		cells complying with a certain "header-byte" pattern, then a copy (or replicate) of this "compliant" ATM cell will be routed to the Transmit Cell Extraction Buffer.
	1. dand		If the user configures Transmit User Cell Filter # 0 to NOT copy all cells complying with a certain "header-byte" pattern, then NO copies (or replicates) of these "compliant" ATM cells will be made nor will any be routed to the Transmit Cell Extraction Buffer.
			0 – Configures Transmit User Cell Filter # 0 to NOT copy any cells that have header byte patterns which are compliant with the "user-defined" filtering criteria.
			1 – Configures Transmit User Cell Filter # 0 to copy any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria, and to route these copies (of cells) to the Transmit Cell Extraction Buffer.
			Notes: This bit-field is only active if "Transmit User Cell Filter # 0" has been enabled.
1	Discard Cell Enable	R/W	Discard Cell Enable – Transmit User Cell Filter # 0:
			This READ/WRITE bit-field permits the user to either

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			configure Transmit User Cell Filter # 0 (within the Transmit ATM Cell Processor Block) to discard all cells that have header byte patterns that comply with the "user-defined" criteria, per Transmit User Cell Filter # 0, or NOT discard any of these cells.
			If the user configures Transmit User Cell Filter # 0 to NOT discarded any cells that is compliant with a certain "header-byte" pattern, then the cell will be retained for further processing.
			0 - Configures Transmit User Cell Filter # 0 to NOT discard any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria.
			1 – Configures Transmit User Cell Filter # 0 to discard any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria.
			Notes: This bit-field is only active if "Transmit User Cell Filter # 0" has been enabled.
0	Filter if Pattern Match	R/W	Filter if Pattern Match Transmit User Cell Filter # 0:
			This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 0 to filter (based upon the configuration settings for Bits 1 and 2, in this register) ATM cells with header bytes that match the "user-defined" header byte patterns, or to filter ATM cells with header bytes that do NOT match the "user-defined" header byte patterns. 0 Configures Transmit User Cell Filter # 0 to filter user cells that do NOT match the header byte patterns (as defined in
		Prodi	the ""registers). 1 Configures Transmit User Cell Filter # 0 to filter user cells that do match the header byte patterns (as defined in the " " registers).
			Notes: This bit-field is only active if "Transmit User Cell Filter # 0" has been enabled.
	The product of and ma	y not	

Table 247: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 1 (Address = 0xNF44)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	Transmit User Cell Filter # 0 – Pattern Register – Byte 1 [7:0]									
							R/W			
0	0	0	0	0	0	0	0			

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 0 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 0 – Pattern Register – Header Byte 1:
	'		The User Cell filtering criteria (for Transmit User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 Control Register.
		oducte	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Register – Header Byte 1" permits the user to define the User Cell Filtering criteria for "Octet # 1" of the incoming User Cell. The user will write the header byte pattern (for Octet 1) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Register – Header Byte 1" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of product are	in of	

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 248: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 2 (Address = 0xNF45)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 0 – Pattern Register – Byte 2 [7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 0 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 0 – Pattern Register – Header Byte 2:
	2		The User Cell filtering criteria (for Transmit User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 Control Register.
		prodi	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Register – Header Byte 2" permits the user to define the User Cell Filtering criteria for "Octet # 2" of the incoming User Cell. The user will write the header byte pattern (for Octet 2) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Register – Header Byte 2" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of the data and man	are to	2010

Table 249: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 3 (Address = 0xNF46)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 0 – Pattern Register – Byte 3 [7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 0 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 0 – Pattern Register – Header Byte 3:
	3		The User Cell filtering criteria (for Transmit User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 Control Register.
		oducte	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Register – Header Byte 3" permits the user to define the User Cell Filtering criteria for "Octet # 3" of the incoming User Cell. The user will write the header byte pattern (for Octet 3) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Register – Header Byte 3" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of product are	the of	

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 250: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 4 (Address = 0xNF47)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 0 – Pattern Register – Byte 4 [7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 0 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 0 – Pattern Register – Header Byte 4:
	4		The User Cell filtering criteria (for Transmit User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 Control Register.
		prodi	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Register – Header Byte 4" permits the user to define the User Cell Filtering criteria for "Octet # 4" of the incoming User Cell. The user will write the header byte pattern (for Octet 4) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Register – Header Byte 4" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of and man	are to	

Table 251: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Register – Byte 1 (Address = 0xNF48)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 0 – Check Register – Byte 1 [7:0]									
							R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 0 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 0 – Check Register – Header Byte 1:
	1		The User Cell filtering criteria (for Transmit User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 Control Register.
		odució	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 1" permits the user to define the User Cell Filtering criteria for "Octet # 1" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 1" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 1" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	roduct or k	to of	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 1" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 1".
	The product or product are		Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 1" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 1" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 1").

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 252: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Register – Byte 2 (Address = 0xNF49)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 0 – Check Register – Byte 2 [7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 0 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 0 – Check Register – Header Byte 2:
	2		The User Cell filtering criteria (for Transmit User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 Control Register.
		prodi	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 2" permits the user to define the User Cell Filtering criteria for "Octet # 2" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 2" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 2" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	roduct	ale to	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 2" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 2".
	The product of and man		Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 2" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 2" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 2").

Table 253: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Register – Byte 3 (Address = 0xNF4A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Transmit User Cell Filter # 0 - Check Register - Byte 3 [7:0]								
							R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 0 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 0 - Check Register - Header Byte 3:
	3		The User Cell filtering criteria (for Transmit User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 Control Register.
		odució	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 3" permits the user to define the User Cell Filtering criteria for "Octet # 3" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 3" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 3" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	roduct or k	the of	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 3" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 3".
	The product or product are		Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 3" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 3" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 3").

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 254: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Register – Byte 4 (Address = 0xNF4B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 0 – Check Register – Byte 4 [7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 0 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 0 - Check Register - Header Byte 4:
	4		The User Cell filtering criteria (for Transmit User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 Control Register.
		orodi	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 4" permits the user to define the User Cell Filtering criteria for "Octet # 4" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 4" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 4" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	roduct	sie to	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 4" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 4".
	The product of and man	3	Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 4" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 4" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 4").

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 255: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Filtered Cell Count – Byte 3 (Address = 0xNF4C)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 0 – Filtered Cell Count[31:24]									
RUR	RUR RUR RUR RUR RUR RUR R						RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION							
7 – 0	Transmit User Cell	RUR	Transmit User Cell Filter # 0 – Filtered Cell Count[31:24]:							
	Filter # 0 – Filtered Cell Count[31:24]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Filtered Cell Count – Bytes 2" through "0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 0 since the last read of this register.							
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – User Cell Filter # 0" Register (Address = 0xNF43), these register bits will be incremented anytime User Cell Filter # 0 performs any of the following functions.							
			Discards an incoming "User Cell".							
			 Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer. 							
			Both the above actions.							
			This particular register contains the MSB (Most Significant Byte) value for this 32-bit expression.							
		, of	Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").							

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 256: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Filtered Cell Count – Byte 2 (Address = 0xNF4D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 0 – Filtered Cell Count[23:16]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

NAME	Түре	DESCRIPTION						
Transmit User Cell	RUR	Transmit User Cell Filter # 0 - Filtered Cell Count[23:16]:						
Cell Count[23:16]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Filtered Cell Count – Bytes 3, 1 and 0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 0 since the last read of this register.						
		Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Transmit User Cell Filter # 0" Register (Address = 0xNF43), these register bits will be incremented anytime User Cell Filter # 0 performs any of the following functions. • Discards an incoming "User Cell".						
		Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer.						
		Both the above actions.						
		Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").						
"0xFFFFFFF" then these registers will saturate to and remain								
	Transmit User Cell Filter # 0 – Filtered Cell Count[23:16]	Transmit User Cell Filter # 0 – Filtered Cell Count[23:16]						

Table 257: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Filtered Cell Count – Byte 1 (Address = 0xNF4E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 0 - Filtered Cell Count[15:8]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION						
7 – 0	Transmit User Cell	RUR	Transmit User Cell Filter # 0 - Filtered Cell Count[15:8]:						
	Filter # 0 – Filtered Cell Count[15:8]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Filtered Cell Count – Bytes 3, 2 and 0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 0 since the last read of this register.						
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Transmit User Cell Filter # 0" Register (Address = 0xNF43), these register bits will be incremented anytime Transmit User Cell Filter # 0 performs any of the following functions.						
			Discards an incoming "User Cell".						
			Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer.						
			Both the above actions.						
			Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x000000000").						
	0xFFFFFFF" then these registers will saturate to and rema								



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 258: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Filtered Cell Count – Byte 0 (Address = 0xNF4F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 0 – Filtered Cell Count[7:0]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION							
7 – 0	Transmit User Cell	RUR	Transmit User Cell Filter # 0 - Filtered Cell Count[7:0]:							
	Filter # 0 – Filtered Cell Count[7:0]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Filtered Cell Count – Bytes 3" through "1" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 0 since the last read of this register.							
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Transmit User Cell Filter # 0" Register (Address = 0xNF43), these register bits will be incremented anytime Transmit User Cell Filter # 0 performs any of the following functions.							
			Discards an incoming "User Cell".							
			 Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer. Both the above actions. 							
			This particular register contains the LSB (Least Significant Byte) value for this 32-bit expression.							
			Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x000000000").							

Table 259: Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Filter 1 (Address = 0xNF53)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused				Copy Cell Enable	Discard Cell Enable	Filter if Pattern Match
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3	Transmit User Cell Filter # 1	R/W	Transmit User Cell Filter #1 - Enable:
	Enable		This READ/WRITE bit-field permits the user to either enable or disable Transmit User Cell Filter # 1.
			If the user enables Transmit User Cell Filter # 1, then Transmit User Cell Filter # 1 will function per the configuration settings in Bits 2 through 0, within this register.
			If the user disables Transmit User Cell Filter # 1, then Transmit User Cell Filter # 1 then all cells that are applied to the input of Transmit User Cell Filter # 1 will pass through to the output of Transmit User Cell Filter # 1.
		N.C	0 - Disables Transmit User Cell Filter # 1.
		11100	Enables Transmit User Cell Filter # 1.
2	Copy Cell Enable	R/W	Copy Cell Enable – Transmit User Cell Filter # 1:
	Copy Cell Enable	rpe do	This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 1 (within the Transmit ATM Cell Processor Block) to copy all cells that have header byte patterns that comply with the "user-defined" criteria, per Transmit User Cell Filter # 1, or to NOT copy any of these cells.
	the proshee in		If the user configures Transmit User Cell Filter # 1 to copy all cells complying with a certain "header-byte" pattern, then a copy (or replicate) of this "compliant" ATM cell will be routed to the Transmit Cell Extraction Buffer.
	A dand		If the user configures Transmit User Cell Filter # 1 to NOT copy all cells complying with a certain "header-byte" pattern, then NO copies (or replicates) of these "compliant" ATM cells will be made nor will any be routed to the Transmit Cell Extraction Buffer.
			0 – Configures Transmit User Cell Filter # 1 to NOT copy any cells that have header byte patterns which are compliant with the "user-defined" filtering criteria.
			1 – Configures Transmit User Cell Filter # 1 to copy any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria, and to route these copies (of cells) to the Transmit Cell Extraction Buffer.
			Notes: This bit-field is only active if "Transmit User Cell Filter # 1" has been enabled.
1	Discard Cell Enable	R/W	Discard Cell Enable – Transmit User Cell Filter # 1:
			This READ/WRITE bit-field permits the user to either

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			configure Transmit User Cell Filter # 1 (within the Transmit ATM Cell Processor Block) to discard all cells that have header byte patterns that comply with the "user-defined" criteria, per Transmit User Cell Filter # 1, or NOT discard any of these cells.
			If the user configures Transmit User Cell Filter # 1 to NOT discarded any cells that is compliant with a certain "header-byte" pattern, then the cell will be retained for further processing.
			0 – Configures Transmit User Cell Filter # 1 to NOT discard any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria.
			1 – Configures Transmit User Cell Filter # 1 to discard any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria.
			Notes: This bit-field is only active if "Transmit User Cell Filter # 1" has been enabled.
0	Filter if Pattern Match	R/W	Filter if Pattern Match Transmit User Cell Filter # 1:
			This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 1 to filter (based upon the configuration settings for Bits 1 and 2, in this register) ATM cells with header bytes that match the "user-defined" header byte patterns, or to filter ATM cells with header bytes that do NOT match the "user-defined" header byte patterns.
			0 Configures Transmit User Cell Filter # 1 to filter user cells that do NOT match the header byte patterns (as defined in the ""registers).
		Pio	1 Configures Transmit User Cell Filter # 1 to filter user cells that do match the header byte patterns (as defined in the " " registers).
	25		Notes: This bit-field is only active if "Transmit User Cell Filter # 1" has been enabled.
	The product of and man	not	

Table 260: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 1 (Address = 0xNF54)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Transmit User Cell Filter # 1 – Pattern Register – Byte 1 [7:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 1 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 1 – Pattern Register – Header Byte 1:
		oducie	The User Cell filtering criteria (for Transmit User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block — Transmit User Cell Filter # 1 — Pattern Registers", the four "Transmit ATM Cell Processor Block — Transmit User Cell Filter # 1 — Check Registers" and the "Transmit ATM Cell Processor Block — Transmit User Cell Filter # 1 Control Register. This READ/WRITE register, along with the "Transmit ATM Cell Processor Block — Transmit User Cell Filter # 1 — Check Register — Header Byte 1" permits the user to define the User Cell Filtering criteria for "Octet # 1" of the incoming User Cell. The user will write the header byte pattern (for Octet 1) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block — Transmit User Cell Filter # 1 — Check Register — Header Byte 1" that indicates which bits within the first octet of the incoming cells
		40	to be compared with the contents of this register.
	The product of and may no	or of	

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 261: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 2 (Address = 0xNF55)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit User Cell Filter # 1 – Pattern Register – Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 1 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 1 – Pattern Register – Header Byte 2:
	2		The User Cell filtering criteria (for Transmit User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 Control Register.
		orodi	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Register – Header Byte 2" permits the user to define the User Cell Filtering criteria for "Octet # 2" of the incoming User Cell. The user will write the header byte pattern (for Octet 2) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Register – Header Byte 2" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of and ma	are to	2010

Table 262: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 3 (Address = 0xNF56)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Transmit User Cell Filter # 1 – Pattern Register – Byte 3 [7:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 1 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 1 – Pattern Register – Header Byte 3:
	3	oducto	The User Cell filtering criteria (for Transmit User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 Control Register. This READ/WRITE register, along with the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Register - Header Byte 3" permits the user to define the User Cell Filtering criteria for "Octet # 3" of the incoming User Cell. The user will write the header byte pattern (for Octet 3) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Register - Header Byte 3" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of a real may not a real and may not a	the of	

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 263: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 4 (Address = 0xNF57)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit User Cell Filter # 1 – Pattern Register – Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 1 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 1 – Pattern Register – Header Byte 4:
	4		The User Cell filtering criteria (for Transmit User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 Control Register.
		orodi	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Register – Header Byte 4" permits the user to define the User Cell Filtering criteria for "Octet # 4" of the incoming User Cell. The user will write the header byte pattern (for Octet 4) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Register – Header Byte 4" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of and man	are to	

Table 264: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Register – Byte 1 (Address = 0xNF58)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit User Cell Filter # 1 – Check Register – Byte 1 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 1 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 1 – Check Register – Header Byte 1:
	1		The User Cell filtering criteria (for Transmit User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 Control Register.
		odució	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 1" permits the user to define the User Cell Filtering criteria for "Octet # 1" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 1" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 1" by the User Cell
	The product or product are	no or	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 1" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 1".
	The Pisheay,		Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 1" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 1" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 1").



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 265: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Register – Byte 2 (Address = 0xNF59)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit User Cell Filter # 1 – Check Register – Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 1 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 1 – Check Register – Header Byte 2:
	2		The User Cell filtering criteria (for Transmit User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 Control Register.
		prodi	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 2" permits the user to define the User Cell Filtering criteria for "Octet # 2" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 2" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 2" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	roduct co	sie to	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 2" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 2".
	The product of and man	•	Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 2" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 2" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 2").

Table 266: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Register – Byte 3 (Address = 0xNF5A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit User Cell Filter # 1 – Check Register – Byte 3 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 1 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 1 – Check Register – Header Byte 3:
	3		The User Cell filtering criteria (for Transmit User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 Control Register.
		odució	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 3" permits the user to define the User Cell Filtering criteria for "Octet # 3" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 3" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 3" by the User Cell
	The product or product are	toe of	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 3" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 3".
	The Pisheay,		Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 3" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 3" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 3").

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 267: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Register – Byte 4 (Address = 0xNF5B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit User Cell Filter # 1 – Check Register – Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 1 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 1 – Check Register – Header Byte 4:
	4		The User Cell filtering criteria (for Transmit User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 Control Register.
		Prod	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 4" permits the user to define the User Cell Filtering criteria for "Octet # 4" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 4" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 4" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	roduct C	are to	Witing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 4" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 4".
	The product of the data and ma	S	Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 4" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 4" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 4").

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 268: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Filtered Cell Count – Byte 3 (Address = 0xNF5C)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit User Cell Filter # 1 – Filtered Cell Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell	RUR	Transmit User Cell Filter # 1 - Filtered Cell Count[31:24]:
	Filter # 1 – Filtered Cell Count[31:24]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Filtered Cell Count – Bytes 2" through "0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 1 since the last read of this register.
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – User Cell Filter # 1" Register (Address = 0xNF53), these register bits will be incremented anytime User Cell Filter # 1 performs any of the following functions.
			Discards an incoming "User Cell".
			Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer.
			Both the above actions.
			This particular register contains the MSB (Most Significant Byte) value for this 32-bit expression.
		, d	Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x000000000").
	The production of the producti	neet at	e toe



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 269: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Filtered Cell Count – Byte 2 (Address = 0xNF5D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit User Cell Filter # 1 – Filtered Cell Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Transmit User Cell	RUR	Transmit User Cell Filter # 1 – Filtered Cell Count[23:16]:
	Filter # 1 – Filtered Cell Count[23:16]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Filtered Cell Count – Bytes 3, 1 and 0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 1 since the last read of this register.
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Transmit User Cell Filter # 1" Register (Address = 0xNF53), these register bits will be incremented anytime User Cell Filter # 1 performs any of the following functions. • Discards an incoming "User Cell".
			Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer.
			Both the above actions.
			Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x000000000").
	Thepr	andin	Notes: If the number of "filtered cells" reaches the value "0xFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 270: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Filtered Cell Count – Byte 1 (Address = 0xNF5E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	Transmit User Cell Filter # 1 – Filtered Cell Count[15:8]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR			
0	0	0	0	0	0	0	0			

Transmit User Cell	RUR	Transmit User Cell Filter # 1 – Filtered Cell Count[15:8]:						
Cell Count[15:8]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Filtered Cell Count – Bytes 3, 2 and 0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 1 since the last read of this register.						
		Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Transmit User Cell Filter # 1" Register (Address = 0xNF53), these register bits will be incremented anytime Transmit User Cell Filter # 1 performs any of the following functions.						
		Discards an incoming "User Cell".						
		 Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer. 						
		Both the above actions.						
		Notes: If the number of "filtered cells" reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x000000000").						
Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and rem								
	Filter # 1 — Filtered Cell Count[15:8]	Filter # 1 – Filtered Cell Count[15:8]						

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 271: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Filtered Cell Count – Byte 0 (Address = 0xNF5F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 1 – Filtered Cell Count[7:0]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION						
7 – 0	Transmit User Cell	RUR	Transmit User Cell Filter # 1 – Filtered Cell Count[7:0]:						
	Filter # 1 - Filtered Cell Count[7:0]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Filtered Cell Count – Bytes 3" through "1" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 1 since the last read of this register.						
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Transmit User Cell Filter # 1" Register (Address = 0xNF53), these register bits will be incremented anytime Transmit User Cell Filter # 1 performs any of the following functions.						
			Discards an incoming "User Cell".						
			 Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer. Both the above actions. 						
			This particular register contains the LSB (Least Significant Byte) value for this 32-bit expression.						
			Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x000000000").						
	"0xFFFFFFF" then these registers will saturate to and rema								

Table 272: Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Filter 2 (Address = 0xNF63)

Віт 7	Віт 6	Віт 5 Віт 4		Віт 3	Віт 2	Віт 1	Віт 0
	Unused				Copy Cell Enable	Discard Cell Enable	Filter if Pattern Match
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3	Transmit User Cell Filter # 2	R/W	Transmit User Cell Filter #2 – Enable:
	Enable		This READ/WRITE bit-field permits the user to either enable or disable Transmit User Cell Filter # 2.
		If the user enables Transmit User Cell Filter # 2, then Transmit User Cell Filter # 2 will function per the configuration settings in Bits 2 through 0, within this register.	
			If the user disables Transmit User Cell Filter # 2, then Transmit User Cell Filter # 2 then all cells that are applied to the input of Transmit User Cell Filter # 2 will pass through to the output of Transmit User Cell Filter # 2.
		340	0 - Disables Transmit User Cell Filter # 2.
		1110	Enables Transmit User Cell Filter # 2.
2	Copy Cell Enable	R/W	Copy Cell Enable – Transmit User Cell Filter # 2:
	Copy Cell Enable	rpe of	This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 2 (within the Transmit ATM Cell Processor Block) to copy all cells that have header byte patterns that comply with the "user-defined" criteria, per Transmit User Cell Filter # 2, or to NOT copy any of these cells.
	the proshee in		If the user configures Transmit User Cell Filter # 2 to copy all cells complying with a certain "header-byte" pattern, then a copy (or replicate) of this "compliant" ATM cell will be routed to the Transmit Cell Extraction Buffer.
	da and		If the user configures Transmit User Cell Filter # 2 to NOT copy all cells complying with a certain "header-byte" pattern, then NO copies (or replicates) of these "compliant" ATM cells will be made nor will any be routed to the Transmit Cell Extraction Buffer.
			0 – Configures Transmit User Cell Filter # 2 to NOT copy any cells that have header byte patterns which are compliant with the "user-defined" filtering criteria.
			1 – Configures Transmit User Cell Filter # 2 to copy any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria, and to route these copies (of cells) to the Transmit Cell Extraction Buffer.
			Notes: This bit-field is only active if "Transmit User Cell Filter # 2" has been enabled.
1	Discard Cell Enable	R/W	Discard Cell Enable – Transmit User Cell Filter # 2:
			This READ/WRITE bit-field permits the user to either

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			configure Transmit User Cell Filter # 2 (within the Transmit ATM Cell Processor Block) to discard all cells that have header byte patterns that comply with the "user-defined" criteria, per Transmit User Cell Filter # 2, or NOT discard any of these cells.
			If the user configures Transmit User Cell Filter # 2 to NOT discarded any cells that is compliant with a certain "header-byte" pattern, then the cell will be retained for further processing.
			0 – Configures Transmit User Cell Filter # 2 to NOT discard any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria.
			Configures Transmit User Cell Filter # 2 to discard any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria.
			Notes: This bit-field is only active if "Transmit User Cell Filter # 2" has been enabled.
0	Filter if Pattern Match	R/W	Filter if Pattern Match Transmit User Cell Filter # 2:
			This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 2 to filter (based upon the configuration settings for Bits 1 and 2, in this register) ATM cells with header bytes that match the "user-defined" header byte patterns, or to filter ATM cells with header bytes that do NOT match the "user-defined" header byte patterns. 0 Configures Transmit User Cell Filter # 2 to filter user cells that do NOT match the header byte patterns (as defined in
		Prodi	the ""registers). 1 Configures Transmit User Cell Filter # 2 to filter user cells that do match the header byte patterns (as defined in the " " registers).
			Notes: This bit-field is only active if "Transmit User Cell Filter # 2" has been enabled.
	The product of and ma	A not	

Table 273: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 1 (Address = 0xNF64)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 2 – Pattern Register – Byte 1 [7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 2 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 2 – Pattern Register – Header Byte 1:
		oducte	The User Cell filtering criteria (for Transmit User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 Control Register. This READ/WRITE register, along with the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Register - Header Byte 1" permits the user to define the User Cell Filtering criteria for "Octet # 1" of the incoming User Cell. The user will write the header byte pattern (for Octet 1) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Register - Header Byte 1" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of and may not a sent a sent and may not a sent and may not a sent and may not a sent a se	the of	

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 274: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 2 (Address = 0XNF65)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 2 – Pattern Register – Byte 2 [7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 2 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 2 – Pattern Register – Header Byte 2:
	2		The User Cell filtering criteria (for Transmit User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 Control Register.
		orodi	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Check Register – Header Byte 2" permits the user to define the User Cell Filtering criteria for "Octet # 2" of the incoming User Cell. The user will write the header byte pattern (for Octet 2) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Check Register – Header Byte 2" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of and ma	are to	2010

Table 275: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 3 (Address = 0xNF66)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 2 – Pattern Register – Byte 3 [7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 2 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 2 – Pattern Register – Header Byte 3:
	3	oducte	The User Cell filtering criteria (for Transmit User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 Control Register. This READ/WRITE register, along with the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Register - Header Byte 3" permits the user to define the User Cell Filtering criteria for "Octet # 3" of the incoming User Cell. The user will write the header byte pattern (for Octet 3) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Register - Header Byte 3" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of product of product are	the of	

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 276: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 4 (Address = 0xNF67)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Transmit User Cell Filter # 2 – Pattern Register – Byte 4 [7:0]								
							R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 2 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 2 – Pattern Register – Header Byte 4:
	4		The User Cell filtering criteria (for Transmit User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 Control Register.
		prodi	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Check Register – Header Byte 4" permits the user to define the User Cell Filtering criteria for "Octet # 4" of the incoming User Cell. The user will write the header byte pattern (for Octet 4) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Check Register – Header Byte 4" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of the data and man	are to	

Table 277: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Check Register – Byte 1 (Address = 0xNF68)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Transmit User Cell Filter # 2 – Check Register – Byte 1 [7:0]								
							R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 2 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 2 – Check Register – Header Byte 1:
	1		The User Cell filtering criteria (for Transmit User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 Control Register.
		oducto	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 1" permits the user to define the User Cell Filtering criteria for "Octet # 1" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 1" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 1" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	roduct or s	no of	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 1" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 1".
	The product or product are		Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 1" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 1" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 1").

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 278: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Check Register – Byte 2 (Address = 0xNF69)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Transmit User Cell Filter # 2 - Check Register - Byte 2 [7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 2 – Check Register – Header Byte 2	R/W	Transmit User Cell Filter # 2 – Check Register – Header Byte 2:
			The User Cell filtering criteria (for Transmit User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 Control Register.
		production of the second	This READWRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 2" permits the user to define the User Cell Filtering criteria for "Octet # 2" within the incoming User Cell. More specifically, these READWRITE register bits permit the user to specify which bit(s) in "Octet 2" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 2" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	The product of	othe	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 2" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 2".
	The data dinas		Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 2" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 2" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 2").

Table 279: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Check Register – Byte 3 (Address = 0xNF6A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Transmit User Cell Filter # 2 – Check Register – Byte 3 [7:0]								
							R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 2 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 2 – Check Register – Header Byte 3:
	3		The User Cell filtering criteria (for Transmit User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 Control Register.
	70	odució	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 3" permits the user to define the User Cell Filtering criteria for "Octet # 3" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 3" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 3" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	roduct or s	the of	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 3" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 3".
	The product or product are		Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 3" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 3" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 3").



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 280: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Check Register – Byte 4 (Address = 0xNF6B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Transmit User Cell Filter # 2 - Check Register - Byte 4 [7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 2 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 2 - Check Register - Header Byte 4:
	4		The User Cell filtering criteria (for Transmit User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 Control Register.
		prod	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 4" permits the user to define the User Cell Filtering criteria for "Octet # 4" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 4" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 4" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	roduct C	are to	Witing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 4" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 4".
	The product of the data and ma	S	Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 4" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 4" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 4").

Table 281: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Filtered Cell Count – Byte 3 (Address = 0xNF6C)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	Transmit User Cell Filter # 2 – Filtered Cell Count[31:24]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION				
7 – 0	Transmit User Cell	RUR	Transmit User Cell Filter # 2 – Filtered Cell Count[31:24]:				
	Filter # 2 – Filtered Cell Count[31:24]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Filtered Cell Count – Bytes 2" through "0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 2 since the last read of this register.				
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – User Cell Filter # 2" Register (Address = 0xNF63), these register bits will be incremented anytime User Cell Filter # 2 performs any of the following functions.				
			Discards an incoming "User Cell".				
			 Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer. 				
			Both the above actions.				
			This particular register contains the MSB (Most Significant Byte) value for this 32-bit expression.				
		, ot s	Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x000000000").				



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 282: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Filtered Cell Count – Byte 2 (Address = 0xNF6D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit User Cell Filter # 2 – Filtered Cell Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

Transmit User Cell Filter # 2 – Filtered Cell Count[23:16]	RUR	Transmit User Cell Filter # 2 – Filtered Cell Count[23:16]: These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Filtered Cell					
		Count — Bytes 3, 1 and 0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 2 since the last read of this register.					
		Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Transmit User Cell Filter # 2" Register (Address = 0xNF63), these register bits will be incremented anytime User Cell Filter # 2 performs any of the following functions. • Discards an incoming "User Cell".					
		Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer.					
		Both the above actions.					
		Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x000000000").					
	Theda	The product of and many and ma					

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 283: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Filtered Cell Count – Byte 1 (Address = 0xNF6E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	Transmit User Cell Filter # 2 – Filtered Cell Count[15:8]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION				
7 – 0	Transmit User Cell	RUR	Transmit User Cell Filter # 2 – Filtered Cell Count[15:8]:				
	Filter # 2 – Filtered Cell Count[15:8]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Filtered Cell Count – Bytes 3, 2 and 0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 2 since the last read of this register.				
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Transmit User Cell Filter # 2" Register (Address = 0xNF63), these register bits will be incremented anytime Transmit User Cell Filter # 2 performs any of the following functions				
			Discards an incoming "User Cell". Conica (Conica (Conica Cell") and revites the "coni".				
			Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer.				
			Both the above actions.				
			Notes: If the number of "filtered cells" reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x000000000").				

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 284: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Filtered Cell Count – Byte 0 (Address = 0xNF6F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit User Cell Filter # 2 – Filtered Cell Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Transmit User Cell Filter # 2 – Filtered	RUR	Transmit User Cell Filter # 2 – Filtered Cell Count[7:0]:
	Cell Count[7:0]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Filtered Cell Count – Bytes 3" through "1" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 2 since the last read of this register.
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Transmit User Cell Filter # 2" Register (Address = 0xNF63), these register bits will be incremented anytime Transmit User Cell Filter # 2 performs any of the following functions.
			Discards an incoming "User Cell".
			Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer.
			Both the above actions.
			This particular register contains the LSB (Least Significant Byte) value for this 32-bit expression.
			Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").
	thepr	andn	"OxFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").

Table 285: Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Filter 3 (Address = 0xNF63)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused				Transmit User Cell Filter # 3 Enable	Copy Cell Enable	Discard Cell Enable	Filter if Pattern Match
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3	Transmit User Cell Filter # 3	R/W	Transmit User Cell Filter #3 – Enable:
	Enable		This READ/WRITE bit-field permits the user to either enable or disable Transmit User Cell Filter # 3.
			If the user enables Transmit User Cell Filter # 3, then Transmit User Cell Filter # 3 will function per the configuration settings in Bits 2 through 0, within this register.
			If the user disables Transmit User Cell Filter # 3, then Transmit User Cell Filter # 3 then all cells that are applied to the input of Transmit User Cell Filter # 3 will pass through to the output of Transmit User Cell Filter # 3.
		N.C	0 - Disables Transmit User Cell Filter # 3.
		1110	Enables Transmit User Cell Filter # 3.
2	Copy Cell Enable	R/W	Copy Cell Enable – Transmit User Cell Filter # 3:
	duct of P	rpe of	This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 3 (within the Transmit ATM Cell Processor Block) to copy all cells that have header byte patterns that comply with the "user-defined" criteria, per Transmit User Cell Filter # 3, or to NOT copy any of these cells.
	2 Copy Cell Enable The Product are and many the product and many the product and many the product are and many the product and the product are al		If the user configures Transmit User Cell Filter # 3 to copy all cells complying with a certain "header-byte" pattern, then a copy (or replicate) of this "compliant" ATM cell will be routed to the Transmit Cell Extraction Buffer.
			If the user configures Transmit User Cell Filter # 3 to NOT copy all cells complying with a certain "header-byte" pattern, then NO copies (or replicates) of these "compliant" ATM cells will be made nor will any be routed to the Transmit Cell Extraction Buffer.
			0 – Configures Transmit User Cell Filter # 3 to NOT copy any cells that have header byte patterns which are compliant with the "user-defined" filtering criteria.
			1 – Configures Transmit User Cell Filter # 3 to copy any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria, and to route these copies (of cells) to the Transmit Cell Extraction Buffer.
			Notes: This bit-field is only active if "Transmit User Cell Filter # 3" has been enabled.
1	Discard Cell Enable	R/W	Discard Cell Enable – Transmit User Cell Filter # 3:
			This READ/WRITE bit-field permits the user to either

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			configure Transmit User Cell Filter # 3 (within the Transmit ATM Cell Processor Block) to discard all cells that have header byte patterns that comply with the "user-defined" criteria, per Transmit User Cell Filter # 3, or NOT discard any of these cells.
			If the user configures Transmit User Cell Filter # 3 to NOT discarded any cells that is compliant with a certain "header-byte" pattern, then the cell will be retained for further processing.
			0 – Configures Transmit User Cell Filter # 3 to NOT discard any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria.
			1 – Configures Transmit User Cell Filter # 3 to discard any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria.
			Notes: This bit-field is only active if "Transmit User Cell Filter # 3" has been enabled.
0	Filter if Pattern Match	R/W	Filter if Pattern Match Transmit User Cell Filter # 3:
			This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 3 to filter (based upon the configuration settings for Bits 1 and 2, in this register) ATM cells with header bytes that match the "user-defined" header byte patterns, or to filter ATM cells with header bytes that do NOT match the "user-defined" header byte patterns. 0 = Configures Transmit User Cell Filter # 3 to filter user cells that do NOT match the header byte patterns (as defined in
		Prodi	the "" registers). 1 Configures Transmit User Cell Filter # 3 to filter user cells that do match the header byte patterns (as defined in the " " registers).
			Notes: This bit-field is only active if "Transmit User Cell Filter # 3" has been enabled.
	The product of and ma	y not	

Table 286: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 1 (Address = 0xNF64)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	Transmit User Cell Filter # 3 – Pattern Register – Byte 1 [7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 3 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 3 – Pattern Register – Header Byte 1:
	'		The User Cell filtering criteria (for Transmit User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 Control Register.
		oducte	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Register – Header Byte 1" permits the user to define the User Cell Filtering criteria for "Octet # 1" of the incoming User Cell. The user will write the header byte pattern (for Octet 1) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Register – Header Byte 1" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of product are	in of	

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 287: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 2 (Address = 0xNF65)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit User Cell Filter # 3 – Pattern Register – Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 3 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 3 – Pattern Register – Header Byte 2:
	2		The User Cell filtering criteria (for Transmit User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 Control Register.
		prodi	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Register – Header Byte 2" permits the user to define the User Cell Filtering criteria for "Octet # 2" of the incoming User Cell. The user will write the header byte pattern (for Octet 2) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Register – Header Byte 2" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of the data and ma	are to	

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 288: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 3 (Address = 0xNF66)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit User Cell Filter # 3 – Pattern Register – Byte 3 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 3 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 3 – Pattern Register – Header Byte 3:
	3	oducte	The User Cell filtering criteria (for Transmit User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 Control Register. This READ/WRITE register, along with the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Register - Header Byte 3" permits the user to define the User Cell Filtering criteria for "Octet # 3" of the incoming User Cell. The user will write the header byte pattern (for Octet 3) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Register - Header Byte 3" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of and may no	the of	

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 289: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 4 (Address = 0xNF67)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit User Cell Filter # 3 – Pattern Register – Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 3 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 3 – Pattern Register – Header Byte 4:
	4		The User Cell filtering criteria (for Transmit User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 Control Register.
		orodi	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Register – Header Byte 4" permits the user to define the User Cell Filtering criteria for "Octet # 4" of the incoming User Cell. The user will write the header byte pattern (for Octet 4) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Register – Header Byte 4" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of and ma	are to	2010

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 290: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Register – Byte 1 (Address = 0xNF68)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit User Cell Filter # 3 – Check Register – Byte 1 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 3 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 3 – Check Register – Header Byte 1:
	1		The User Cell filtering criteria (for Transmit User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 Control Register.
	70	odució	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 1" permits the user to define the User Cell Filtering criteria for "Octet # 1" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 1" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 1" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	roduct or b	the of	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 1" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 1".
	The product or product are		Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 1" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 1" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 1").



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 291: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Register – Byte 2 (Address = 0xNF69)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit User Cell Filter # 3 – Check Register – Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 3 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 3 – Check Register – Header Byte 2:
	2		The User Cell filtering criteria (for Transmit User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 Control Register.
		prodi	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 2" permits the user to define the User Cell Filtering criteria for "Octet # 2" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 2" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 2" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	roduct co	ale to	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 2" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 2".
	The product of and man		Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 2" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 2" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 2").

Table 292: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Register – Byte 3 (Address = 0xNF6A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit User Cell Filter # 3 – Check Register – Byte 3 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 3 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 3 – Check Register – Header Byte 3:
	3		The User Cell filtering criteria (for Transmit User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 Control Register.
		odució	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 3" permits the user to define the User Cell Filtering criteria for "Octet # 3" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 3" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 3" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	roduct or s	the of	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 3" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 3".
	The product or product are		Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 3" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 3" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 3").



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 293: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Register – Byte 4 (Address = 0xNF6B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit User Cell Filter # 3 – Check Register – Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 3 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 3 – Check Register – Header Byte 4:
	4		The User Cell filtering criteria (for Transmit User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 Control Register.
		, prod	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter #3 – Pattern Register – Header Byte 4" permits the user to define the User Cell Filtering criteria for "Octet #4" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 4" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter #3 – Pattern Register – Header Byte 4" by the User Cell Filter, when determine whether to "filter" a given User Cell. Wtiting a "1" to a particular bit-field in this register, forces the
	roduct (c	are to	Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 4" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 4".
	The product of the data and ma	S	Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 4" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 4" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 4").

Table 294: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Filtered Cell Count – Byte 3 (Address = 0xNF6C)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit User Cell Filter # 3 – Filtered Cell Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell	RUR	Transmit User Cell Filter # 3 – Filtered Cell Count[31:24]:
	Filter # 3 – Filtered Cell Count[31:24]	-	These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Filtered Cell Count – Bytes 2" through "0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 3 since the last read of this register.
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – User Cell Filter # 3" Register (Address = 0xNF63), these register bits will be incremented anytime User Cell Filter # 3 performs any of the following functions.
			Discards an incoming "User Cell".
			 Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer.
			Both the above actions.
			This particular register contains the MSB (Most Significant Byte) value for this 32-bit expression.
		, of	Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").
	The production	neet at	e be

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 295: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Filtered Cell Count – Byte 2 (Address = 0xNF6D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit User Cell Filter # 3 – Filtered Cell Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION		
7 – 0	Transmit User Cell	RUR	Transmit User Cell Filter # 3 – Filtered Cell Count[23:16]:		
	Filter # 3 – Filtered Cell Count[23:16]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Filtered Cell Count – Bytes 3, 1 and 0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 3 since the last read of this register.		
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Transmit User Cell Filter # 3" Register (Address = 0xNF63), these register bits will be incremented anytime User Cell Filter # 3 performs any of the following functions. • Discards an incoming "User Cell".		
			Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer.		
			Both the above actions.		
			Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").		
Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").					
		•			

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 296: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Filtered Cell Count – Byte 1 (Address = 0xNF6E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Transmit User Cell Filter # 3 – Filtered Cell Count[15:8]						
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 3 – Filtered	RUR	Transmit User Cell Filter # 3 – Filtered Cell Count[15:8]:
	Cell Count[15:8]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Filtered Cell Count – Bytes 3, 2 and 0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 3 since the last read of this register.
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Transmit User Cell Filter # 3" Register (Address = 0xNF63), these register bits will be incremented anytime Transmit User Cell Filter # 3 performs any of the following functions
			Discards an incoming "User Cell".
		Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer.	
			Both the above actions.
			Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x000000000").
	The production of the producti	neet at	eno oro

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 297: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Filtered Cell Count – Byte 0 (Address = 0xNF6F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit User Cell Filter # 3 – Filtered Cell Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 3 – Filtered	RUR	Transmit User Cell Filter # 3 – Filtered Cell Count[7:0]:
	Cell Count[7:0]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Filtered Cell Count – Bytes 3" through "1" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 3 since the last read of this register.
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Transmit User Cell Filter # 3" Register (Address = 0xNF63), these register bits will be incremented anytime Transmit User Cell Filter # 3 performs any of the following functions.
			Discards an incoming "User Cell".
			 Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer. Both the above actions.
			This particular register contains the LSB (Least Significant Byte) value for this 32-bit expression.
			Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x000000000").
	Thepr	andn	"OxFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").

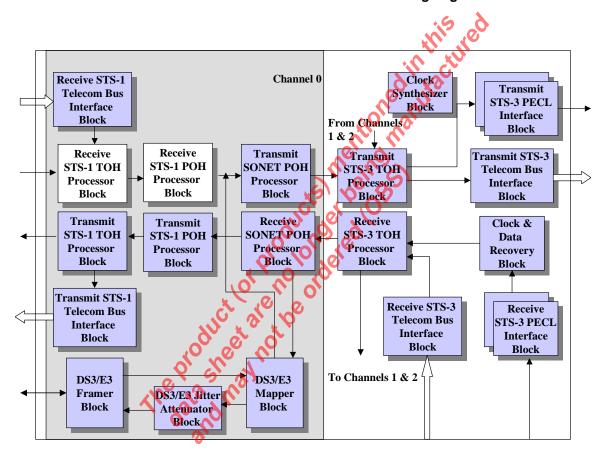
1.9 RECEIVE STS-1 TOH AND POH PROCESSOR BLOCK

The register map for the Receive STS-1 TOH and POH Processor Block is presented in the Table below. Additionally, a detailed description of each of the "Receive STS-1 TOH and POH Processor" block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33 device, with the "Receive STS-1 TOH and POH Processor Blocks "highlighted" is presented below in

Figure 10

Figure 10: Illustration of the Functional Block Diagram of the XRT94L33 device, with the Receive STS-1 TOH and POH Processor Blocks "High-lighted".







1.9.1 RECEIVE STS-1 TOH AND POH PROCESSOR BLOCK REGISTER

Table 298: Receive STS-1 TOH and POH Processor Block Control Register Address Map

Individual Register Address	Address Location	REGISTER NAME	DEFAULT VALUES
0x00 - 0x02	0xN000 - 0xN102	Reserved	0x00
0x03	0xN103	Receive STS-1 Transport Control Register – Byte 0	0x00
0x04, 0x05	0xN104 – 0xN105	Reserved	0x00
0x06	0xN106	Receive STS-1 Transport Status Register – Byte 1	0x00
0x07	0xN107	Receive STS-1 Transport Status Register – Byte 0	0x02
0x08	0xN108	Reserved	0x00
0x09	0xN109	Receive STS-1 Transport Interrupt Status Register – Byte 2	0x00
0x0A	0xN10A	Receive STS-1 Transport Interrupt Status Register – Byte 1	0x00
0x0B	0xN10B	Receive STS-1 Transport Interrupt Status Register – Byte 0	0x00
0x0C	0xN10C	Reserved	0x00
0x0D	0xN10D	Receive STS-1 Transport Interrupt Enable Register – Byte 2	0x00
0x0E	0xN10E	Receive STS-1 Transport Interrupt Enable Register – Byte 1	0x00
0x0F	0xN10F	Receive STS-1 Transport Intetrupt Enable Register – Byte 0	0x00
0x10	0xN110	Receive STS-1 Transport B1 Byte Error Count – Byte 3	0x00
0x11	0xN111	Receive STS-1 Transport B1 Byte Error Count – Byte 2	0x00
0x12	0xN112	Receive STS-1 Transport B1 Byte Error Count – Byte 1	0x00
0x13	0xN113	Receive STS-1 Transport B1 Byte Error Count – Byte 0	0x00
0x14	0xN114	Receive STS-1 Transport B2 Byte Error Count – Byte 3	0x00
0x15	0xN115	Receive STS-1 Transport B2 Byte Error Count – Byte 2	0x00
0x16	0xN116	Receive STS-1 Transport B2 Byte Error Count – Byte 1	0x00
0x17	0xN117	Receive STS-1 Transport B2 Byte Error Count – Byte 0	0x00
0x18	0xN118	Receive STS-1 Transport REI-L Error Count – Byte 3	0x00
0x19	0xN119	Receive STS-1 Transport REI-L Error Count – Byte 2	0x00
0x1A	0xN11A	Receive STS-1 Transport REI-L Error Count – Byte 1	0x00
0x1B	0xN11B	Receive STS-1 Transport REI-L Error Count – Byte 0	0x00
0x1C	0xN11C	Reserved	0x00
0x1D, 0x1E	0xN11D – 0xN11E	Reserved	0x00
0x1F	0xN11F	Receive STS-1 Transport – Received K1 Byte Value Register	0x00

INDIVIDUAL REGISTER ADDRESS	Address Location	REGISTER NAME	DEFAULT VALUES
0x20 - 0x22	0xN120 - 0xN122	Reserved	0x00
0x23	0xN123	Receive STS-1 Transport – Received K2 Byte Value Register	0x00
0x24 - 0x26	0xN124 - 0xN126	Reserved	0x00
0x27	0xN127	Receive STS-1 Transport – Received S1 Byte Value Register	0x00
0x28 - 0x2D	0xN128 – 0xN12D	Reserved	0x00
0x2E	0xN12E	Receive STS-1 Transport – LOS Threshold Value – MSB	0xFF
0x2F	0xN12F	Receive STS-1 Transport – LOS Threshold Value LSB	0xFF
0x30	0xN130	Reserved	0x00
0x31	0xN131	Receive STS-1 Transport – Receive SF Set Monitor Interval – Byte 2	0x00
0x32	0xN132	Receive STS-1 Transport – Receive SF Set Monitor Interval – Byte 1	0x00
0x33	0xN133	Receive STS-1 Transport - Receive SF Set Monitor Interval - Byte 0	0x00
0x34, 0x35	0xN134, 0xN135	Reserved	0x00
0x36	0xN136	Receive STS-1 Transport - Receive SF Set Threshold - Byte 1	0x00
0x37	0xN137	Receive STS-1 Transport - Receive SF Set Threshold - Byte 0	0x00
0x38, 0x39	0xN138 - 0xN139	Resetved	0x00
0x3A	0xN13A	Receive STS-1 Transport – Receive SF Clear Threshold – Byte 1	0x00
0x3B	0xN13B	Receive STS-1 Transport – Receive SF Clear Threshold – Byte 0	0x00
0x3C	0xN13C	Reserved	0x00
0x3D	0xN13D	Receive STS-1 Transport – Receive SD Set Monitor Interval – Byte	0x00
0x3E	0xN13E	Receive STS-1 Transport – Receive SD Set Monitor Interval – Byte	0x00
0x3F	0xN13F	Receive STS-1 Transport – Receive SD Set Monitor Interval – Byte 0	0x00
0x40, 0x41	0xN140 - 0xN141	Reserved	0x00
0x42	0xN142	Receive STS-1 Transport – Receive SD Set Threshold – Byte 1	0x00
0x43	0xN143	Receive STS-1 Transport – Receive SD Set Threshold – Byte 0	0x00
0x44, 0x45	0xN144, 0xN145	Reserved	0x00
0x46	0xN146	Receive STS-1 Transport – Receive SD Clear Threshold – Byte 1	0x00

Experience Our

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

INDIVIDUAL REGISTER ADDRESS	Address Location	REGISTER NAME	DEFAULT VALUES
0x47	0xN147	Receive STS-1 Transport – Receive SD Clear Threshold – Byte 0	0x00
0x48 – 0x4A	0xN14B – 0xN14A	Reserved	0x00
0x4B	0xN14B	Receive STS-1 Transport – Force SEF Condition	0x00
0x4C - 0x4E	0xN14C - 0xN14E	Reserved	0x00
0x4F	0xN14F	Receive STS-1 Transport – Receive J0 Byte Trace Buffer Control Register	0x00
0x50 – 0x51	0xN150 – 0xN151	Reserved	
0x52	0xN152	Receive STS-1 Transport – Receive SD Burst Error Count Tolerance – Byte 1	0x00
0x53	0xN153	Receive STS-1 Transport – Receive SD Burst Error Count Tolerance – Byte 0	0x00
0x54, 0x55	0xN154, 0xN155	Reserved	0x00
0x56	0xN156	Receive STS-1 Transport – Receive ST Burst Error Count Tolerance – Byte 1	0x00
0x57	0xN157	Receive STS-1 Transport Receive SF Burst Error Count Tolerance – Byte 0	0x00
0x58	0xN158	Reserved	0x00
0x59	0xN159	Receive STS-OTransport Receive SD Clear Monitor Interval – Byte 2	0x00
0x5A	0xN15A	Receive STS-1 Transport - Receive SD Clear Monitor Interval - Byte 1	0x00
0x5B	0xN15B	Receive STS-1 Transport - Receive SD Clear Monitor Interval - Byte 0	0x00
0x5C	0xN15C	Reserved	0x00
0x5D	0xN15D	Receive STS-1 Transport – Receive SF Clear Monitor Interval – Byte 2	0x00
0x5E	0xN15E	Receive STS-1 Transport – Receive SF Clear Monitor Interval – Byte 1	0x00
0x5F	0xN15F	Receive STS-1 Transport – Receive SF Clear Monitor Interval – Byte 0	0x00
0x60 - 0x62	0xN160 – 0xN162	Reserved	0x00
0x63	0xN163	Receive STS-1 Transport – Auto AIS Control Register	0x00
0x64 – 0x6A	0xN164 – 0xN16A	Reserved	0x00
0x6B	0xN16B	Receive STS-1 Transport – Auto AIS (in Downstream STS-1s) Control Register	0x00

Individual Register Address	Address Location	REGISTER NAME	DEFAULT VALUES
0x6C - 0x82	0xN16C - 0xN182	Reserved	0x00
0x83	0xN183	Receive STS-1 Path – Control Register – Byte 2	0x00
0x84, 0x85	0xN184 - 0xN185	Reserved	0x00
0x86	0xN186	Receive STS-1 Path – Control Register – Byte 1	
0x87	0xN187	Receive STS-1 Path – Status Register – Byte 0	0x00
0x88	0xN188	Reserved	0x00
0x89	0xN189	Receive STS-1 Path – Interrupt Status Register – Byte 2	0x00
0x8A	0xN18A	Receive STS-1 Path – Interrupt Status Register – Byte 1	0x00
0x8B	0xN18B	Receive STS-1 Path – Interrupt Status Register – Byte 0	0x00
0x8C	0xN18C	Reserved	0x00
0x8D	0xN18D	Receive STS-1 Path – Interrupt Enable Register – Byte 2	0x00
0x8E	0xN18E	Receive STS-1 Path – Interrupt Enable Register – Byte 1	0x00
0x8F	0xN18F	Receive STS-1 Path Interrupt Enable Register – Byte 0	0x00
0x90 - 0x92	0xN190 - 0xN192	Reserved	0x00
0x93	0xN193	Receive STS Path SONET Receive RDI-P Register	0x00
0x94, 0x95	0xN194, 0xN195	Reserved	0x00
0x96	0xN196	Receive STS-1 Path - Received Path Label Value (C2 Byte) Register	0x00
0x97	0xN197	Receive STS-1 Path – Expected Path Label Value (C2 Byte) Register	0x00
0x98	0xN198	Receive STS-1 Path – B3 Error Count Register – Byte 3	0x00
0x99	0xN199	Receive STS-1 Path – B3 Error Count Register – Byte 2	0x00
0x9A	0xN19A	Receive STS-1 Path – B3 Error Count Register – Byte 1	0x00
0x9B	0xN19B	Receive STS-1 Path – B3 Error Count Register – Byte 0	0x00
0x9C	0xN19C	Receive STS-1 Path – REI-P Error Count Register – Byte 3	0x00
0x9D	0xN19D	Receive STS-1 Path – REI-P Error Count Register – Byte 2	0x00
0x9E	0xN19E	Receive STS-1 Path – REI-P Error Count Register – Byte 1	0x00
0x9F	0xN19F	Receive STS-1 Path – REI-P Error Count Register – Byte 0	0x00
0xA0 - 0xA5	0xN1A0 – 0xN1A5	Reserved	0x00
0xA6	0xN1A6	Receive STS-1 Path – Pointer Value Register – Byte 1	0x00
0xA7	0xN1A7	Receive STS-1 Path – Pointer Value Register – Byte 0	0x00

XRT94L33

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Individual Register Address	Address Location	REGISTER NAME	DEFAULT VALUES
0xA8 – 0xBA	0xN1A8 – 0xN1BA	Reserved	0x00
0xBB	0xN1BB	Receive STS-1 Path – AUTO AIS Control Register	0x00
0xBC - 0xBE	0xN1BC – 0xN1BE	Reserved	0x00
0xBF	0xN1BF	Receive STS-1 Path – Serial Port Control Register	0x00
0xC0 - 0xC2	0xN1C0 - 0xN1C2	Reserved	0x00
0xC3	0xN1C3	Receive STS-1 Path – SONET Receive Auto Alarm Register – Byte 0	0x00
0xC4 - 0xD2	0xN1C4 - 0xN1D2	Reserved	
0xD3	0xN1D3	Receive STS-1 Path – Receive J1 Byte Capture Register	0x00
0xC4-0xC6	0xN1C4 - 0xN1C6	Reserved	0x00
0xD7	0xN1D7	Receive STS-1 Path – Receive B3 Byte Capture Register	0x00
0xD8 – 0xDA	0xN1D8 – 0xN1DA	Reserved	0x00
0xDB	0xN1DB	Receive STS-1 Path – Receive C2 Byte Capture Register	0x00
0xDC - 0xDE	0xN1DC – 0xN1DE	Reserved	0x00
0xDF	0xN1DF	Receive STS-1 Path - Receive G1 Byte Capture Register	0x00
0xE0 - 0xE2	0xN1E0 - 0xN1E2	Reserved	0x00
0xE3	0xN1E3	Receive STS-1 Path - Receive F2 Byte Capture Register	0x00
0xE4 - 0xE6	0xN1E4 – 0xN1E6	Reserved	0x00
0xE7	0xN1E7	Receive STS-1 Path – Receive H4 Byte Capture Register	0x00
0xE8 – 0xEA	0xN1E8 0xN1EA	Reserved	0x00
0xEB	0xN1EB	Receive STS-1 Path – Receive Z3 Byte Capture Register	0x00
0xEC - 0xEE	0xN1EC - 0xN1EE	Reserved	0x00
0xEF	0xN1EF	Receive STS-1 Path – Receive Z4 (K3) Byte Capture Register	0x00
0xF0 - 0xF2	0xN1F0 – 0xN1F2	Reserved	0x00
0xF3	0xN1F3	Receive STS-1 Path – Receive Z5 Byte Capture Register	0x00
0xF6 - 0xFF	0xN1F6 – 0xN1FF	Reserved	0x00

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

1.9.2 RECEIVE STS-1 TOH AND POH PROCESSOR BLOCK REGISTER DESCRIPTION

Table 299: Receive STS-1 Transport Control Register – Byte 0 (Address Location = 0xN103)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	SF Detect Enable	SD Detect Enable	Descramble Disable	Unused	REI-L Error Type	B2 Error Type	B1 Error Type
R/O	R/W	R/W	R/W	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Unused	R/O	nis ed
6	SF Detect	R/W	Signal Failure (SF) Detect Enable:
	Enable		This READ/WRITE bit-field permits the user to enable or disable SF Detection by the Receive STS-1 TOH Processor block.
			0 – SF Detection is disabled.
			1 – SF Detection is enabled
5	SD Detect	R/W	Signal Degrade (SD) Detect Enable:
	Enable		This READ/WRITE bit-field permits the user to enable or disable SD Detection by the Receive STS-1 TOH Processor block.
			0 – SD Detection is disabled.
			1 – SB Detection is enabled.
4	Descramble	R/W	De-Scramble Disable:
	Disable	الخار	This READ/WRITE bit-field permits the user to either enable or disable descrambling by the Receive STS-1 TOH Processor block, associated with channel N.
		All	0 – De-Scrambling is enabled.
		10,46	1 De-Scrambling is disabled.
3	Unused	R/O	
2	REI-L Error	R/W	REI-L Error Type:
	Туре	alle	This READ/WRITE bit-field permits the user to specify how the "Receive Transport REI-L Error Count" register is incremented.
			0 – Configures the Receive STS-1 TOH Processor block to count REI-L Bit Errors.
			In this case the "Receive Transport REI-L Error Count" register will be incremented by the value of the lower nibble within the M0/M1 byte.
			1 – Configures the Receive STS-1 TOH Processor block to count REI-L Frame Errors.
			In this case the "Receive Transport REI-L Error Count" register will be incremented each time the Receive STS-1 TOH Processor block receives a "non-zero" M0/M1 byte.
1	B2 Error	R/W	B2 Error Type:
	Type		This READ/WRITE bit-field permits the user to specify how the "Receive

EXAR Experience Our Connectivit

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

		,
		Transport B2 Error Count" register is incremented.
		0 - Configures the Receive STS-1 TOH Processor block to count B2 bit errors.
		In this case, the "Receive Transport B2 Error Count" register will be incremented by the number of bits, within the B2 value, that is in error.
		1 – Configures the Receive STS-1 TOH Processor block to count B2 frame errors.
		In this case, the "Receive Transport B2 Error Count" register will be incremented by the number of erred STS-1 frames.
B1 Error	R/W	B1 Error Type:
Туре		This READ/WRITE bit-field permits the user to specify how the "Receive Transport B1 Error Count" register is incremented.
		0 - Configures the Receive STS-1 TOH Processor block to count B1 bit errors.
		In this case, the "Receive Transport B1 Error Count" register will be incremented by the number of bits, within the B1 value, that is in error.
		1 - Configures the Receive STS-1 TOH Processor block to count B2 bit errors.
		In this case, the "Receive Transport B1 Error Count" register will be incremented by the number of erred STS-1 frames.
	ne produ	In this case, the "Receive Transport B1 Error Count" register will be incremented by the number of erred STS-1 frames.
	Туре	Туре

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 300: Receive STS-1 Transport Status Register – Byte 1 (Address Location= 0xN106)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Unused	J0 Message Mismatch	J0 Message Unstable	AIS_L Detected		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	Description
7 – 3	Unused	R/O	
2	J0 Message Mismatch	R/O	J0 – Section Trace Mismatch Indicator: This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring the Section Trace Mismatch condition. The Receive STS-1 TOH Processor block will declare a J0 (Section Trace) Mismatch condition, whenever it accepts a J0 Message that differs from the "Expected J0 Message". 0 – Section Trace Mismatch Condition is NOT declared. 1 – Section Trace Mismatch Condition is currently declared.
1	J0 Message Unstable	R/O	J0 – Section Trace Unstable Indicator: This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring the Section Trace Instability condition. The Receive STS-1 TOH Processor block will declare a J0 (Section Trace) Unstable condition, whenever the "J0 Unstable" counter reaches the value 8. The "J0 Unstable" counter will be incremented for each time that it receives a J0 message that differs from the "Expected J0 Message". The "J0 Unstable" counter is cleared to "0" whenever the Receive STS-3 TOH Processor block has received a given J0 Message 3 (or 5) consecutive times. Note: Receiving a given J0 Message 3 (or 5) consecutive times also sets this bit-field to "0". 1 – Section Trace Instability condition is NOT declared.
0	AIS_L Detected	R/O	This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently detecting an AIS-L (Line AIS) pattern in the incoming STS-1 data stream. AIS-L is declared if bits 6, 7 and 8 (e.g., the Least Significant Bits, within the K2 byte) value the value "1, 1, 1" for five consecutive STS-1 frames. 0 – AIS-L is NOT currently declared. 1 – AIS-L is currently being declared.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 301: Receive STS-1 Transport Status Register – Byte 0 (Address Location = 0xN107)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
RDI-L	S1 Unstable	APS	SF	SD	LOF	SEF	LOS
Declared		Unstable	Detected	Detected	Defect	Defect	Defect
					Detected	Declared	Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	RDI-L	R/O	RDI-L Indicator:
	Declared		This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is detecting a Line-Remote Defect Indicator, in the incoming STS-1 signal. RDI-L is declared when bits 6, 7 and 8 (e.g., the three least significant bits) of the K2 byte contains the 1, 1, 0" pattern in 5 consecutive STS-1 frames.
			0 – RDI-L is NOT being declared
			1 – RDI-L is currently being declared.
6	S1 Unstable	R/O	S1 Unstable Condition:
			This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring the "S1 Byte Instability" condition. The Receive STS-1 TOH Processor block will declare an "S1 Byte Instability" condition whenever the "S1 Byte Unstable Counter" reaches the value 32. The "S1 Byte Unstable Counter" is incremented for each time that the Receive STS-1 TOH Processor block receives an S1 byte that differs from the previously received S1 byte. The "S1 Byte Unstable Counter" is cleared to "0" when the same S1 byte is received for 8 consecutive STS-1 frames.
			Note: Receiving a given S1 byte, in 8 consecutive STS-1 frames also sets this bit-field to "0".
			0 - S1/mstability Condition is NOT declared.
		50.	1 – S1 Instability Condition is currently declared.
5	APS Unstable	R/O	APS (K1, K2 Byte) Instability:
	N.	data	This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring the "K1, K2 Byte Unstable" condition. The Receive STS-1 TOH Processor block will declare a "K1, K2 Byte Unstable" condition whenever the Receive STS-1 TOH Processor block fails to receive the same set of K1, K2 bytes, in 12 consecutive STS-1 frames. The "K1, K2 Byte Instability" condition is cleared whenever the STS-1 Receiver receives a given set of K1, K2 byte values in three consecutive STS-1 frames.
			0 – K1, K2 Instability Condition is NOT declared.
			1 – K1, K2 Instability Condition is currently declared.
4	SF Detected	R/O	SF (Signal Failure) Defect Indicator:
			This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring the SF defect. The SF defect is declared when the number of B2 errors observed over a given time interval exceeds a certain threshold.
			0 – SF Defect is NOT being declared.
			This bit is set to "0" when the number of B2 errors (accumulated over a given

	1		
			interval of time) does not exceed the "SF Declaration" threshold.
			1 – SF Defect is being declared.
			This bit is set to "1" when the number of B2 errors (accumulated over a given interval of time) does exceed the "SF Declaration" threshold.
3	SD Detected	R/O	SD (Signal Degrade) Defect Indicator:
			This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring the SD defect. The SD defect is declared when the number of B2 errors observed over a given time interval exceeds a certain threshold.
			0 – SD Defect is NOT being declared.
			This bit is set to "0" when the number of B2 errors (accumulated over a given interval of time) does not exceed the "SD Declaration" threshold.
			1 – SD Defect is being declared.
			This bit is set to "1" when the number of B2 errors (accumulated over a given interval of time) does exceed the "SD Declaration" threshold.
2	LOF	R/O	LOF (Loss of Frame) Indicator:
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring the LOF defect. The Receive STS-1 TOH Processor block will declare the LOF defect if it has been declaring the SEF condition for 24 consecutive STS-1 frame periods. Once the LOF defect is declared, then the Receive STS-1 TOH Processor block will clear the LOF defect if it has not been declaring the SEF condition for 3ms (or 24 consecutive STS-1 frame periods).
			 0 - The Receive STS-1 TOH Processor block is NOT currently declaring the LOF condition. 1 - The Receive STS-1 TOH Processor block is currently declaring the LOF condition.
1	SEF	R/O	SEF (Severely Errored Frame):
	Defect Declared	roduct roshe	This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring an SEF condition. The Receive STS-1 TOH Processor block will declare an SEF condition if it detects Framing Alignment byte errors in four consecutive STS-1 frames. Once the SEF condition is declared the Receive STS-1 TOH Processor block will clear the SEF condition if it detects two consecutive STS-1 frames with un-erred framing alignment bytes.
	7, 8	9,79,	0 - Indicates that the Receive STS-1 TOH Processor block is NOT declaring
		9	the SEF condition. 1 – Indicates that the Receive STS-1 TOH Processor block is currently declaring the SEF condition.
0	LOS	R/O	LOS (Loss of Signal) Indicator:
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring an LOS (Loss of Signal) condition. The Receive STS-1 TOH Processor block will declare an LOS condition if it detects "LOS_THRESHOLD[15:0]" consecutive "All Zero" bytes in the incoming STS-1 data stream.
			Note: The user can set the "LOS_THRESHOLD[15:0]" value by writing the appropriate data into the "Receive STS-1 Transport – LOS Threshold Value" Register (Address Location= 0xN12E and 0xN12F).
			0 - Indicates that the Receive STS-1 TOH Processor block is NOT currently

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

	declaring an LOS condition.
	1 – Indicates that the Receive STS-1 TOH Processor block is currently declaring an LOS condition.

The product are no ordered (OBS)

The product are no be ordered (OBS)

Table 302: Receive STS-1 Transport Interrupt Status Register – Byte 2 (Address Location= 0xN109)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused						Change of AIS-L Interrupt Status	Change of RDI-L Interrupt Status
R/O	R/O	R/O	R/O	R/O	R/O	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 2	Unused	R/O	
1	Change of AIS-L Interrupt Status	RUR	Change of AIS-L (Line AIS) Condition Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change of AIS-L Condition" interrupt has occurred since the last read of this register. 0 – The "Change of AIS-L Condition" interrupt has not occurred since the last read of this register. 1 – The "Change of AIS-L Condition" interrupt has occurred since the last read of this register. Note: The user can obtain the current state of AIS-L by reading the contents of Bit 0 (AIS-L Defect Declared) within the "Receive STS-1 Transport Status Register – Byte 1" (Address Location= 0xN106).
0	Change of RDI-L Interrupt Status	RUR	Change of RDI-L (Line - Remote Defect Indicator) Condition Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change of RDI-L Condition" interrupt has occurred since the last read of this register. 0 - The "Change of RDI-L Condition" interrupt has not occurred since the last read of this register. - The "Change of RDI-L Condition" interrupt has occurred since the last read of this register. Note: The user can obtain the current state of RDI-L by reading out the state of Bit 7 (RDI-L Declared) within the "Receive STS-1 Transport Status Register - Byte 0" (Address Location= 0xN107).

Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 303: Receive STS-1 Transport Interrupt Status Register – Byte 1 (Address Location= 0xN10A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
New S1 Byte Interrupt Status	Change in S1 Unstable State Interrupt Status	Change in J0 Unstable State Interrupt Status	New J0 Message Interrupt Status	J0 Mismatch Interrupt Status	Unused	Change in APS Unstable State Interrupt Status	NEW K1K2 Byte Interrupt Status
RUR	RUR	RUR	RUR	RUR	R/O	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	Description
7	New S1 Byte Value Interrupt Status	RUR	New S1 Byte Value Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "New S1 Byte Value" Interrupt has occurred since the last read of this register. 0 – Indicates that the "New S1 Byte Value" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "New S1 Byte Value" interrupt has occurred since the last read of this register. Note: The user can obtain the value for this most recently accepted value of the S1 byte by reading the "Receive STS-1 Transport S1 Value" register (Address Location= 0xN127).
6	Change in S1 Byte Unstable State Interrupt Status Change in J0 Message Unstable State Interrupt	RUR	Change in S1 Byte Unstable State – Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change in S1 Byte Unstable State" Interrupt has occurred since the last read of this register. Indicates that the "Change in S1 Byte Unstable State" Interrupt has occurred since the last read of this register. I – Indicates that the "Change in S1 Byte Unstable State" Interrupt has not occurred since the last read of this register. Note: The user can obtain the current "S1 Unstable" state by reading the contents of Bit 6 (S1 Unstable) within the "Receive STS-1 Transport Status Register – Byte 0" (Address Location= 0xN107).
5	Change in J0 Message Unstable State Interrupt Status	RUR	Change of J0 (Section Trace) Message Unstable condition – Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change of J0 (Section Trace) Message Instability" condition interrupt has occurred since the last read of this register. 0 – Indicates that the "Change of J0 (Section Trace) Message Instability" condition interrupt has not occurred since the last read of this register. 1 – Indicates that the "Change of J0 (Section Trace) Message Instability" condition interrupt has occurred since the last read of this register.
4	New J0 Message Interrupt Status	RUR	New J0 Trace Message Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the

			"New J0 Trace Message" interrupt has occurred since the last
			read of this register. 0 – Indicates that the "New J0 Trace Message Interrupt" has not occurred since the last read of this register.
			1 – Indicates that the "New J0 Trace Message Interrupt" has occurred since the last read of this register.
			Note: The user can read out the contents of the "Receive J0 Trace Buffer", which is located at Address Locations 0xN300 through 0xN33F.
3	J0 Mismatch Interrupt Status	RUR	Change in J0 – Section Trace Mismatch Condition" Interrupt Status:
			This RESET-upon-READ bit-field indicates whether or not the "Change in J0 – Section Trace Mismatch Condition" interrupt has occurred since the last read of this register.
			0 – Indicates that the "Change in J0 – Section Trace Mismatch Condition" interrupt has not occurred since the last read of this register.
			1 – Indicates that the "Change in J0 – Section Trace Mismatch Condition" interrupt has occurred since the last read of this register.
			Note: The user can determine whether the "J0 – Section Trace Mismatch" condition is "cleared" or "declared" by feading the state of Bit 2 (J0_MIS) within the "Receive STS-1 Transport Status Register – Byte 1 (Address Location= 0xN106).
2	Unused	R/O	40,9
1	Change in APS Unstable State Interrupt Status	RUR	Change of APS (K1, K2 Byte) Instability Condition – Interrupt Status:
	Change in APS Unstable State Interrupt Status	Me ve	This RESET-upon-READ bit-field indicates whether or not the Change of APS (K1, K2 Byte) Instability Condition" interrupt has occurred since the last read of this register.
	orodine.	not	0 – Indicates that the "Change of APS (K1, K2 Byte) Instability Condition" interrupt has NOT occurred since the last read of this register.
	The data di		$1-\mbox{Indicates}$ that the "Change of APS (K1, K2 Byte) Instability Condition" interrupt has occurred since the last read of this register.
			Note: The user can determine whether the "K1, K2 Instability Condition" is being declared or cleared by reading out the contents of Bit 5 (APS_INV), within the "Receive STS-1 Transport Status Register – Byte 0" (Address Location= 0xN107).
0	New K1K2 Byte Interrupt Status	RUR	New K1, K2 Byte Value Interrupt Status:
	Status		This RESET-upon-READ bit-field indicates whether or not the "New K1, K2 Byte Value" Interrupt has occurred since the last read of this register.
			0 - Indicates that the "New K1, K2 Byte Value" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "New K1, K2 Byte Value" Interrupt has occurred since the last read of this register.
			Note: The user can obtain the contents of the new K1 byte by

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

contents of the "Receive STS-1 Transport K2 Value" Register (Address Location= 0xN123).

The product of products in the product of products in the product of products in the product of the product of

Table 304: Receive STS-1 Transport Interrupt Status Register – Byte 0 (Address Location= 0xN10B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Change of SF Condition Interrupt Status	Change of SD Condition Interrupt Status	Detection of REI-L Error Interrupt Status	Detection of B2 Error Interrupt Status	Detection of B1 Error Interrupt Status	Change of LOF Condition Interrupt Status	Change of SEF Interrupt Status	Change of LOS Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Change of SF	RUR	Change of Signal Failure (SF) Condition Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of SF Interrupt" has occurred since the last read of this register.
			0 - The "Change of SF Condition Interrupt" has NOT occurred since the last read of this register.
			1 – The "Change of SF Condition Interrupt" has occurred since the last read of this register.
			Note: The user can determine the current "SF" condition by reading out the state of Bit 4(SF Declared) within the "Receive STS-1 Transport Status Register – Byte 0 (Address Location= 0xN107).
6	Change of SD	RUR	Change of Signal Degrade (SD) Condition Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of SD Condition Interrupt" has occurred since the last read of this register.
			0 - The "Change of SD Condition Interrupt" has NOT occurred since the last read of this register.
		ري.	1 – The "Change of SD Condition Interrupt" has occurred since the last read of this register.
	o	odule	Note: The user can determine the current "SD" condition by reading out the state of Bit 3 (SD Declared) within the "Receive STS-1 Transport Status Register – Byte 0 (Address Location= 0xN107).
5	Detection of	RUR	Detection of Line – Remote Error Indicator Interrupt Status:
	REI-L Interrupt Status	andi	This RESET-upon-READ bit-field indicates whether or not the "Detection of Line – Remote Error Indicator" Interrupt has occurred since the last read of this register.
			0 - The "Detection of Line – Remote Error Indicator" Interrupt has NOT occurred since the last read of this register.
			1 – The "Detection of Line – Remote Error Indicator" Interrupt has occurred since the last read of this register.
4	Detection of B2	RUR	Detection of B2 Error Interrupt Status:
	Error Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of B2 Error Interrupt" has occurred since the last read of this register.
			0 - The "Detection of B2 Error Interrupt" has NOT occurred since the last read of this register.
			1 – The "Detection of B2 Error Interrupt" has occurred since the last read of this register.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

3	Detection of B1	RUR	Detection of B1 Error Interrupt Status:
	Error Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of B1 Error Interrupt" has occurred since the last read of this register.
			$\bf 0$ - The "Detection of B1 Error Interrupt" has NOT occurred since the last read of this register.
			1 - The "Detection of B1 Error Interrupt" has occurred since the last read of this register
2	Change of LOF	RUR	Change of Loss of Frame (LOF) Condition Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of LOF Condition" interrupt has occurred since the last read of this register.
			0 – The "Change of LOF Condition" interrupt has NOT occurred since the last read of this register.
			1 – The "Change of LOF Condition" interrupt has occurred since the last read of this register.
			Note: The user can determine the current "LOF" condition by reading out the state of Bit 2 (LOF Defect Declared) within the "Receive STS-1 Transport Status Register – Byte 0 (Address Location= 0xN107).
1	Change of SEF	RUR	Change of SEF Condition Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of SEF Condition" Interrupt has occurred since the last read of this register.
			0 – The "Change of SEF Condition" Interrupt has NOT occurred since the last read of this register
			1 – The "Change of SEF Condition" Interrupt has occurred since the last read of this register.
			Note: The user can determine the current "SEF" condition by reading out the state of Bit 1 (SEF Defect Declared) within the "Receive STS-1 Transport Status Register – Byte 0 (Address Location= 0xN107).
0	Change of LOS	RUR	Change of Loss of Signal (LOS) Condition Interrupt Status:
	Condition Interrupt Status	6	This RESET upon-READ bit-field indicates whether or not the "Change of LOS Condition" interrupt has occurred since the last read of this register.
		, bio	The "Change of LOS Condition" Interrupt has NOT occurred since the last read of this register.
	1/1/2	7313	1 The "Change of LOS Condition" Interrupt has occurred since the last read of this register.
			Note: The user can determine the current "LOS" status by reading out the contents of Bit 0 (LOS Defect Declared) within the Receive STS-1 Transport Status Register – Byte 0 (Address Location= 0xN107).

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 305: Receive STS-1 Transport Interrupt Enable Register – Byte 2 (Address Location= 0xN10D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused						Change of AIS-L Condition Interrupt Enable	Change of RDI-L Condition Interrupt Enable
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 2	Unused	R/O	
1	Change of AIS-L Condition Interrupt Enable	R/W	Change of AIS-L (Line AIS) Condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change of AIS-L Condition" interrupt. If the user enables this interrupt, then the XRT94L33 device will generate an interrupt in response to either of the following conditions. • When the Receive STS-1 TOH Processor block declares the "AIS-L" condition. • When the STS-1 Receiver clears the "AIS-L" condition. 0 – Disables the "Change of AIS-L Condition" Interrupt. 1 – Enables the "Change of AIS-L Condition" Interrupt.
0	Change of RDI-L Condition Interrupt Enable	R/W	Change of RDI-L (Line Remote Defect Indicator) Condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change of RDI-L Condition" interrupt. If the user enables this interrupt, then the XRT94L33 device will generate an interrupt in response to either of the following conditions. When the Receive STS-1 TOH Processor block declares the "RDI-L" condition. When the Receive STS-1 TOH Processor clears the "RDI-L" condition. 0 – Disables the "Change of RDI-L Condition" Interrupt.

Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 306: Receive STS-1 Transport Interrupt Enable Register – Byte 1 (Address Location= 0xN10E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
New S1 Byte Interrupt Enable	Change in S1 Byte Unstable State Interrupt Enable	Change in J0 Message Unstable State Interrupt Enable	New J0 Message Interrupt Enable	J0 Mismatch Interrupt Enable	Unused	Change in APS Unstable State Interrupt Enable	New K1K2 Byte Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	Description >
7	New S1 Byte Value	R/W	New S1 Byte Value Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to enable or disable the "New S1 Byte Value" Interrupt. If the user enables this interrupt, then the Receive STS-1 TOH Processor block will generate this interrupt anytime it receives and accepts a new S1 byte value. The Receive STS-1 TOH Processor block will accept a new S1 byte after it has received it for 8 consecutive STS-1 frames. 0 – Disables the "New S1 Byte Value" Interrupt. 1 – Enables the "New S1 Byte Value" Interrupt.
6	Change in S1	R/W	Change in S1 Byte Unstable State Interrupt Enable:
	Unstable State Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in \$1 Byte Unstable State" Interrupt. If the user enables this bit-field, then the Receive STS-1 TOH Processor block will generate an interrupt in response to either of the following conditions.
		k	When the Receive STS-1 TOH Processor block declares the "S1 Byte Instability" condition.
		duc	When the Receive STS-1 TOH Processor block clears the "S1 Byte Instability" condition.
		10,76	0 - Disables the "Change in S1 Byte Unstable State" Interrupt.
		(5)	Enables the "Change in S1 Byte Unstable State" Interrupt.
5	Change in J0 Message Unstable	R/W	Change of J0 (Section Trace) Message Instability condition Interrupt Enable:
	State Interrupt Enable	%	This READ/WRITE bit-field permits the user to either enable or disable the "Change of J0 Message Instability Condition" Interrupt. If the user enables this interrupt, then the Receive STS-1 TOH Processor block will generate an interrupt in response to either of the following conditions.
			Whenever the Receive STS-1 TOH Processor block declares the "Jo Message Instability" condition.
			Whenever the Receive STS-1 TOH Processor block clears the "Jo Message Instability" condition.
			0 – Disable the "Change of J0 Message Instability" Interrupt.
			1 – Enables the "Change of J0 Message Instability" Interrupt.
4	New J0 Message	R/W	New J0 Trace Message Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to enable or disable the "New J0 Trace Message" interrupt. If the user enables this interrupt, then the

0

New K1K2 Byte

Interrupt Enable

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			Receive STS-1 TOH Processor block will generate this interrupt anytime it receives and accepts a new J0 Trace Message. The Receive STS-1 TOH Processor block will accept a new J0 Trace Message after it has received it 3 (or 5) consecutive times.
			0 – Disables the "New J0 Trace Message" Interrupt.
			1 – Enables the "New J0 Trace Message" Interrupt.
3	J0 Mismatch Interrupt Enable	R/W	Change in "J0 – Section Trace Mismatch Condition" interrupt enable:
			This READ/WRITE bit-field permits the user to either enable or disable the "Change in J0 – Section Trace Mismatch condition" interrupt. If the user enables this interrupt, then the Receive STS-1 TOH Processor block will generate an interrupt in response to either of the following events.
			 a. The Receive STS-1 TOH Processor block declares a "J0 – Section Trace Mismatch" condition.
			b. The Receive STS-1 TOH Processor block clears the "J0 – Section Trace Mismatch" condition.
			Note: The user can determine whether the "JO – Section Trace Mismatch" condition is "cleared or "declared" by reading the state of Bit 2 (J0 MIS) within the "Receive STS-1 Transport Status Register – Byte 1 (Address Location= 0xN106).
2	Unused	R/O	cent di
1	Change in APS Unstable State Interrupt Enable	R/W	Change of APS (K1, K2 Byte) Instability Condition - Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change of APS (K1, K2 Byte) Instability condition" interrupt. If the user enables this interrupt, then the Receive STS-1 TOH Processor block will generate an Interrupt in response to either of the following events. a. If the Receive STS-1 TOH Processor block declares a "K1, K2 Instability" condition. b. If the Receive STS-1 TOH Processor block clears the "K1, K2

New K1, K2 Byte Value Interrupt Enable:

Instability" condition.

This READ/WRITE bit-field permits the user to either enable or disable the "New K1, K2 Byte Value" Interrupt. If the user enables this interrupt, then the Receive STS-1 TOH Processor block will generate this interrupt anytime it receives and accepts a new K1, K2 byte value. The Receive STS-1 TOH Processor block will accept a new K1, K2 byte value, after it has received it within 3 (or 5) consecutive STS-1 frames.

- 0 Disables the "New K1, K2 Byte Value" Interrupt.
- 1 Enables the "New K1, K2 Byte Value" Interrupt.



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 307: Receive STS-1Transport Interrupt Status Register – Byte 0 (Address Location= 0xN10F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Change of SF Condition Interrupt Enable	Change of SD Condition Interrupt Enable	Detection of REI-L Error Interrupt Enable	Detection of B2 Error Interrupt Enable	Detection of B1 Error Interrupt Enable	Change of LOF Condition Interrupt Enable	Change of SEF Condition Interrupt Enable	Change of LOS Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7	Change of SF	R/W	Change of Signal Failure (SF) Condition Interrupt Enable:
	Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of Signal Failure (SF) Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 device will generate an interrupt anytime the Receive STS-1 TOH Processor block detects an SF condition.
			0 - Disables the "Change of SF Condition Interrupt".
			1 – Enables the "Change of SF Condition Interrupt".
6	Change of SD	R/W	Change of Signal Degrade (SD) Condition Interrupt Enable:
	Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of Signal Degrade (SD) Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 device will generate an interrupt anytime the Receive STS-17OH Processor block detects an SD condition.
			0 – Disables the "Change of SD Condition Interrupt".
			1 – Enables the "Change of SD Condition Interrupt".
5	Detection of	R/W	Detection of Line – Remote Error Indicator Interrupt Enable:
	REI-L Interrupt Enable		This READWRITE bit-field permits the user to either enable or disable the "Detection of Line – Remote Error Indicator" interrupt. If the user enables this interrupt, then the XRT94L33 device will generate an interrupt anytime the Receive STS-1 TOH Processor block detects an REI-L condition.
		6. 3	0 Disables the "Line - Remote Error Indicator" Interrupt.
	11/1		Enables the "Line – Remote Error Indicator" Interrupt.
4	Detection of B2	R/W	Detection of B2 Error Interrupt Enable:
	Error Interrupt Enable	&	This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B2 Error" Interrupt. If the user enables this interrupt, then the XRT94L33 device will generate an interrupt anytime the Receive STS-1 TOH Processor block detects a B2 error.
			0 – Disables the "Detection of B2 Error Interrupt".
			1 – Enables the "Detection of B2 Error Interrupt".
3	Detection of B1	R/W	Detection of B1 Error Interrupt Enable:
	Error Interrupt Enable	•	This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B1 Error" Interrupt. If the user enables this interrupt, then the XRT94L33 device will generate an interrupt anytime the Receive STS-1 TOH Processor block detects a B1 error.
			0 – Disables the "Detection of B1 Error Interrupt".
			1 – Enables the "Detection of B1 Error Interrupt".

S

		3-CHANNEL	DS3/E3/STS-1	TO STS-3/STM-	1 MAPPER – A	ATM REGISTERS
--	--	-----------	--------------	---------------	--------------	---------------

2	Change of LOF Condition	R/W	Change of Loss of Frame (LOF) Condition Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of LOF Condition" interrupt. If the user enables this interrupt, then the XRT94L33 device will generate an interrupt in response to either of the following conditions.
			When the Receive STS-1 TOH Processor block declares the "LOF" condition.
			When the Receive STS-1 TOH Processor block clears the "LOF" condition.
			0 – Disables the "Change of LOF Condition Interrupt.
			1 – Enables the "Change of LOF Condition" Interrupt.
1	Change of SEF	R/W	Change of SEF Condition Interrupt Enable:
	Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of SEF Condition" Interrupt: If the user enables this interrupt, then the XRT94L33 device will generate an interrupt in response to either of the following conditions.
			When the Receive STS-1 TOH Processor block declares the "SEF" condition.
			When the Receive STS-1 TOH Processor block clears the "SEF" condition.
			0 – Disables the "Change of SEF Condition Interrupt".
			1 - Enables the "Change of SEF Condition Interrupt".
0	Change of LOS	R/W	Change of Loss of Signal (LOS) Condition Interrupt Enable:
	Condition Interrupt Enable		This READWRITE bit-field permits the user to either enable or disable the "Change of LOF Condition" interrupt. If the user enables this interrupt, then the XRT94L33 device will generate an interrupt in response to either of the following conditions.
		,ct	• When the Receive STS-1 TOH Processor block declares the "LOF" condition.
	_ - -(-	oduce	• When the Receive STS-1 TOH Processor block clears the "LOF" condition.
	6	5 0	0 – Disables the "Change of LOF Condition Interrupt.
	Theor	3 400	1 – Enables the "Change of LOF Condition" Interrupt.

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 308: Receive STS-1 Transport – B1 Error Count Register – Byte 3 (Address Location= 0xN110)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
B1_Error_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B1_Error_Count[31:24]	RUR	B1 Error Count – MSB:
			This RESET-upon-READ register, along with "Receive Transport – B1 Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a B1 byte error. Note: 1. If the B1 Error Type is configured to be "bit errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of bits, within the B1 value that are in error 2. If the B1 Error Type is configured to be "frame errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B1 bytes.

Table 309: Receive STS-1 Transport – B1 Error Count Register – Byte 2 (Address Location= 0xN111)

Віт 7	Віт 6	Віт 5	Bit 4 Bit 3	Віт 2	Віт 1	Віт 0
B1_Error_Count[23:16]						
RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0,00,00	0	0	0

BIT NUMBER	NAME TYPE	DESCRIPTION
7 - 0	B1_Error_Count[23:16] RUR	B1 Error Count (Bits 23 through 16):
	The base may	This RESET-upon-READ register, along with "Receive Transport – B1 Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a B1 byte error.
	'	Note:
		1. If the B1 Error Type is configured to be "bit errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of bits, within the B1 value that are in error.
		2. If the B1 Error Type is configured to be "frame errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B1 bytes.

Table 310: Receive STS-1 Transport – B1 Error Count Register – Byte 1 (Address Location= 0xN112)

Bit 7 Bit 6 Bit 5 Bit 4 Bit 3 Bit 2 Bit 1 Bit 6



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

B1_Error_Count[15:8]								
RUR RUR RUR RUR RUR RUR RUR								
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	B1_Error_Count[15:8]	RUR	B1 Error Count – (Bits 15 through 8)
			This RESET-upon-READ register, along with "Receive Transport – B1 Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a B1 byte error.
			Note:
			1. If the B1 Error Type is configured to be "bit errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of bits, within the B1 value that are in error
			2. If the B1 Error Type is configured to be "frame errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B1 bytes.

Table 311: Receive STS-1 Transport – B1 Error Count Register – Byte 0 (Address Location= 0xN113)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
			B1_Error_	Count[7:0]						
RUR	RUR	RUR	RUR (RUR	RUR	RUR	RUR			
0	0	0	00 60	0	0	0	0			
	Pic 10 delle									

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B1_Error_Count[7:0]	RUR	B1 Error Count – LSB:
	Producet a	not	This RESET-upon-READ register, along with "Receive Transport – B1 Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a B1 byte error.
	The to We		Note:
	y gand		1. If the B1 Error Type is configured to be "bit errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of bits, within the B1 value that are in error.
			2. If the B1 Error Type is configured to be "frame errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B1 bytes.



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 312: Receive STS-1 Transport – B2 Error Count Register – Byte 3 (Address Location= 0xN114)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
B2_Error_Count[31:24]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	B2_Error_Count[31:24]	RUR	B2 Error Count – MSB:
			This RESET-upon-READ register, along with "Receive STS-1 Transport – B2 Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a B2 byte error. Note: 1. If the B2 Error Type is configured to be "bit errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of bits, within the B2 value that are in error. 2. If the B2 Error Type is configured to be "frame errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B2 bytes.

Table 313: Receive STS-1 Transport – B2 Error Count Register – Byte 2 (Address Location= 0xN115)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 2	Віт 1	Віт 0
			B2_Error_Count[23:16]			
RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0 00	0	0	0

BIT NUMBER	NAME J	YPE	DESCRIPTION
7 - 0	B2_Error_Count[23:16]	RUR	B2 Error Count (Bits 23 through 16):
	The data of the		This RESET-upon-READ register, along with "Receive Transport – B2 Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a B2 byte error.
	'0 '		Note:
			1. If the B2 Error Type is configured to be "bit errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of bits, within the B2 value that are in error.
			2. If the B2 Error Type is configured to be "frame errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B2 bytes.

Table 314: Receive STS-1 Transport – B2 Error Count Register – Byte 1 (Address Location= 0xN116)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
B2_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	B2_Error_Count[15:8]	RUR	B2 Error Count – (Bits 15 through 8)
			This RESET-upon-READ register, along with "Receive Transport – B2 Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a B2 byte error. *Note:* 1. If the B2 Error Type is configured to be "bit errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of bits, within the B2 value that are in error. 2. If the B2 Error Type is configured to be "frame errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B2 bytes.

Table 315: Receive STS-1 Transport – B2 Error Count Register – Byte 0 (Address Location= 0xN117)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0
	1	1	B2_Error_(06unt[7:0]			
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0 (0	000	0	0	0	0

BIT NUMBER	Name	TXPE	DESCRIPTION	
7 - 0	B2_Error_Count[7:0]	RUR	B2 Error Count – LSB:	
	The Hatas	May	This RESET-upon-READ register, along with "Receive Transport – B2 Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a B2 byte error.	
	'0 '		Note:	
			1. If the B2 Error Type is configured to be "bit errors", then the ReceistSTS-1 TOH Processor block will increment this 32 bit counter by the number of bits, within the B2 value that are in error.	
			2. If the B2 Error Type is configured to be "frame errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B2 bytes.	

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 316: Receive STS-1 Transport - REI-L Error Count Register - Byte 3 (Address Location = 0xN118)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
REI_L_Error_Count[31:24]										
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR			
0	0	0	0	0	0	0	0			

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	REI_L_Error_Count[31:24]	RUR	REI-L Error Count – MSB:
			This RESET-upon-READ register, along with "Receive Transport – REI-L Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a Line - Remote Error Indicator.
			Note: 1. If the REI-L Error Type is configured to be "bit errors", then the Receive STS-1 TOP Processor block will increment this 32 bit
			counter by the nibble-value within the REI-L field of the M0 byte.
			2. If the REI-L Error Type is configured to be "frame errors", then the Receive STS-1 TOH Processor block will increment this 32 bit
			counter by the number of frames that contain non-zero REI-L values.

Table 317: Receive STS-1 Transport – REI L Error Count Register – Byte 2 (Address Location= 0xN119)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
REI_L_Erro Count[23:16]											
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR				
0	0	0 %	0	0	0	0	0				
	ato hee the										

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	REI_L_Error_Count[23:16]	RUR	REI-L Error Count (Bits 23 through 16):
	o and		This RESET-upon-READ register, along with "Receive Transport – REI-L Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a Line – Remote Error Indicator.
			Note:
			1. If the REI-L Error Type is configured to be "bit errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the nibble-value within the REI-L field of the M0 byte.
			2. If the REI-L Error Type is configured to be "frame errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of frames that contain non-zero REI-L values.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 318: Receive STS-1 Transport - REI_L Error Count Register - Byte 1 (Address Location= 0xN11A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
REI_L_Error_Count[15:8]										
RUR	RUR RUR RUR RUR RUR RUR RUF									
0	0	0	0	0	0	0	0			

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	REI_L_Error_Count[15:8]	RUR	REI-L Error Count – (Bits 15 through 8)
			This RESET-upon-READ register, along with "Receive Transport – REI-L Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a Line – Remote Error Indicator.
			Note:
			1. If the REI-L Error Type is configured to be "bit errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the nibble-value within the REI-L field of the M0 byte.
			2. If the REI-L Error Type is configured to be "frame errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of frames that contain non-zero REI-L values.
			values.

Table 319: Receive STS-1 Transport – REI_L Error Count Register – Byte 0 (Address Location= 0xN11B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		10	1				
			REI_LUTIIC	or_Count[7:0]			
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0
		No hee	N				

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	REI_L_Error_Count[7:0]	RUR	REI-L Error Count – LSB:
	dano		This RESET-upon-READ register, along with "Receive Transport – REI-L Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a Line – Remote Error Indicator.
			Note:
			1. If the REI-L Error Type is configured to be "bit errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the nibble-value within the REI-L field of the M0 byte.
			2. If the REI-L Error Type is configured to be "frame errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of frames that contain non-zero REI-L values.

EXAR Experience Our Connectivi

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 320: Receive STS-1 Transport – Received K1 Byte Value (Address Location= 0xN11F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
Filtered_K1_Value[7:0]										
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O			
0	0	0	0	0	0	0	0			

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Filtered_K1_Value[7:0]	R/O	Filtered/Accepted K1 Value:
			These READ-ONLY bit-fields contain the value of the most recently "filtered" K1 value, that the Receive STS-1 TOH Processor block has received. These bit-fields are valid if the K1/K2 pair (to which it belongs) has been received for 3 consecutive STS-1 frames. This register should be polled by software in order to determine various APS codes.

Table 321: Receive STS-1Transport – Received K2 Byte Value (Address Location= 0xN123)

Віт 7	Віт 6	Віт 5	Віт 4	Bit 3	Віт 2	Віт 1	Віт 0
			Filtered_K2	_Value[7:0]			
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0		0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7-0	Filtered_K2_Value[7:0]	R/O CO	Filtered/Accepted K2 Value: These READ-ONLY bit-fields contain the value of the most recently filtered. K2 value, that the Receive STS-1 TOH Processor block has received. These bit-fields are valid if the K1/K2 pair (to which it belongs) has been received for 3 consecutive STS-1 frames. This register should be polled by Software in order to determine various APS codes.

Table 322: Receive STS-1 Transport - Received S1 Byte Value (Address Location= 0xN127)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	Filtered_S1_Value[7:0]									
R/O R/O R/O R/O R/O R/O R							R/O			
0	0	0	0	0	0	0	0			

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Filtered_S1_Value[7:0]	R/O	Filtered/Accepted S1 Value:
			These READ-ONLY bit-fields contain the value of the most recently "filtered" S1 value that the Receive STS-1 TOH Processor block has received. These bit-fields are valid if it has been received for 8 consecutive STS-1 frames.

Table 323: Receive STS-1 Transport – LOS Threshold Value MSB (Address Location= 0xN12E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	LOS_THRESHOLD[15:8]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
1	1	1	1 🔇	1	1	1	1			

BIT NUMBER	Name	TYPE	DESCRIPTION
7 - 0	LOS_THRESHOLD[15:8]	R/W	LOS Threshold Value – MSB:
	adjust of product of are	100 of	These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – LOS Threshold Value – LSB" register specify the number of consecutive (All Zero) bytes that the Receive STS-1 TOH Processor block must detect before it can declare an LOS condition.
	The proshed in		

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER – ATM REGISTERS



Rev 2.0.0

Table 324: Receive STS-1 Transport – LOS Threshold Value - LSB (Address Location= 0xN12F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
LOS_THRESHOLD[7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	LOS_THRESHOLD[7:0]	R/W	LOS Threshold Value – LSB:
			These READ/WRITE bits, along the contents of the "Receive STS-1Transport – LOS Threshold Value – MSB" register specify the number of consecutive (All Zero) bytes that the Receive STS-1 TOH Processor block must detect before it can declare an LOS condition.

Table 325: Receive STS-1 Transport – Receive SF SET Monitor Interval – Byte 2 (Address Location= 0xN131)

					- 1/ V				
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
SF_SET_MONITOR_WINDOW[23:16]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	5/000	1	1	1		

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_SET_MONITOR_WINDOW[23:1	R/W	SF_SET_MONITOR_INTERVAL - MSB:
	The product of and may not and and may not	pe of	These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF SET Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the number of STS-1 Frame periods that will constitute a SET Sub-Interval for SF (Signal Failure). When the Receive STS-1 TOH Processor block is checking for SF, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors exceeds that of programmed into the "Receive Transport SF SET Threshold" register, then an SF condition will be declared.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 326: Receive STS-1 Transport – Receive SF SET Monitor Interval – Byte 1 (Address Location= 0xN132)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	SF_SET_MONITOR_WINDOW[15:8]									
R/W R/W R/W R/W R/W R/W R/W										
1	1	1	1	1	1	1	1			

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SF_SET_MONITOR_WINDOW[15:8]	R/W	SF_SET_MONITOR_INTERVAL (Bits 15 through 8):
		net	These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF SET Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the number of STS-1 Frame periods that will constitute a SET Sub-Interval for SF (Signal Failure). When the Receive STS-1 TOH Processor block is checking for SF, it will accumulate B2 bit errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 bit errors exceeds that of programmed into the "Receive STS-1 Transport SF SET Threshold" register, then an SF condition will be declared.

Table 327: Receive STS-1 Transport – Receive SF SET Monitor Interval – Byte 0 (Address Location= 0xN133)

Віт 7	Віт 6	Віт 5	Віт4	Віт 3	Віт 2	Віт 1	Віт 0			
	SF_SET_MONITOR_WINDOW[7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
1	1	10	1100	1	1	1	1			

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SF_SET_MONITOR_WINDOW[7:0	R/W	SF_SET_MONITOR_INTERVAL - LSB:
	11. 93grid II.		These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF SET Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the number of STS-1 Frame periods that will constitute a SET Sub-Interval for SF (Signal Failure).
			When the Receive STS-1 TOH Processor block is checking for SF, it will accumulate B2 bit errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 bit errors exceeds that of programmed into the "Receive STS-1 Transport SF SET Threshold" register, then an SF condition will be declared.

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 328: Receive STS-1 Transport - Receive SF SET Threshold - Byte 1 (Address Location= 0xN136)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
SF_SET_THRESHOLD[15:8]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SF_SET_THRESHOLD[15:8]	R/W	SF_SET_THRESHOLD - MSB:
			These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF SET Threshold – Byte 0" registers permit the user to specify the number of B2 bit errors that will cause the Receive STS-1 TOH Processor block to declare an SF (Signal Failure) condition. When the Receive STS-1 TOH Processor block is checking for SF, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors exceeds that of programmed into this and the "Receive STS-1 Transport SF SET Threshold – Byte 0" register, then an SF condition will be declared.

Table 329: Receive STS-1 Transport - Receive SF SET Threshold - Byte 0 (Address Location= 0xN137)

Віт 7	Віт 6	Віт 5	BIT 40 BIT 3	Віт 2	Віт 1	Віт 0		
SF_SET_THRESHOLD[7:0]								
R/W	R/W	R/W	R/W R/W	R/W	R/W	R/W		
1	1	1	1 1	1	1	1		

BIT NUMBER	NAME TYPE	DESCRIPTION
7 - 0	SF_SET_THRESHOLD[7:0] R/W	SF_SET_THRESHOLD - LSB:
	The data din has	These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF SET Threshold – Byte 1" registers permit the user to specify the number of B2 bit errors that will cause the Receive STS-1 TOH Processor block to declare an SF (Signal Failure) condition.
		When the Receive STS-1 TOH Processor block is checking for SF, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors exceeds that of programmed into this and the "Receive STS-1 Transport SF SET Threshold – Byte 1" register, then an SF condition will be declared.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 330: Receive STS-1 Transport – Receive SF CLEAR Threshold – Byte 1 (Address Location= 0xN13A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
SF_CLEAR_THRESHOLD[15:8]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SF_CLEAR_THRESHOLD	R/W	SF_CLEAR_THRESHOLD - MSB:
	[15:8]		These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF CLEAR Threshold – Byte 0" registers permit the user to specify the upper limit for the number of B2 bit errors that will cause the Receive STS-1 TOH Processor block to clear the SF (Signal Failure) condition. When the Receive STS-1 TOH Processor block is checking for clearing SF, it will accumulate B2 errors for a total of 8 CLEAR Sub-Interval periods. If the number of accumulated B2 errors is less than that programmed into this and the "Receive STS-1 Transport SF CLEAR Threshold – Byte 0" register, then an SF condition will be cleared.

Table 331: Receive STS-1 Transport - Receive SF CLEAR Threshold - Byte 0 (Address Location= 0xN13B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
SF_CLEAR_THRESHOLD[7:0]										
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
1	1	1 1	,0 b,	1	1	1	1			
	Auc al De									

BIT NUMBER	NAME	ТҮРЕ	DESCRIPTION
7 - 0	SF_CLEAR_THRESHOLD	R/W	SF_CLEAR_THRESHOLD - LSB:
	They of the		These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF CLEAR Threshold – Byte 1" registers permit the user to specify the upper limit for the number of B2 bit errors that will cause the Receive STS-1 TOH Processor block to clear the SF (Signal Failure) condition.
			When the Receive STS-1 TOH Processor block is checking for clearing SF, it will accumulate B2 errors for a total of 8 CLEAR Sub-Interval periods. If the number of accumulated B2 errors is less than that programmed into this and the "Receive STS-1 Transport SF CLEAR Threshold – Byte 1" register, then an SF condition will be cleared.

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 332: Receive STS-1 Transport – Receive SD Set Monitor Interval – Byte 2 (Address Location= 0xN13D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
SD_SET_MONITOR_WINDOW[23:16]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW	R/W	SF_SET_MONITOR_INTERVAL - MSB:
	[23:16]		These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF SET Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the number of STS-1 Frame periods that will constitute a SET Sub-Interval for SD (Signal Degrade) declaration. When the Receive STS-1 TOH Processor block is checking for SD, it will accumulate B2 bit errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 bit errors exceeds that of programmed into the "Receive STS-1 Transport SD SET Threshold" register, then an SD condition will be declared.

Table 333: Receive STS-1 Transport – Receive SD Set Monitor Interval – Byte 1 (Address Location= 0xN13E)

Віт 7	Віт 6	Віт 5	Віт4	Віт 3	Віт 2	Віт 1	Віт 0		
SD_SET_MONITOR_WINDOW[15:8]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0 0	0	0	0	0		
	All and the								

BIT NUMBER	NAME O	YPE	DESCRIPTION
7-0	SD_SET_MONITOR WINDOW R	R/W	SD_SET_MONITOR_INTERVAL – Bits 15 through 8:
	[15/8] data dino		These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SD SET Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the number of STS-1 Frame periods that will constitute a SET Sub-Interval for SD (Signal Degrade) declaration.
			When the Receive STS-1 TOH Processor block is checking for SD, it will accumulate B2 bit errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 bit errors exceeds that of programmed into the "Receive STS-1 Transport SD SET Threshold" register, then an SD condition will be declared.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 334: Receive STS-1 Transport – Receive SD Set Monitor Interval – Byte 0 (Address Location= 0xN13F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SD_SET_MONITOR_WINDOW[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW	R/W	SD_SET_MONITOR_INTERVAL - LSB:
	[7:0]		These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SD SET Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the number of STS-1 Frame periods that will constitute a SET Sub-Interval for SD (Signal Degrade) declaration. When the Receive STS-1 TOH Processor block is checking for SD, it will accumulate B2 bit errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 bit errors exceeds that of programmed into the "Receive STS-1 Transport SD SET Threshold" register, then an SD condition will be declared.

Table 335: Receive STS-1 Transport - Receive SD SET Threshold - Byte 1 (Address Location= 0xN142)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
			SD_SET_THR	SHOLD[15:8]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	.O b.	1	1	1	1	
	All of all the							

BIT NUMBER	NAME	Түре	DESCRIPTION		
7 - 0	SD_SET_THRESHOLD[15:8] R/W		SD_SET_THRESHOLD – MSB: These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SD SET Threshold – Byte 0" registers permit the user to specify the number of B2 bit errors that will cause the Receive STS-1 TOH Processor block to declare an SD (Signal Degrade) condition.		
			When the Receive STS-1 TOH Processor block is checking for SD, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors exceeds that of programmed into this and the "Receive STS-1 Transport SD SET Threshold – Byte 0" register, then an SD condition will be declared.		

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 336: Receive STS-1 Transport - Receive SD SET Threshold - Byte 0 (Address Location= 0xN143)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SD_SET_THRESHOLD[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SD_SET_THRESHOLD[7:0]	R/W	SD_SET_THRESHOLD - LSB:
			These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SD SET Threshold – Byte 1" registers permit the user to specify the number of B2 bit errors that will cause the Receive STS-1 TOH Processor block to declare an SD (Signal Degrade) condition. When the Receive STS-1 TOH Processor block is checking for SD, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors exceeds that of programmed into this and the "Receive STS-1 Transport SD SET Threshold – Byte 1" register, then an SD condition will be declared.

Table 337: Receive STS-1 Transport – Receive SD CLEAR Threshold – Byte 1 (Address Location= 0xN146)

Віт 7	Віт 6	Віт 5	Віт4	Віт 3	Віт 2	Віт 1	Віт 0	
	SD_CLEAR_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	0 0	1	1	1	1	
	Allog at the							

BIT NUMBER	NAME TYPE	DESCRIPTION
7 - 0	SD_CLEAR_THRESHOLD R/W	SD_CLEAR_THRESHOLD - MSB: These READ/WRITE bits, along the contents of the "Receive STS-1 Transport - SD CLEAR Threshold - Byte 0" registers permit the user to specify the upper limit for the number of B2 bit errors that will cause the Receive STS-1 TOH Processor block to clear the SD (Signal Degrade) condition. When the Receive STS-1 TOH Processor block is checking for clearing SD, it will accumulate B2 errors for a total of 8 CLEAR Sub-Interval periods. If the number of accumulated B2 errors is less than that programmed into this and the "Receive STS-1"
		less than that programmed into this and the "Receive STS-1 Transport SD CLEAR Threshold – Byte 0" register, then an SD condition will be cleared.

Table 338: Receive STS-1 Transport – Receive SD CLEAR Threshold – Byte 1 (Address Location= 0xN147)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SD_CLEAR_THRESHOLD[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SD_CLEAR_THRESHOLD[7:0]	R/W	SD_CLEAR_THRESHOLD - LSB:
			These READ/WRITE bits, along the contents of the "Receive STS-1 Transport - SD CLEAR Threshold - Byte 1" registers permit the user to specify the upper limit for the number of B2 bit errors that will cause the Receive STS-1 TOH Processor block to clear the SD (Signal Degrade) condition. When the Receive STS-1 TOH Processor block is checking for clearing SD, it will accumulate B2 errors for a total of 8 CLEAR Sub-Interval periods. If the number of accumulated B2 errors is less than that programmed into this and the "Receive STS-1 Transport SD CLEAR Threshold - Byte 1" register then an SD condition will be cleared.

Table 339: Receive STS-1 Transport – Force SEF Condition Register (Address Location= 0xN14B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			Unused	10			SEF FORCE
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0 0	0	0	0	0
	All of all the						

BIT NUMBER	Name 👍	TYPE	DESCRIPTION
7 – 1	Unused	<i>R</i> /O	
0	SEF FORCE	R/W	SEF Force:
	, 90	and	This READ/WRITE bit-field permits the user to force the Receive STS-1 TOH Processor block (within Channel N) to declare an SEF defect. The Receive STS-1 TOH Processor block will then attempt to reacquire framing.
			Writing a "1" into this bit-field configures the Receive STS-1 TOH Processor block to declare the SEF defect. The Receive STS-1 TOH Processor block will automatically set this bit-field to "0" once it has reacquired framing (e.g., has detected two consecutive STS-1 frames with the correct A1 and A2 bytes).

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 340: Receive STS-1 Transport – Receive J0 Trace Buffer Control Register (Address Location= 0xN14F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		READ SEL	ACCEPT THRD	MSG TYPE	MSG LENGTH	
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION					
7 – 5	Unused	R/O						
4	READ SEL	R/W	J0 Buffer Read Selection:					
			This READ/WRITE bit-field permits a user to specify which of the following buffer segments to read.					
			a. Valid Message Buffer					
			b. Expected Message Buffer					
			0 - Executing a READ to the Receive J0 Trace Buffer, will return contents within the "Valid Message" buffer.					
			1 – Executing a READ to the Receive J0 Trace Buffer, will return contents within the "Expected Message Buffer".					
			Note: In the case of the Receive STS-3 TOH Processor block, the "Receive J0 Trace Buffer" is located at Address Location 0xN300 through 0xN33F.					
3	ACCEPT THRD	R/W	Message Accept Threshold:					
			This READ/WRITE bit-field permits a user to select the number of consecutive times that the Receive STS-1 TOH Processor block must receive a given J0 Trace Message, before it is accepted, as described below.					
		8	0 – The Receive STS-1 TOH Processor block accepts the J0 Message after it has received it the third time in succession.					
		Pro.	12 The Receive STS-1 TOH Processor block accepts the J0 Message after it has received in the fifth time in succession.					
2	MSG TYPE	R/W	Message Alignment Type:					
		9so	This READ/WRITE bit-field permits a user to specify have the Receive STS-1 TOH Processor block will locate the boundary of the J0 Trace Message, as indicated below.					
			0 – Message boundary is indicated by "Line Feed".					
			1 – Message boundary is indicated by the presence of a "1" in the MSB of the first byte (within the J0 Trace Message).					
1 - 0	MSG LENGTH	R/W	J0 Message Length:					
			These READ/WRITE bit-fields permit the user to specify the length of the J0 Trace Message, that the Receive STS-1 TOH Processor block will receive. The relationship between the content of these bit-fields and the corresponding J0 Trace Message Length is presented below.					
			MSG LENGTH Resulting J0 Trace Message Length					

00	1 Byte	
01	16 Bytes	
10/11	64 Bytes	

Table 341: Receive STS-1 Transport – Receive SD Burst Error Tolerance – Byte 1 (Address Location= 0xN152)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SD_BURST_TOLERANCE[15:8]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SD_BURST_TOLERANCE [15:8]	Produ	SD_BURST_TOLERANCE - MSB: These READ/WRITE bits, along with the contents of the "Receive STS-1 Transport - SD BURST Tolerance - Byte 0" registers permit the user to specify the maximum number of B2 bit errors that the corresponding Receive STS-1 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-1 frame period), when determining whether or not to declare an SD (Signal Degrade) defect condition. Note: The purpose of this feature is to permit the user to provide some level of B2 error burst filtering, when the Receive STS-1 TOH Processor block is accumulating B2 byte errors in order to declare the SD defect condition. The user can implement this feature in order to configure the Receive STS-1 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SD defect condition.
	The producet and may	, no	



Rev 2.0.0

Table 342: Receive STS-1 Transport – Receive SD Burst Error Tolerance – Byte 0 (Address Location= 0xN153)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SD_BURST_TOLERANCE[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SD_BURST_TOLERANCE[7:0]	R/W	SD_BURST_TOLERANCE - LSB:
			These READ/WRITE bits, along with the contents of the "Receive STS-1 Transport – SD BURST Tolerance – Byte 1" registers permit the user to specify the maximum number of B2 bit errors that the corresponding Receive STS-1 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-1 frame period), when determining whether or not to declare an SD (Signal Degrade) condition. *Note: The purpose of this feature is to permit the user to provide some level of B2 error burst filtering, when the Receive STS-1 TOH Processor block is accumulating B2 byte errors in order to declare the SD defect condition. The user can implement this feature in order to configure the Receive STS-1
	The product of the data and ma	are to	

Table 343: Receive STS-1 Transport – Receive SF Burst Error Tolerance – Byte 1 (Address Location= 0xN156)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SF_BURST_TOLERANCE[15:8]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SF_BURST_TOLERANCE[15:8]	R/W	SF_BURST_TOLERANCE - MSB:
		Aucte	These READ/WRITE bits, along with the contents of the "Receive STS-1 Transport - SF BURST Tolerance – Byte 0" registers permit the user to specify the maximum number of B2 bit errors that the corresponding Receive STS-1 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-1 frame period), when determining whether or not to declare an SF (Signal Failure) condition. *Note: The purpose of this feature is to permit the user to provide some level of B2 error burst filtering, when the Receive STS-1 TOH Processor block is accumulating B2 byte errors in order to declare the SF defect condition. The user can implement this feature in order to configure the Receive STS-1 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SF defect condition.
	The product or product are and may no	no or	geret de la company de la comp

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 344: Receive STS-1 Transport – Receive SF Burst Error Tolerance – Byte 0 (Address Location= 0xN157)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SF_BURST_TOLERANCE[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SF_BURST_TOLERANCE[7:0]	R/W	SF_BURST_TOLERANCE - LSB:
			These READ/WRITE bits, along with the contents of the "Receive STS-1 Transport – SF BURST Tolerance – Byte 1" registers permit the user to specify the maximum number of B2 bit errors that the corresponding Receive STS-1 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-1 frame period), when determining whether or not to declare an SF (Signal Failure) condition. **Note:** The purpose of this feature is to permit the user to provide some level of B2 error burst filtering, when the Receive STS-1 TOH Processor block is accumulating B2 byte errors in order to declare the SF defect condition. The user can implement this feature in order to configure the Receive STS-1 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SF defect condition.

Table 345: Receive STS-1 Transport – Receive SD Clear Monitor Interval – Byte 2 (Address Location= 0xN159)

Віт 7	Віт 6	Віт 5 🙏	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0
		SD_C	LEAR_MONITO	OR_WINDOW[2	23:16]		
R/W	R/W	R/W	Ø R/W	R/W	R/W	R/W	R/W
1	1	01 10	1 1	1	1	1	1

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW [23:16]	R/W	SD_CLEAR_MONITOR_INTERVAL - MSB:
			These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SD Clear Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the number of STS-1 Frame periods that will constitute a CLEAR Sub-Interval for SD (Signal Degrade).
			When the Receive STS-1 TOH Processor block is checking for clearing the SD defect, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors is less than that of programmed into the "Receive STS-1 Transport SD Clear Threshold" register, then the SD defect will be cleared.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 346: Receive STS-1 Transport – Receive SD Clear Monitor Interval – Byte 1 (Address Location= 0xN15A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SD_CLEAR_MONITOR_WINDOW[15:8]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW [15:8]	R/W	SD_CLEAR_MONITOR_INTERVAL - Bits 15 through 8:
		74	These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SD Clear Monitor Interval – Byte 2 and Byte 0" tegisters permit the user to specify the number of STS-1 Frame periods that will constitute a CLEAR Sub-Interval for SD (Signal Degrade). When the Receive STS-1 TOH Processor block is checking for clearing the SD defect, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors is less than that of programmed into the "Receive STS-1 Transport SD Clear Threshold" register, then the SD defect will be cleared.

Table 347: Receive STS-1 Transport – Receive SD Clear Monitor Interval – Byte 0 (Address Location= 0xN15B)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SD_CLEAR_MONITOR_WINDOW[7:0]								
R/W	R/W	R/W	RW	R/W	R/W	R/W	R/W		
1	1	1)	1	1	1	1	1		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW [7:0]	R/W	SD_CLEAR_MONITOR_INTERVAL – LSB: These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SD Clear Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the number of STS-1 Frame periods that will constitute a
			CLEAR Sub-Interval for SD (Signal Degrade). When the Receive STS-1 TOH Processor block is checking for clearing the SD defect, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors is less than that of programmed into the "Receive STS-1 Transport SD Clear Threshold" register, then the SD defect will be cleared.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 348: Receive STS-1 Transport – Receive SF Clear Monitor Interval – Byte 2 (Address Location= 0xN15D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
SF_CLEAR_MONITOR_WINDOW[23:16]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	NAME SF_CLEAR_MONITOR_WINDOW [23:16]	TYPE R/W	SF_CLEAR_MONITOR_INTERVAL – MSB: These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF Clear Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the number of STS-1 Frame periods that will constitute a CLEAR Sub-Interval for SF (Signal Failure). When the Receive STS-1 TOH Processor block is checking for clearing the SF defect, it will accumulate B2 errors for a
			total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors is less than that of programmed into the "Receive STS-1 Transport SF Clear Threshold"
			register, then the SF defect will be cleared.

Table 349: Receive STS-1 Transport – Receive SF Clear Monitor Interval – Byte 1 (Address Location= 0xN15E)

Віт 7	Віт 6	Віт 5	Віт4	Віт 3	Віт 2	Віт 1	Віт 0		
SF_CLEAR_MONITOR_WINDOW[15:8]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	0 0	1	1	1	1		
	MC, of D								

	0 0	7	
BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDOW [15:8]	R/W	SF_CLEAR_MONITOR_INTERVAL - Bits 15 through 8: These READ/WRITE bits, along the contents of the "Receive STS-1 Transport - SF Clear Monitor Interval - Byte 2 and Byte 0" registers permit the user to specify the number of STS-1 Frame periods that will constitute a CLEAR Sub-Interval for SF (Signal Failure). When the Receive STS-1 TOH Processor block is checking for clearing the SF defect, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors is less than that of programmed into the "Receive STS-1 Transport SF Clear Threshold" register, then the SF defect will be cleared.

Table 350: Receive STS-1 Transport – Receive SF Clear Monitor Interval – Byte 0 (Address Location= 0xN15F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SF_CLEAR_MONITOR_WINDOW[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDOW	R/W	SF_CLEAR_MONITOR_INTERVAL - LSB:
	[7:0]		These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF Clear Monitor Interval – Byte 2 and Byte 1 registers permit the user to specify the number of STS-1 Frame periods that will constitute a CLEAR Sub-Interval for SF (Signal Failure).
			When the Receive STS-1 TOH Processor block is checking for clearing the SF defect, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors is less than that of programmed into the "Receive STS-1 Transport SF Clear Threshold" register, then the SF defect will be cleared.
	The product or product are to the data and may not to	loude olde	Led OFS Led OF

xperience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 351: Receive STS-1 Transport – Auto AIS Control Register (Address Location= 0xN163)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit AIS-P (Down- stream) upon J0 Message Unstable	Transmit AIS-P (Down- stream) Upon Section Trace Message Mismatch	Transmit AIS-P (Down- stream) upon SF	Transmit AIS-P (Down- stream) upon SD	Unused	Transmit AIS-P (Down- stream) upon LOF	Transmit AIS-P (Down- stream) upon LOS	Transmit AIS-P (Down- stream) Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

RIT NUMBER	NAME	Тург	DESCRIPTION
7	NAME Transmit AIS-P (Downstream) upon J0 Message Unstable	TYPE R/W	Transmit Path AlS upon Detection of Unstable Section Trace (J0): This READ/WRITE bit-field permits the user to configure the Receive STS-1 TOH Processor block to automatically transmit a Path AlS (AlS-P) Indicator via the "downstream" traffic (e.g., towards the Receive STS-1 POH Processor blocks), anytime it detects an Unstable Section Trace (J0) condition in the "incoming" STS-1 data-stream.
			0 – Does not configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects an "Unstable Section Trace" condition.
		্ব	1 Configures the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects an "Unstable Section Trace" condition.
	٥	ucite	Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
6	Transmit AIS-P (Down- stream) Upon J0	R/W	Transmit Path AIS (AIS-P) upon Detection of Section Trace (J0) Mismatch:
	Message Mismatch	dn	This READ/WRITE bit-field permits the user to configure the Receive STS-1 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive STS-1 POH Processor blocks), anytime it detects a Section Trace (J0) Mismatch condition in the "incoming" STS-1 data stream.
			0 – Does not configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects a "Section Trace Mismatch" condition.
			1 – Configures the Receive STS-1 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects a "Section Trace Mismatch" condition.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
5	Transmit AIS-P (Down-	R/W	Transmit Path AIS upon Signal Failure (SF):
	stream) upon SF		This READ/WRITE bit-field permits the user to configure the Receive

			STS-1 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive STS-1 POH Processor block), anytime it declares an SF condition.
			0-Does not configure the Receive STS-1 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the SF defect.
			1-Configures the Receive STS-1 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the SF detect.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
4	Transmit AIS-P (Down-	R/W	Transmit Path AIS upon Signal Degrade (SD):
	stream) upon SD		This READ/WRITE bit-field permits the user to configure the Receive STS-1 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive STS-1 POH Processor block) anytime it declares an SD condition.
			0 – Does not configure the Receive STS-1 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the SD defect.
			1 – Configures the Receive STS-1 TOH Processor block to transmit the AIS P indicator (via the "downstream" traffic) upon declaration of the SD defect.
		, pr	Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
3	Unused	R/O	, 0,
2	Transmit AIS-P (Down	R/W	Transmit Path AIS upon Loss of Frame (LOF):
	stream) upon LOF	at no	This READ/WRITE bit-field permits the user to configure the Receive STS-1 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive STS-1 POH Processor block), anytime it declares an LOF condition.
	, ga sug		0-Does not configure the Receive STS-1 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the LOF defect.
			1 – Configures the Receive STS-1 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the LOF defect.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
1	Transmit AIS-P (Down-	R/W	Transmit Path AIS upon Loss of Signal (LOS):
	stream) upon LOS		This READ/WRITE bit-field permits the user to configure the Receive STS-1 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive STS-1 POH Processor block), anytime it declares an LOS condition.

EXAR Experience Our Connectivit

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			0 – Does not configure the Receive STS-1 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) anytime it declares the LOS defect.
			1 – Configures the Receive STS-1 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) anytime it declares the LOS defect.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
0	AUTO AIS	R/W	Automatic Transmission of AIS-P Enable:
			This READ/WRITE bit-field serves two purposes.
			It permits the user to configure the Receive STS-1 TOH Processor block to automatically transmit the Path AIS (AIS-P) indicator, via the down-stream traffic (e.g., towards the Receive STS-1 POH Processor block), upon detection of an SF, SD, Section Trace Mismatch, Section Trace Unstability, LOF or LOS conditions.
			It also permits the user to configure the Receive STS-1 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive STS-1 POH Processor block) anytime it detects an AIS-L condition in the "incoming" STS-1 datastream.
			0 - Configures the Receive STS-1 TOH Processor block to NOT automatically transmit the AIS-P indicator (via the "downstream" traffic) upon detection of the AIS-L or any of the "above-mentioned" conditions.
		4	1 - Configures the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) upon detection of the AIS-L or any of the "above-mentioned" condition.
	6	ner lo	Note: The user must also set the corresponding bit-fields (within this register) to "1" in order to configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator upon detection of a given a
	Theprod	id may	

Table 352: Receive STS-1 Transport – Auto AIS (in Downstream STS-1s) Control Register (Address Location= 0xN16B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unu	Unused		Transmit AIS-P (via Downstream STS-1s) upon LOF	Transmit AIS-P (via Downstream STS-1s) upon SD	Transmit AIS-P (via Downstream STS-1s) upon SF	Unused	Transmit AIS-P (via Downstream STS-1s) Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 6	Unused	R/O	"His reo
5	Transmit AIS-P (via Downstream STS-1s) upon LOS	R/W	Transmit AIS-P (via Downstream STS-1s) upon LOS (Loss of Signal): This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (in the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares the LOS defect. O — Does not configure the corresponding Transmit SONET POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares the LOS defect. Configure the corresponding Transmit SONETPOH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares the LOS defect.
	The production of the data and	nay nay	Note: In the "long-run" the function of this bit-field is exactly the same as that of Bit 1 (Transmit AIS-P Down-stream – Upon LOS), within the Receive STS-1 Transport – Auto AIS Control Register (Address Location= 0xN163). The only difference is that this register bit will cause the corresponding "downstream" Transmit SONET POH Processor block to IMMEDIATELY begin to transmit the AIS-P condition whenever the Receive STS-1 TOH Processor block declares the LOS defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the NE declaring the LOS defect.
			In the case of Bit 1 (Transmit AIS-P Downstream – Upon LOS), several SONET frame periods are required (after the Receive STS-1 TOH Processor block has declared the LOS defect), before the corresponding Transmit SONET POH Processor block will begin the process of transmitting the AIS-P indicator.
			2. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STS-1s Enable) within this register, in order enable this feature.
4	Transmit AIS-P (via Downstream STS-1s)	R/W	Transmit AIS-P (via Downstream STS-1s) upon LOF (Loss of Frame):
	upon LOF		This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (in the corresponding channel) to

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares the LOF defect.
			0 - Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares the LOF defect.
			1 — Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares the LOF defect.
			Note:
			1. In the "long-run" the function of this bit-field is exactly the same as that of Bit 2 (Transmit AIS-P Down stream — Upon LOF), within the Receive STS-1 Transport — Auto AIS Control Register (Address Location= 0xN163). The only difference is that this register bit will cause the corresponding downstream" Transmit SONET POH Processor blocks to IMMEDIATELY begin to transmit the AIS-P condition whenever the Receive STS-1 TOH Processor block declares the LOF defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the NE declaring the LOF defect.
			In the case of Bit 2 (Transmit AIS-P Downstream – Upon LOF), several SONET frame periods are required (after the Receive STS-3 TOH Processor block has declared the LOS defect), before the corresponding Transmit SONET POH Processor block will begin the process of transmitting the AIS-P indicator.
			2. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AlS-P via Downstream STS-1s Enable) within this register, in order enable this feature.
3	Transmit AIS-P (via Downstream STS-1s)	R/W	Transmit AIS-P (via Downstream STS-1s) upon SD (Signal Degrade):
	upon SD	o the o	This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (in the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signals (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares the SD defect.
	1,90	andli	0 - Does not configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares the SD defect.
			1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares the SD defect.
			Note:
			1. In the "long-run" the function of this bit-field is exactly the same as that of Bit 4 (Transmit AIS-P Down-stream – Upon SD), within the Receive STS-1 Transport – Auto AIS Control Register (Address Location= 0xN163). The only difference is that this register bit will cause the corresponding "downstream" Transmit SONET POH Processor blocks to IMMEDIATELY begin to transmit the AIS-P condition whenever the Receive STS-1 TOH Processor block declares

			the SD defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the NE declaring the LOS defect.
			In the case of Bit 1 (Transmit AIS-P Downstream – Upon LOF), several SONET frame periods are required (after the Receive STS-1 TOH Processor block has declared the SD defect), before the corresponding Transmit SONET POH Processor block will begin the process of transmitting the AIS-P indicator.
			2. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STS-1s Enable) within this register, in order enable this feature.
2	Transmit AIS-P (via	R/W	Transmit AIS-P (via Downstream STS-1s) upon Signal Failure (SF):
	Downstream STS-1s) upon SF		This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (in the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares an SF condition.
			0 - Does not configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1TOH Processor block declares the SF defect.
			1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares the SF defect.
	*odu	or of the state of	Note: In the "long-run" the function of this bit-field is exactly the same as that of Bit 5 (Transmit AIS-P Down-stream – Upon SF), within the Receive STS-1 Transport – Auto AIS Control Register (Address Location – 0xN163). The only difference is that this register bit will cause the corresponding "downstream" Transmit SONET POH Processor blocks to IMMEDIATELY begin to transmit the AIS-P condition whenever the Receive STS-1 TOH Processor block declares the SF defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the NE declaring the SF defect.
	The prata	may	In the case of Bit 5 (Transmit AIS-P Downstream – Upon SF), several SONET frame periods are required (after the Receive STS-1 TOH Processor block has declared the SF defect), before the corresponding Transmit SONET POH Processor blocks will begin the process of transmitting the AIS-P indicator.
			2. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STS-1s Enable) within this register, in order enable this feature.
1	Unused	R/O	
0	Transmit AIS-P (via Downstream STS-1s) Enable	R/W	Automatic Transmission of AIS-P (via the downstream STS-1s) Enable:
	Enable		This READ/WRITE bit-field permits the user to configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P indicator, via its "outbound" STS-1 signal (within the outbound STS-3 signal), upon detection of an SF, SD, LOS and LOF condition via the Receive STS-1 TOH Processor block.
			0 – Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P indicator, whenever the Receive STS-1 TOH Processor block declares either the LOS, LOF,

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

SD or th	e SF defects.
block to Receive	offigures the corresponding Transmit SONET POH Processor automatically transmit the AIS-P indicator, whenever the STS-1 TOH Processor block declares either the LOS, LOF, SD = defects.

The product are no longered (OBS)

The product are no longered (OBS)

The product are no longered (OBS)

Table 353: Receive STS-1 Path - Control Register - Byte 2 (Address Location= 0xN183)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unu	sed		Check	RDI-P	REI-P	B3 Error Type
					Type	Error Type	
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3	Check Stuff	R/W	Check (Pointer Adjustment) Stuff Select:
			This READ/WRITE bit-field permits the user to enable/disable the SONET standard recommendation that a pointer increment or decrement operation, detected within 3 SONET frames of a previous pointer adjustment operation (e.g., negative stuff, positive stuff) is ignored.
			0 – Disables this SONET standard implementation. In this mode, all pointer-adjustment operations that are detected will be accepted.
			1 – Enables this "SONET standard" implementation. In this mode, all pointer-adjustment operations that are detected within 3 SONET frame periods of a previous pointer-adjustment operation, will be ignored.
2	RDI-P Type	R/W	Path - Remote Defect Indicator Type Select:
			This READ/WRITE bit-field permits the user to configure the Receive STS-1 POH Processor block to support either the "Single-Bit" or the "Enhanced" RDI-P, as described below.
		, in	0 - Configures the Receive STS-1 POH Processor block to support the Single-Bit RDI-P. In this mode, the Receive STS-1 POH Processor block will only monitor Bit 5, within the G1 byte (of the incoming SPE data), in order to declare and clear the RDI-P indicator.
	ď	oduci	1 Configures the Receive STS-1 POH Processor block to support the Enhanced RDI-P (ERDI-P). In this mode, the Receive STS-1 POH Processor block will monitor bits 5, 6 and 7, within the G1 byte, in order to declare and clear the RDI-P indicator.
1	REI-P Error	R/W	REI-P Error Type:
	Туре	9	This READ/WRITE bit-field permits the user to specify how the "Receive Path REI-P Error Count" register is incremented.
		9 1.	0 – Configures the Receive STS-1 POH Processor block to count REI-P Bit Errors.
			In this case, the "Receive Path REI-P Error Count" register will be incremented by the value of the lower nibble within the G1 byte.
			1 – Configures the Receive STS-1 POH Processor block to count REI-P Frame Errors.
			In this case, the "Receive Path REI-P Error Count" register will be incremented by a single count each time the Receive STS-1 POH Processor block receives a G1 byte, in which bits 1 through 4 are set to a "non-zero" value.
0	B3 Error Type	R/W	B3 Error Type:
			This READ/WRITE bit-field permits the user to specify how the "Receive Path B3 Error Count" register is incremented.

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

0 - Configures the Receive STS-1 POH Processor block to count B3 bit errors. In this case, the "Receive Path B3 Error Count" register will be incremented by the number of bits, within the B3 value, that is in error.
1 – Configures the Receive STS-1 POH Processor block to count B3 frame errors. In this case, the "Receive Path B3 Error Count" register will be incremented by the number of erred STS-1 frames.

The product of products mentioned in this deline of the product are no ordered (OBS)

Table 354: Receive STS-1 Path - Control Register - Byte 1 (Address Location= 0xN186)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused							J1 Unstable Indicator
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

Processor block is currently declaring the Path Trace Un Receive STS-1 POH Processor block will declare a J1 condition, whenever the "J1 Unstable" counter reaches the Unstable counter will be incremented for each time message that differs from the previously received message counter is cleared to "0" whenever the Receive STS-1 PO received a given J1 Message 3 (or 5) consecutive times. Note: Receiving a given J1 Message 3 (or 5) consecutive bit-field to "0".	BIT NUMBER	NAME TYPE	DESCRIPTION
Indicator This READ-ONLY bit-field indicates whether or not the Processor block is currently declaring the Path Trace Ur Receive STS-1 POH Processor block will declare a J1 condition, whenever the "J1 Unstable" counter reaches to Unstable counter will be incremented for each time message that differs from the previously received message counter is cleared to "0" whenever the Receive STS-1 PO received a given J1 Message 3 (or 5) consecutive times. Note: Receiving a given J1 Message 3 (or 5) consecutive bit-field to "0".	7 – 1	Unused R/O	
0 – Path Trace Instability condition is NOT declared. 1 – Path Trace Instability condition is currently declared.	0 J1	1 Unstable R/O Indicator	This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the Path Trace Unstable condition. The Receive STS-1 POH Processor block will declare a J1 (Path Trace) Unstable condition, whenever the "J1 Unstable" counter reaches the value "8". The "J0 Unstable" counter will be incremented for each time that it receives a J1 message that differs from the previously received message. The "J1 Unstable" counter is cleared to "0" whenever the Receive STS-1 POH Processor block has received a given J1 Message 3 (or 5) consecutive times. **Note: Receiving a given J1 Message 3 (or 5) consecutive times also sets this bit-field to "0".



Table 355: Receive STS-1 Path – SONET Receive POH Status – Byte 0 (Address Location= 0xN187)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TIM-P Defect Declared	C2 Byte Unstable Condition	UNEQ-P Defect Declared	PLM-P Defect Declared	RDI-P Defect Declared	RDI-P Unstable Condition	LOP-P Defect Declared	AIS-P Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	TIM-P	R/O	Trace Identification Mismatch (TIM-P) Defect Indicator:
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the "Trace Identification Mismatch" condition.
			The Receive STS-1 POH Processor block will declare the "TIM-P" condition, when none of the received 64 byte string (received via the J1 byte) matches the expected 64 byte message.
			The Receive STS-1 POH Processor block will clear the "TIM-P" condition, when 80% of the received 64 byte string (received via the J1 byte) matches the expected 64 byte message.
			0 - Indicates that the Receive STS-1 POH Processor block is NOT currently declaring the TIM-P condition.
			1 – Indicates that the Receive STS-1 POH Processor block is currently declaring the TIM-P condition.
6	C2 Byte	R/O	C2 Byte (Path Signal Label Byte) Unstable Indicator:
	Unstable Condition		This READ ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the "Path Signal Label Byte" Unstable condition.
		200	The Receive STS-1 POH Processor block will declare a C2 (Path Signal Label Byte) Unstable condition, whenever the "C2 Unstable" counter reaches the value "5". The "C2 Unstable" counter will be incremented for each time that it receives an SPE with a C2 byte value that differs from the previously received C2 byte value. The "C2 Unstable" counter is cleared to "0" whenever the Receive STS-1 POH Processor block has received 3 (or 5) consecutive SPEs of the same C2 byte value.
		11.93	Note: Receiving a given C2 byte value in 3 (or 5) consecutive SPEs also sets this bit-field to "0".
			0 – C2 (Path Signal Label Byte) Unstable condition is NOT declared.
			1 – C2 (Path Signal Label Byte) Unstable condition is currently declared.
5	UNEQ-P	R/O	Path – Unequipped Indicator (UNEQ-P):
			This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the UNEQ-P condition.
			The Receive STS-1 POH Processor block will declare a UNEQ-P condition, if it receives at least five (5) consecutive STS-1 frames, in which the C2 byte was set to 0x00 (which indicates that the SPE is "Unequipped").
			The Receive STS-1 POH Processor block will clear the UNEQ-P condition, if it receives at least five (5) consecutive STS-1 frames, in which the C2 byte was set to a value other than 0x00.
			0 - Indicates that the Receive STS-1 POH Processor block is NOT declaring the

1	T	1	LINEO D. 199
			UNEQ-P condition.
			1 – Indicates that the Receive STS-1 POH Processor block is currently declaring the UNEQ-P condition.
			Note: The Receive STS-1 POH Processor block will not declare the UNEQ-P condition if it configured to expect to receive STS-1 frames with C2 bytes being set to "0x00" (e.g., if the "Receive STS-1 Path – Expected Path Label Value" Register –Address Location= 0xN197) is set to "0x00".
4	PLM-P	R/O	Path Payload Mismatch Indicator (PLM-P):
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the PLM-P condition.
			The Receive STS-1 POH Processor block will declare an PLM-P condition, if it receives at least five (5) consecutive STS-1 frames, in which the C2 byte was set to a value other than that which it is expecting to receive.
			Whenever the Receive STS-1 POH Processor block is determine whether or not it should declare the PLM-P defect, it checks the contents of the following two registers.
			The "Receive STS-1 Path Received Path Label Value" Register (Address Location= 0xN196).
			The "Receive STS-1 Path – Expected Path Label Value" Register (Address Location= 0xN197).
			The "Receive STS-1 Path - Expected Path Label Value" Register contains the value of the C2 bytes, that the Receive STS-1 POH Processor blocks expects to receive.
			The "Receive STS-1 Path - Received Path Label Value" Register contains the value of the C2 byte, that the Receive STS-1 POH Processor block has most received "validated" (by receiving this same C2 byte in five consecutive STS-1 frames).
			The Receive STS-1 POH Processor block will declare a PLM-P condition, if the contents of these two register do not match. The Receive STS-1 POH Processor block will clear the PLM-P condition if whenever the contents of these two registers do match.
		6	0 -PLM-P defect is currently not being declared.
		of	1 – PLM-P defect is currently being declared.
	(%	0 0	Note: The Receive STS-1 POH Processor block will clear the PLM-P defect, upon detecting the UNEQ-P condition.
3	RDI-P	R/O	Path Remote Defect Indicator (RDI-P):
		'0'	This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the RDI-P condition.
			If the Receive STS-1 POH Processor block is configured to support the "Single-bit RDI-P" function, then it will declare an RDI-P condition if Bit 5 (within the G1 byte of the incoming STS-1 frame) is set to "1" for "RDI-P_THRD" number of consecutive STS-1 frames.
			If the Receive STS-1 POH Processor block is configured to support the Enhanced RDI-P" (ERDI-P) function, then it will declare an RDI-P condition if Bits 5, 6 and 7 (within the G1 byte of the incoming STS-1 frame) are set to [0, 1, 0], [1, 0, 1] or [1, 1, 0] for "RDI-P_THRD" number of consecutive STS-1 frames.
			0 – Indicates that the Receive STS-1 POH Processor block is NOT declaring an RDI-P condition.
			1 – Indicates that the Receive STS-1 POH Processor block is currently declaring an RDI-P condition.

			Note: The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-1 Path – SONET Receive RDI-P Register (Address Location= 0xN193).
2	RDI-P	R/O	RDI-P (Path – Remote Defect Indicator) Unstable:
	Unstable		This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the "RDI-P Unstable" condition. The Receive STS-1 POH Processor block will declare a "RDI-P I Unstable" condition whenever the "RDI-P Unstable Counter" reaches the value "RDI-P THRD". The "RDI-P Unstable" counter is incremented for each time that the Receive STS-1 POH Processor block receives an RDI-P value that differs from that of the previous STS-1 frame. The "RDI-P Unstable" counter is cleared to "0" whenever the same RDI-P value is received in "RDI-P_THRD" consecutive STS-1 frames.
			Note: Receiving a given RDI-P value, in "RDI-P_THRD" consecutive STS-1 frames also clears this bit-field to "0"
			0 – RDI-P Unstable condition is NOT declared.
			1 – RDI-P Unstable condition is currently declared.
			Note: The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-1 Path – SONET Receive RDI-P Register (Address Location= 0xN193).
1	LOP-P	R/O	Loss of Pointer Indicator (LOP-P):
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the LOP (Loss of Pointer) condition.
			The Receive STS-1 POH Processor block will declare the LOP-P condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the TOH) within 8 to 10 consecutive SONET frames. Further, the Receive STS-1 POH Processor block will declare the LOP-P condition, if it detects 8 to 10 consecutive NDF events.
			The Receive STS-1 POH Processor block will clear the LOP-P condition, whenever the Receive STS-1 POH Processor detects valid pointer bytes (e.g., the H1 and H2 bytes, within the TOH) and normal NDF value for three consecutive STS-1 frames.
			0 Indicates that the Receive STS-1 POH Processor block is NOT declaring the LOP-P condition.
		we c	1 - Indicates that the Receive STS-1 POH Processor block is currently declaring the LOP P condition.
0	AIS-P	R/O	Path AIS (AIS-P) Indicator:
			This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring an AIS-P condition. The Receive STS-1 POH Processor block will declare an AIS-P if it detects all of the following conditions for three consecutive STS-1 frames.
			The H1, H2 and H3 bytes are set to an "All Ones" pattern.
			The entire SPE is set to an "All Ones" pattern.
			The Receive STS-1 POH Processor block will clear the AIS-P indicator when it detects a valid STS-1 pointer (H1 and H2 bytes) and a "set" or "normal" NDF for three consecutive STS-1 frames.
			0 - Indicates that the Receive STS-1 POH Processor block is NOT currently declaring the AIS-P condition.
			1 – Indicates that the Receive STS-1 POH Processor block is currently declaring the AIS-P condition.
			Note: The Receive STS-1 POH Processor block will NOT declare the LOP-P

It will, instead, declare the AIS-P condition.				condition if it detects an "All Ones" pattern in the H1, H2 and H3 bytes. It will, instead, declare the AIS-P condition.
--	--	--	--	--

The product are no longered (Oss)



Table 356: Receive STS-1 Path – SONET Receive Path Interrupt Status – Byte 2 (Address Location= 0xN189)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		Detection of AIS Pointer Interrupt Status	Detection of Pointer Change Interrupt Status	Unused	Change in TIM-P Condition Interrupt Status	Change in J1 Unstable Condition Interrupt Status
R/O	R/O	R/O	RUR	RUR	R/O	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 5	Unused	R/O	"his red
4	Detection of AIS Pointer Interrupt Status	RUR	Detection of AIS Pointer Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Detection of AIS Pointer" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate this interrupt anytime it detects an "AIS Pointer" in the incoming STS-1 data stream. Note: An "AIS Pointer" is defined as a condition in which both the H1 and H2 bytes (within the TOH) are each set to an "AII Ones" pattern.
		orpro	0 - Indicates that the "Detection of AIS Pointer" interrupt has NOT occurred since the last read of this register. 1 - Indicates that the "Detection of AIS Pointer" interrupt has occurred since the last read of this register.
3	Detection of Pointer Change Interrupt Status	RUR	This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Change" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it accepts a new pointer value (e.g., H1 and H2 bytes, in the TOH bytes). 0 – Indicates that the "Detection of Pointer Change" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of Pointer Change" Interrupt has
2	Unused	R/O	occurred since the last read of this register.
_		. , ,	
1	Change in TIM-P Condition Interrupt Status	RUR	Change in TIM-P (Trace Identification Mismatch) Condition Interrupt. This RESET-upon-READ bit-field indicates whether or not the "Change in TIM-P" Condition interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events.

not occurred since the last read of this register. 1 – Indicates that the "Change in TIM-P Condition" Interrupt had occurred since the last read of this register. O Change in J1 Unstable Condition Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change in J1 Unstable Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 POP Processor block will generate an interrupt in response to either the following events. • When the Receive STS-1 POH Processor block declare the "J1 Unstable" Condition. • When the Receive STS-1 POH Processor block clears the "Unstable" condition. • When the Receive STS-1 POH Processor block clears the "Unstable" condition. • Indicates that the "Change in J1 Unstable Condition Interrupt has NOT occurred since the last read of this register.				
0 — Indicates that the "Change in TIM-P Condition" Interrupt had not occurred since the last read of this register. 1 — Indicates that the "Change in TIM-P Condition" Interrupt had occurred since the last read of this register. RUR Change in "J1 (Trace Identification Message) Unstabe Condition" Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change in J1 Unstable Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 PC Processor block will generate an interrupt in response to either the following events. • When the Receive STS-1 POH Processor block declare the "J1 Unstable" Condition. • When the Receive STS-1 POH Processor block clears the "Unstable" condition. 0 — Indicates that the "Change in J1 Unstable Condition Interrupt has NOT occurred since the last read of this register.				If the TIM-P condition is declared.
not occurred since the last read of this register. 1 - Indicates that the "Change in TIM-P Condition" Interrupt had occurred since the last read of this register. Change in "J1 (Trace Identification Message) Unstable Condition Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change in J1 Unstable Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 PC Processor block will generate an interrupt in response to either the following events. When the Receive STS-1 POH Processor block declare the "J1 Unstable" Condition. When the Receive STS-1 POH Processor block clears the "Unstable" condition O - Indicates that the "Change in J1 Unstable Condition Interrupt has NOT occurred since the last read of this register.				If the TIM-P condition is cleared.
Occurred since the last read of this register. RUR Change in "J1 (Trace Identification Message) Unstable Condition Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change in J1 Unstable Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 PC Processor block will generate an interrupt in response to either the following events. When the Receive STS-1 POH Processor block declare the "J1 Unstable" Condition. When the Receive STS-1 POH Processor block clears the "Unstable" condition. Interrupt has NOT occurred since the last read of this register.				0 – Indicates that the "Change in TIM-P Condition" Interrupt has not occurred since the last read of this register.
Condition Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change in J1 Unstable Condition" Interrupt has occurred sind the last read of this register. If this interrupt is enabled, then the Receive STS-1 PC Processor block will generate an interrupt in response to either the following events. • When the Receive STS-1 POH Processor block declare the "J1 Unstable" Condition. • When the Receive STS-1 POH Processor block clears the "Unstable" condition. • This RESET-upon-READ bit-field indicates whether or not the "Change in J1 Unstable Condition on the "Change in J1 Unstable Change in J1 Unstable Cha				1 – Indicates that the "Change in TIM-P Condition" Interrupt has occurred since the last read of this register.
"Change in J1 Unstable Condition" Interrupt has occurred sind the last read of this register. If this interrupt is enabled, then the Receive STS-1 PC Processor block will generate an interrupt in response to either the following events. • When the Receive STS-1 POH Processor block declare the "J1 Unstable" Condition. • When the Receive STS-1 POH Processor block clears the "Unstable" condition. • Unstable "condition. 0 — Indicates that the "Change in J1 Unstable Condition Interrupt has NOT occurred since the last read of this register.	0		RUR	Change in "J1 (Trace Identification Message) Unstable Condition" Interrupt Status:
Processor block will generate an interrupt in response to either the following events. • When the Receive STS-1 POH Processor block declare the "J1 Unstable" Condition. • When the Receive STS-1 POH Processor block clears the "Unstable" condition. 0 — Indicates that the "Change in J1 Unstable Condition Interrupt has NOT occurred since the last read of this register.				This RESET-upon-READ bit-field indicates whether or not the "Change in J1 Unstable Condition" Interrupt has occurred since the last read of this register.
"J1 Unstable" Condition. • When the Receive STS-1 POH Processor block clears the " Unstable" condition. 0 — Indicates that the "Change in J1 Unstable Condition Interrupt has NOT occurred since the last read of this register.				If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events.
Unstable" condition 0 — Indicates that the "Change in J1 Unstable Condition Interrupt has NOT occurred since the last read of this register.				When the Receive STS-1 POH Processor block declare the "J1 Unstable" Condition.
Interrupt has NOT occurred since the last read of this register.				When the Receive STS-1 POH Processor block clears the "J1 Unstable" condition.
1 - Indicates that the "Change in J1 Unstable Condition Interrupt has occurred since the last read of this register.				0 - Indicates that the "Change in J1 Unstable Condition" Interrupt has NOT occurred since the last read of this register.
The product are no ordered of the product are not be ordered of the product are not be ordered.				1 — Indicates that the "Change in J1 Unstable Condition" Interrupt has occurred since the last read of this register.
		The product of and may	production of the production o	ordered Ob

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 357: Receive STS-1 Path – SONET Receive Path Interrupt Status – Byte 1 (Address Location= 0xN18A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
New J1 Message Interrupt Status	Detection of REI-P Event Interrupt Status	Change in UNEQ-P Condition Interrupt Status	Change in PLM-P Condition Interrupt Status	New C2 Byte Interrupt Status	Change in C2 Byte Unstable Condition Interrupt Status	Change in RDI-P Unstable Condition Interrupt Status	New RDI-P Value Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	New J1	RUR	New J1 (Trace Identification) Message Interrupt Status:
	Message Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "New J1 Message" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it has accepted (or validated) and new J1 (Trace Identification) Message.
			0 – Indicates that the "New J1 Message" Interrupt has NOT occurred since the last read of this register.
			1 - Indicates that the "New J1-Message" Interrupt has occurred since the last read of this register.
6	Detection of	RUR	Detection of REI-P Event Interrupt Status:
	REI-P Event Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of REI-P Event" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects an REI-P condition in the coming STS-1 data-stream.
		odu	0 Indicates that the "Detection of REI-P Event" Interrupt has NOT occurred since the last read of this register.
		6, 8	1 – Indicates that the "Detection of REI-P Event" Interrupt has occurred since the last read of this register.
5	Change in	RUR	Change in UNEQ-P (Path – Unequipped) Condition Interrupt Status:
	UNEQ-P Condition Interrupt Status	o all	This RESET-upon-READ bit-field indicates whether or not the "Change in UNEQ-P Condition" interrupt has occurred since the last read of this register.
			If this interrupt is enabled , then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following conditions.
			When the Receive STS-1 POH Processor block declares the UNEQ-P Condition.
			When the Receive STS-1 POH Processor block clears the UNEQ-P Condition.
			0 - Indicates that the "Change in UNEQ-P Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in UNEQ-P Condition" Interrupt has occurred since the last read of this register.
			Note: The user can determine the current state of UNEQ-P by reading

			out the state of Bit 5 (UNEQ-P Defect Declared) within the "Receive STS-1 Path – SONET Receive POH Status – Byte 0" Register (Address Location= 0xN187).
4	Change in PLM- P Condition Interrupt Status	RUR	Change in PLM-P (Path – Payload Mismatch) Condition Interrupt Status:
	mioriapi diatas		This RESET-upon-READ bit indicates whether or not the "Change in PLM-P Condition" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following conditions.
			When the Receive STS-1 POH Processor block declares the "PLM-P" Condition.
			When the Receive STS-1 POH Processor block clears the "PLM-P" Condition.
			0 – Indicates that the "Change in PLM-P Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in PLM-P Condition" Interrupt has occurred since the last read of this register.
3	New C2 Byte	RUR	New C2 Byte Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "New C2 Byte" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it has accepted a new C2 byte.
			0 - Indicates that the "New C2 Byte" Interrupt has NOT occurred since the last read of this register.
			1 - Indicates that the "New C2 Byte" Interrupt has occurred since the last read of this register.
2	Change in C2	RUR	Change in C2 Byte Unstable Condition Interrupt Status:
	Byte Unstable Condition Interrupt Status	Juck	This RESET-upon-READ bit-field indicates whether or not the "Change in C2 Byte Unstable Condition" Interrupt has occurred since the last read of this register.
	or	0,400	If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events.
	They	9 11	When the Receive STS-1 POH Processor block declares the "C2 Byte Unstable" condition.
	, 90	ano	When the Receive STS-1 POH Processor block clears the "C2 Byte Unstable" condition.
			0 – Indicates that the "Change in C2 Byte Unstable Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in C2 Byte Unstable Condition" Interrupt has occurred since the last read of this register.
			Note: The user can determine the current state of "C2 Byte Unstable Condition" by reading out the state of Bit 6 (C2 Byte Unstable Condition) within the "Receive STS-1 Path — SONET Receive POH Status — Byte 0" Register (Address Location= 0xN187).
1	Change in RDI-	RUR	Change in RDI-P Unstable Condition Interrupt Status:
	P Unstable Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in RDI-P Unstable Condition" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			generate an interrupt in response to either of the following conditions.
			When the Receive STS-1 POH Processor block declares an "RDI-P Unstable" condition.
			When the Receive STS-1 POH Processor block clears the "RDI-P Unstable" condition.
			0 – Indicates that the "Change in RDI-P Unstable Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in RDI-P Unstable Condition" Interrupt has occurred since the last read of this register.
			Note: The user can determine the current state of "RDI-P Unstable" by reading out the state of Bit 2 (RDI-P Unstable Condition) within the "Receive STS-1 Path – SONET Receive POH Status – Byte 0" Register (Address Location= 0xN187).
0	New RDI-P Value Interrupt Status	RUR	New RDI-P Value Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "New RDI-P Value" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate this interrupt anytime it receives and "validates" a new RDI-P value. 0 – Indicates that the "New RDI-P Value" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "New RDI-P Value" Interrupt has occurred since the last read of this register. Note: The user can obtain the "New RDI-P Value" by reading out the contents of the "RDI-P ACCEPT[2:0]" bit-fields. These bit-fields are located in Bits 6 through 4, within the "Receive STS-1 Path – SONET Receive RDI-P Register" (Address Location= 0xN193).
	The	or odd datand	contents of the "RDI-P ACCEPT[2:0]" bit-fields. These bit-fields are located in Bits 6 through 4, within the "Receive STS-1 Path – SONET Receive RDI-P Register" (Address Location= 0xN193).

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 358: Receive STS-1 Path – SONET Receive Path Interrupt Status – Byte 0 (Address Location= 0xN18B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Detection of B3 Byte Error Interrupt Status	Detection of New Pointer Interrupt Status	Detection of Unknown Pointer Interrupt Status	Detection of Pointer Decrement Interrupt Status	Detection of Pointer Increment Interrupt Status	Detection of NDF Pointer Interrupt Status	Change of LOP-P Condition Interrupt Status	Change of AIS-P Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Detection of B3 Byte Error Interrupt Status	RUR	Detection of B3 Byte Error Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Detection of B3 Byte Error" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a B3 byte error in the incoming STS-1 data stream. 0 – Indicates that the "Detection of B3 Byte Error" Interrupt has NOT occurred since the last read of this interrupt. 1 – Indicates that the "Detection of B3 Byte Error" Interrupt has occurred since the last read of this interrupt.
6	Detection of New Pointer Interrupt Status Detection of Unknown Pointer Interrupt	RUR	Detection of New Pointer Interrupt Status: This RESET-upon-READ indicates whether the "Detection of New Pointer" interrupt has occurred since the last read of this register. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a new pointer value in the incoming STS-1 frame. Note: Pointer Adjustments with NDF will not generate this interrupt. 0 – Indicates that the "Detection of New Pointer" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of New Pointer" Interrupt has occurred since the last read of this register.
5	Detection of Unknown Pointer Interrupt Status	RUR	Detection of Unknown Pointer Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Detection of Unknown Pointer" interrupt has occurred since the last read of this register. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime that it detects a "pointer" that does not fit into any of the following categories. • An Increment Pointer • A Decrement Pointer • An NDF Pointer • An AIS (e.g., All Ones) Pointer • New Pointer 0 – Indicates that the "Detection of Unknown Pointer" interrupt has NOT

			occurred since the last read of this register.
			1 – Indicates that the "Detection of Unknown Pointer" interrupt has occurred since the last read of this register.
4	Detection of Pointer	RUR	Detection of Pointer Decrement Interrupt Status:
	Decrement Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Decrement" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a "Pointer Decrement" event.
			0 - Indicates that the "Detection of Pointer Decrement" interrupt has NOT occurred since the last read of this register.
			1 - Indicates that the "Detection of Pointer Decrement" interrupt has occurred since the last read of this register.
3	Detection of Pointer	RUR	Detection of Pointer Increment Interrupt Status:
	Increment Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Increment" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a "Pointer Increment" event.
			0 – Indicates that the "Detection of Pointer Increment" interrupt has NOT occurred since the last read of this register.
			1 - Indicates that the 'Detection of Pointer Increment" interrupt has occurred since the last read of this register.
2	Detection of NDF	RUR	Detection of NDF Pointer Interrupt Status:
	Pointer Interrupt Status	duct	This RESET-upon-READ bit-field indicates whether or not the "Detection of NDF Pointer" interrupt has occurred since the last read of this register. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects an NDF Pointer event.
	A CONTRACTOR OF THE CONTRACTOR		Or Indicates that the "Detection of NDF Pointer" interrupt has NOT occurred since the last read of this register.
	Theor	SIME	1 – Indicates that the "Detection of NDF Pointer" interrupt has occurred since the last read of this register.
1	Change of LOP-P	RUR	Change of LOP-P Condition Interrupt Status:
	Condition Interrupt Status	•	This RESET-upon-READ bit-field indicates whether or not the "Change in LOP-P Condition" interrupt has occurred since the last read of this register.
			If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events.
			When the Receive STS-1 POH Processor block declares an "Loss of Pointer" condition.
			When the Receive "STS-1 POH Processor" block clears the "Loss of Pointer" condition.
			0 – Indicates that the "Change in LOP-P Condition" interrupt has NOT occurred since the last read of this register.
			1 - Indicates that the "Change in LOP-P Condition" interrupt has

3-CHANNEL DS3/E3/STS-1	TO STS-3/STM-1 MAPPER	R – ATM REGISTERS
------------------------	-----------------------	-------------------

			occurred since the last read of this register.
			Note: The user can determine the current state of LOP-P by reading out the state of Bit 1 (LOP-P Defect Declared) within the "Receive STS-1 Path – SONET Receive POH Status – Byte 0" Register (Address Location=0xN187).
0	Change of AIS-P	RUR	Change of AIS-P Condition Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of AIS-P Condition" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events.
			When the Receive STS-1 POH Processor block declares an AIS-P condition.
			When the Receive STS POH Processor block clears the AIS-P condition.
			0 – Indicates that the "Change of AIS-P Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change of AIS-P Condition" Interrupt has occurred since the last read of this register.
			Note: The user can determine the current state of AIS-P by reading out the state of Bit 0 (AIS-P Defect Declared) within the "Receive STS-1 Path – SONET Receive POH Status – Byte 0" Register (Address Location= 0xN187).
	The data and	est of the state o	"Receive STS-1 Path – SONET Receive POH Status – Byte 0" Register (Address Location= 0xN187).



Rev 2.0.0

Table 359: Receive STS-1 Path – SONET Receive Path Interrupt Enable – Byte 2 (Address Location = 0xN18D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		Detection of AIS Pointer Interrupt Enable	Detection of Pointer Change Interrupt Enable	Unused	Change in TIM-P Condition Interrupt Enable	Change in J1 Unstable Condition Interrupt Enable
R/O	R/O	R/O	R/W	R/W	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7-5	Unused	R/O	nis red
4	Detection of AIS Pointer	R/W	Detection of AIS Pointer Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of AIS Rointer" interrupt.
			If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects an "AIS Pointer", in the incoming STS-1 data stream.
			Note: An "AIS Pointer" is defined as a condition in which both the H1 and H2 bytes (within the TOH) are each set to an "All Ones" Pattern
			0 - Disables the "Detection of AIS Pointer" Interrupt.
			1 – Enables the "Detection of AIS Pointer" Interrupt.
3	Detection of Pointer	R/W	Detection of Pointer Change Interrupt Enable:
	Change Interrupt Enable	, (0)	This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Pointer Change" Interrupt.
		C n	If this interrupt is enabled, then the Receive STS-1 POH Processor
	6	o l	block will generate an interrupt anytime it has accepted a new pointer value.
	oro	No 7	0 – Disables the "Detection of Pointer Change" Interrupt.
	10° 10°	3/10	1 - Enables the "Detection of Pointer Change" Interrupt.
2	Unused	R/O	
1	Change in TIM-P Condition Interrupt	R/W	Change in TIM-P (Trace Identification Mismatch) Condition Interrupt:
	Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in TIM-P Condition" interrupt.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events.
			If the TIM-P condition is declared.
			If the TIM-P condition is cleared.
			0 – Disables the "Change in TIM-P Condition" Interrupt.
			1 – Enables the "Change in TIM-P Condition" Interrupt.
0	Change in J1 Unstable Condition Interrupt	R/W	Change in "J1 (Trace Identification Message) Unstable Condition" Interrupt Status:

S

Rev 2.0.0	3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Enable	Condition" Interrupt Status:
	This READ/WRITE bit-field permits the user to either enable or disable the "Change in J1 (Trace Identification) Message Unstable Condition" Interrupt.
	If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events.
	When the Receive STS-1 POH Processor block declares the "J1 Unstable" Condition.
	When the Receive STS-1 POH Processor block clears the "J1 Unstable" Condition.
	0 – Disables the "Change in J1 Message Unstable Condition" interrupt.
	1 – Enables the "Change in John Message Unstable Condition" interrupt.
The product	1 - Enables the "Change in Ja Message Unstable Condition" interrupt. 1 - Enables the "Change in Ja Message Unstable Condition" interrupt.

fience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 360: Receive STS-1 Path – SONET Receive Path Interrupt Enable – Byte 1 (Address Location= 0xN18E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
New J1 Message Interrupt Enable	Detection of REI-P Event Interrupt Enable	Change in UNEQ-P Condition Interrupt Enable	Change in PLM-P Condition Interrupt Enable	New C2 Byte Interrupt Enable	Change in C2 Byte Unstable Condition Interrupt Enable	Change in RDI-P Unstable Condition Interrupt Enable	New RDI-P Value Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	New J1 Message	R/W	New J1 (Trace Identification) Message Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "New J1 Message" Interrupt.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it has accepted (or validated) and new J1 (Trace Identification) Message.
			0 – Disables the "New J1 Message" Interrupt.
			1 – Enables the "New J1 Message" Interrupt.
6	Detection of REI-P	R/W	Detection of REI-P Event Interrupt Enable:
	Event Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of REI-P Event" Interrupt.
		(If this interrupt is enabled, then he Receive STS-1 POH Processor block will generate an interrupt anytime it detects an REI-P condition in the coming STS-1 data-stream.
			0-2 Disables the "Detection of REI-P Event" Interrupt.
		X VIX	Enables the "Detection of REI-P Event" Interrupt.
5	Change in UNEQ-P	R/W	Change in UNEQ-P (Path – Unequipped) Condition Interrupt Enable:
	Enable	o M	This READ/WRITE bit-field permits the user to either enable or disable the "Change in UNEQ-P Condition" interrupt.
		and	If this interrupt is enabled , then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following conditions.
			When the Receive STS-1 POH Processor block declares the UNEQ-P Condition.
			When the Receive STS-1 POH Processor block clears the UNEQ-P Condition.
			0 - Disables the "Change in UNEQ-P Condition" Interrupt.
			1 – Enables the "Change in UNEQ-P Condition" Interrupt.
4	Change in PLM-P Condition Interrupt	R/W	Change in PLM-P (Path – Payload Mismatch) Condition Interrupt Enable:
	Enable		This READ/WRITE bit permits the user to either enable or disable the "Change in PLM-P Condition" interrupt.
			If this interrupt is enabled, then the Receive STS-1 POH Processor

			block will generate an interrupt in response to either of the following conditions.
			• When the Receive STS-1 POH Processor block declares the "PLM-P" Condition.
			When the Receive STS-1 POH Processor block clears the "PLM-P" Condition.
			0 – Disables the "Change in PLM-P Condition" Interrupt.
			1 – Enables the "Change in PLM-P Condition" Interrupt.
3	New C2 Byte Interrupt Enable	R/W	New C2 Byte Interrupt Enable:
	ппенирі Епаріе		This READ/WRITE bit-field permits the user to either enable or disable the "New C2 Byte" Interrupt.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it has accepted a new C2 byte. 0 – Disables the "New C2 Byte" Interrupt.
			1 – Enables the "New C2 Byte" Interrupt.
			Note: The user can obtain the value of this "New C2" byte by reading the contents of the "Receive STS-1 Path – Received Path Label Value" Register (Address Location= 0xN196).
2	Change in C2 Byte	R/W	Change in C2 Byte Unstable Condition Interrupt Enable:
	Unstable Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in C2 Byte Unstable Condition" Interrupt.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events.
		, 0	• When the Receive STS-1 POH Processor block declares the "C2 Byte Unstable" condition.
		10.	When the Receive STS-1 POH Processor block clears the "C2 Byte Unstable" condition.
		7 V.	0 Disables the "Change in C2 Byte Unstable Condition" Interrupt.
	400	8	– Enables the "Change in C2 Byte Unstable Condition" Interrupt.
1	Change in RDI-P	R/W	Change in RDI-P Unstable Condition Interrupt Enable:
	Unstable Condition Interrupt Enable	Mo	This READ/WRITE bit-field permits the user to either enable or disable the "Change in RDI-P Unstable Condition" interrupt.
	and		If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following conditions.
			When the Receive STS-1 POH Processor block declares an "RDI-P Unstable" condition.
			When the Receive STS-1 POH Processor block clears the "RDI-P Unstable" condition.
			0 – Disables the "Change in RDI-P Unstable Condition" Interrupt.
			1 – Enables the "Change in RDI-P Unstable Condition" Interrupt.
0	New RDI-P Value Interrupt Enable	R/W	New RDI-P Value Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "New RDI-P Value" interrupt.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate this interrupt anytime it receives and "validates" a

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

	new RDI-P value.
	0 – Disables the "New RDI-P Value" Interrupt.
	1 – Enable the "New RDI-P Value" Interrupt.

The product are no ordered (OBS)

The product are no be ordered (OBS)

Table 361: Receive STS-1 Path – SONET Receive Path Interrupt Enable – Byte 0 (Address Location= 0xN18F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Detection of B3 Byte Error Interrupt Enable	Detection of New Pointer Interrupt Enable	Detection of Unknown Pointer Interrupt Enable	Detection of Pointer Decrement Interrupt Enable	Detection of Pointer Increment Interrupt Enable	Detection of NDF Pointer Interrupt Enable	Change of LOP-P Condition Interrupt Enable	Change of AIS-P Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Detection of B3 Byte Error Interrupt Enable	R/W	Detection of B3 Byte Error Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B3 Byte Error" Interrupt. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a B3-byte error in the incoming STS-1 data-stream. 0 – Disables the "Detection of B3 Byte Error" interrupt. 1 – Enables the "Detection of B3 Byte Error" interrupt.
6	Detection of	R/W	Detection of New Pointer Interrupt Enable:
	New Pointer Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of New Pointer" interrupt. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a new pointer value in the incoming STS-1 frame.
			Note: Pointer Adjustments with NDF will not generate this interrupt.
			0 – Disables the "Detection of New Pointer" Interrupt.
			1 + Enables the "Detection of New Pointer" Interrupt.
5	Detection of Unknown	R/W	Detection of Unknown Pointer Interrupt Enable:
	Pointer Interrupt Enable	OT S	This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Unknown Pointer" interrupt. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a "Pointer Adjustment" that does not fit into any of the following categories.
		90 %	An Increment Pointer.
		9,	A Decrement Pointer
			An NDF Pointer
			AIS Pointer
			New Pointer.
			0 - Disables the "Detection of Unknown Pointer" Interrupt.
			1 – Enables the "Detection of Unknown Pointer" Interrupt.
4	Detection of	R/W	Detection of Pointer Decrement Interrupt Enable:
	Pointer Decrement Interrupt Enable		This READ/WRITE bit-field permits the user to enable or disable the "Detection of Pointer Decrement" Interrupt. If the user enables this interrupt, then the Receive STS-1 TOH Processor block will generate an interrupt anytime it detects a "Pointer-Decrement" event.
			0 – Disables the "Detection of Pointer Decrement" Interrupt.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			1 – Enables the "Detection of Pointer Decrement" Interrupt.
3	Detection of Pointer Increment Interrupt Enable	R/W	Detection of Pointer Increment Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Pointer Increment" Interrupt. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a "Pointer Increment" event. 0 – Disables the "Detection of Pointer Increment" Interrupt. 1 – Enables the "Detection of Pointer Increment" Interrupt.
2	Detection of NDF Pointer Interrupt Enable	R/W	Detection of NDF Pointer Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Detection of NDF Pointer" Interrupt. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects an NDF Pointer event. 0 – Disables the "Detection of NDF Pointer" interrupt. 1 – Enables the "Detection of NDF Pointer" interrupt.
1	Change of LOP-P Condition Interrupt Enable	R/W	Change of LOP-P Condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change in LOP (Loss of Pointer)" Condition interrupt. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events. • When the Receive STS-1 POH Processor block declares a "Loss of Pointer" condition. • When the Receive STS-1 POH Processor block clears the "Loss of Pointer" condition. 0 – Disable the "Change of LOP" Interrupt. 1 – Enables the "Change of LOP" Interrupt. Note: The user can determine the current state of "LOP" by reading out the contents of Bit 1 (LOP) within the "Receive STS-1 Path – SONET Receive POH Status – Byte 0" (Address Location= 0xN187).
0	Change of AIS-P Interrupt Enable	R/W	Change of AlS-P Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change of AlS-P (Path AlS)" interrupt. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events. When the Receive STS-1 POH Processor block declares an "AlS-P" condition. When the Receive STS-1 POH Processor block clears the "AlS-P" condition. Disables the "Change of AlS-P" Interrupt. The user can determine the current state of "AlS-P" by reading out the contents of Bit 0 (AlS-P Defect Declared) within the "Receive STS-1 Path — SONET Receive POH Status — Byte 0" (Address Location= 0xN187).

Table 362: Receive STS-1 Path – SONET Receive RDI-P Register (Address Location= 0xN193)

BIT 7 BIT 6 BIT 5 BIT 4 BIT 3 BIT 2	Віт 1 Віт 0
---	-------------



Unused	RDI-P_ACCEPT[2:0]			used RDI-P_ACCEPT[2:0] RDI-P THRESHOLD[3:0]				
R/O	R/O	R/O R/O R/O		R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7	Unused	R/O	
6 - 4	RDI-P_ACCEPT[2:0]	R/O	Accepted RDI-P Value:
			These READ-ONLY bit-fields contain the value of the most recently "accepted" RDI-P (e.g., bits 5, 6 and 7 within the G1 byte) value.
			Note: A given RDI-P value will be "accepted" by the Receive STS-1 POH Processor block, if this RDI-P value has been consistently received in "RDI-P THRESHOLD[3:0]" number of STS-1 frames.
3 - 0	RDI-P THRESHOLD[3:0]	R/W	RDI-P Threshold:
			These READ/WRITE bit-fields permit the user to defined the "RDI-P Acceptance Threshold" for the Receive STS-1 POH Processor Block.
			The "RDI-P Acceptance Threshold" is the number of consecutive STS-1 frames, in which the Receive STS-1 POH Processor block must receive a given RDI-P value, before it "accepts" or "validates" it.
			The most recently "accepted" RDI-P value is written into the "RDI-P ACCEPT[2:0]" bit-fields, within this register.
	The product of and many	or process	ordered Condered

EXAR Experience Our Connectivi

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 363: Receive STS-1 Path – Received Path Label Value (Address Location= 0xN196)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Received_C2_Byte_Value[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
1	1	1	1	1	1	1	1

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Received C2 Byte Value[7:0]	R/O	Received "Filtered" C2 Byte Value:
			These READ-ONLY bit-fields contain the value of the most recently "accepted" C2 byte, via the Receive STS-1 POH Processor block. The Receive STS-1 POH Processor block will "accept" a C2 byte value (and load it into these bit-fields) if it has received a consistent C2 byte, in five (5) consecutive STS-1 frames. Note: The Receive STS-1 POH Processor block uses this register, along the "Receive STS-1 Path – Expected Path Label Value" Register (Address Location = 0x(197), when declaring or clearing the UNEQ-P and PLM-P alarm conditions.

Table 364: Receive STS-1 Path - Expected Path Label Value (Address Location= 0xN197)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 2	Віт 1	Віт 0	
Expected_C2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W R/W	R/W	R/W	R/W	
1	1	1	100 0 1	1	1	1	

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Expected C2 Byte Value[7:0]	R/W	Expected C2 Byte Value:
	The proshed his	3	These READ/WRITE bit-fields permits the user to specify the C2 (Path Label Byte) value, that the Receive STS-1 POH Processor block should expect when declaring or clearing the UNEQ-P and PLM-P alarm conditions.
	and		If the contents of the "Received C2 Byte Value[7:0]" (see "Receive STS-1 Path – Received Path Label Value" register) matches the contents in these register, then the Receive STS-1 POH will not declare any alarm conditions.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 365: Receive STS-1 Path - B3 Error Count Register - Byte 3 (Address Location= 0xN198)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			B3_Error_C	ount[31:24]			
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	B3_Error_Count[31:24]	RUR	B3 Error Count – MSB:
			This RESET-upon-READ register, along with "Receive STS-1 Path – B3 Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a B3 byte error. *Note:* 1. If the B3 Error Type is configured to be "bit errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the number of bits, within the B3 value that are in error. 2. If the B3 Error Type is configured to be "frame errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the number of frames that contain erred B3 bytes.

Table 366: Receive STS-1 Path - B3 Error Count Register - Byte 2 (Address Location= 0xN199)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0
			B3_Error_C	ount[23:16]			
RUR	RUR	RUR	RUR X	RUR	RUR	RUR	RUR
0	0	0 (0	000	0	0	0	0

BIT NUMBER	NAME	O TYPE	DESCRIPTION
7 - 0	B3_Error_Count[23:16]	RUR	B3 Error Count (Bits 23 through 16):
	The bata	(18)	This RESET-upon-READ register, along with "Receive STS-1 Path – B3 Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a B3 byte error.
	'		Note:
			1. If the B3 Error Type is configured to be "bit errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the number of bits, within the B3 value that are in error.
			2. If the B3 Error Type is configured to be "frame errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the number of frames that contain erred B3 bytes.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 367: Receive STS-1 Path - B3 Error Count Register - Byte 1 (Address Location= 0xN19A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			B3_Error_0	Count[15:8]			
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	B3_Error_Count[15:8]	RUR	B3 Error Count – (Bits 15 through 8):
			This RESET-upon-READ register, along with "Receive STS-1 Path – B3 Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a B3 byte error. *Note:* 1. If the B3 Error Type is configured to be "bit errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the number of bits, within the B3 value that are in error. 2. If the B3 Error Type is configured to be "frame errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the number of frames that contain erred B3 bytes.

Table 368: Receive STS-1 Path - B3 Error Count Register - Byte 0 (Address Location= 0xN19B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 2	Віт 1	Віт 0
			B3_Error_Count[7:0]			
RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0 0	0	0	0

BIT NUMBER	Name	YPE	DESCRIPTION
7 - 0	B3_Error_Count[7:0]	RUR	B3 Error Count - LSB:
	They	andma	This RESET-upon-READ register, along with "Receive STS-1 Path – B3 Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a B3 byte error.
	(0	Note:
			1. If the B3 Error Type is configured to be "bit errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the number of bits, within the B3 value that are in error.
			2. If the B3 Error Type is configured to be "frame errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the number of frames that contain erred B3 bytes.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 369: Receive STS-1 Path – REI-P Error Count Register – Byte 3 (Address Location= 0xN19C)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			REI_P_Error_	_Count[31:24]			
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	REI_P_Error_Count[31:24]	RUR	REI-P Error Count – MSB:
			This RESET-upon-READ register, along with "Receive STS-1 Path – REI-P Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a Path – Remote Error Indicator. Note: 1. If the REI-P Error Type is configured to be "bit errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the hibble-value within the REI-P field of the incoming G1 byte. 2. If the REI-P Error Type is configured to be "frame errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the number of frames that contain non-zero REI-P values.

Table 370: Receive STS-1 Path – REI_P Error Count Register – Byte 2 (Address Location= 0xN19D)

Віт 7	Віт 6	Віт 5	Вп 4	Віт 3	Віт 2	Віт 1	Віт 0
			REI_P_Error_	_Count[23:16]			
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	QC		0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	REI_P_Error_Count[23:16]	RUR	REI-P Error Count (Bits 23 through 16):
	11 dated 1		This RESET-upon-READ register, along with "Receive STS-1 Path – REI-P Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a Path – Remote Error Indicator.
			Note:
			1. If the REI-P Error Type is configured to be "bit errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the nibble-value within the REI-P field of the incoming G1 byte.
			2. If the REI-P Error Type is configured to be "frame errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the number of frames that contain non-zero REI-P values.



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 371: Receive STS-1 Path – REI_P Error Count Register – Byte 1 (Address Location= 0xN19E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	REI_P_Error_Count[15:8]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	REI_P_Error_Count[15:8]	RUR	REI-P Error Count – (Bits 15 through 8)
			This RESET-upon-READ register, along with "Receive STS-1 Path – REI-P Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a Path – Remote Error Indicator. Note: 1. If the REI-P Error Type is configured to be "bit errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the nibble-value within the REI-P field of the incoming G1 byte. 2. If the REI-P Error Type is configured to be "frame errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the number of frames that contain non-zero REI-P values.

Table 372: Receive STS-1 Path – REI_P Error Count Register – Byte 0 (Address Location= 0xN19F)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0		
	REI_P Grror Count[7:0]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0 (200	0	0	0	0		

BIT NUMBER	NAME TYPE	DESCRIPTION
7 - 0	REI_P_Error_Count[7:0] RUR	REI-P Error Count – LSB:
	1, 93, 91,	This RESET-upon-READ register, along with "Receive STS-1 Path – REI-P Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a Path – Remote Error Indicator.
		Note:
		1. If the REI-P Error Type is configured to be "bit errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the nibble-value within the REI-P field of the incoming G1 byte.
		2. If the REI-P Error Type is configured to be "frame errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the number of frames that contain non-zero REI-P values.

Table 373: Receive STS-1 Path - Receive J1 Control Register (Address Location= 0xN1A3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		Receive J1 Message Buffer Read Select	Accept Threshold	Message Type	Message Le	ength[1:0]
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре		DESCRIPTION				
7 – 5	Unused	R/O						
4	Received J1 Message	R/W	J1 Buffer Read Se	lection:				
	Buffer Read Select		This READ/WRITE following buffer seg	bit-field permits a user to specify which of the ments to read.				
			a. Valid Message Buffer					
			b. Expected I	Message Buffer				
				EAD to the Receive J1 Trace Buffer, will return "Valid Message" buffer.				
				EAD to the Receive J1 Trace Buffer, will return "Expected Message Buffer".				
			"Receive	of the Receive STS-1 POH Processor block, the In Trace Buffer" is located at Address Location brough 0xN53F.				
3	Accept Threshold	R/W	Message Accept T	hreshold:				
		or pr	This READ/WRITE bit-field permits a user to select the numbe consecutive times that the Receive STS-1 POH Processor blanust feceive a given J1 Trace Message, before it is accepted, described below.					
	, juc [†]	* SIO		STS-1 POH Processor block accepts the J1 s received it the third time in succession.				
	oroche	8,40		SONET POH Processor block accepts the J1 s received in the fifth time in succession.				
2	Message Type	R/O	Message Alignme	nt Type:				
	Ti datid			E bit-field permits a user to specify have the H Processor block will locate the boundary of the as indicated below.				
			0 – Message bound	lary is indicated by "Line Feed".				
				dary is indicated by the presence of a "1" in the yte (within the J1 Trace Message).				
1 – 0	Message Length[1:0]	R/W	J1 Message Lengt	h[1:0]:				
			These READ/WRITE bit-fields permit the user to specify the length of the J1 Trace Message, that the Receive STS-1 POH Processor block will receive. The relationship between the content of these bit-fields and the corresponding J1 Trace Message Length is presented below.					
			MSG LENGTH	Resulting J1 Trace Message Length				
		l	MSG LENGTH Resulting J1 Trace Message Length					

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

	01	16 Bytes	
	10/11	64 Bytes	

The product are no ordered (OBS)

The product are no be ordered (OBS)

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 374: Receive STS-1 Path - Pointer Value - Byte 1 (Address Location= 0xN1A6)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Unu	sed		Current_Po MSB		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 2	Unused	R/O	
1 – 0	Current_Pointer_Value_MSB[7:0]	R/O	Current Pointer Value – MSB:
			These READ-ONLY bit-fields, along with that from the "Receive STS-1 Path —Pointer Value — Byte 0" Register combine to reflect the current value of the pointer that the "Receive STS-1 POH Processor" block is using to locate the SPE within the incoming STS-1 data stream. Note: These register bits comprise the Upper Byte value of the Pointer Value.

Table 375: Receive STS-1 Path – Pointer Value – Byte 0 (Address Location= 0xN1A7)

Віт 7	Віт 6	Віт 5	Віт 4 9 Віт 3	Віт 2	Віт 1	Віт 0			
	Current_Pointer_Value_LSB[7:0]								
R/O	R/O	R/O	R/O R/O	R/O	R/O	R/O			
0	0	0	0 0	0	0	0			

BIT NUMBER	Name Name	TYPE	DESCRIPTION
7 – 0	Current_Pointer_Value_LSB[7:0]	R/O	Current Pointer Value – LSB:
	The progreet not		These READ-ONLY bit-fields, along with that from the "Receive STS-1 Path – Pointer Value – Byte 1" Register combine to reflect the current value of the pointer that the "Receive STS-1 POH Processor" block is using to locate the SPE within the incoming STS-1 data stream.
	o's and		Note: These register bits comprise the Lower Byte value of the Pointer Value.



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 376: Receive STS-1 Path – AUTO AIS Control Register (Address Location= 0xN1BB)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Transmit AIS-P (Down- stream) Upon C2 Byte Unstable	Transmit AIS-P (Down- stream) Upon UNEQ-P	Transmit AIS-P (Down- stream) Upon PLM- P	Transmit AIS-P (Down- stream) Upon J1 Message Unstable	Transmit AIS-P (Down- stream) upon TIM-P	Transmit AIS-P (Down- stream) upon LOP-P	Transmit AIS-P (Down- stream) Enable
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7	Unused	R/O	thi Ire
6	Transmit AIS-P	R/W	Transmit Path AIS upon Detection of Unstable C2 Byte:
	(Downstream) upon C2 Byte Unstable		This READ/WRITE bit-field permits the user to configure the Receive STS-1 POH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Transmit SONET POH Processor blocks), anytime it detects an Unstable C2 Byte condition in the "incoming" STS-1 data-stream.
			0 – Does not configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects an "Unstable C2 Byte" condition.
			1 - Configures the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects an "Unstable C2 Byte" condition.
		, ct of	Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
5	Transmit AIS-P (Downstream) upon UNEQ-P	R/W	Transmit Path AIS upon Detection of Path-Unequipped Defect (UNEQ-P):
	Transmit AIS-P (Downstream) upon UNEQ-P	dnay	This READ/WRITE bit-field permits the user to configure the Receive STS-1 POH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Transmit SONET POH Processor blocks), anytime it declares an UNEQ-P condition.
	'0		0 – Does not configure the Receive STS-1 POH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the UNEQ-P defect.
			1 – Configures the Receive STS-1 POH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the UNEQ-P defect.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
4	Transmit AIS-P (Downstream) upon PLM-P	R/W	Transmit Path AIS upon Detection of Path-Payload Label Mismatch Defect (PLM-P):
	I LIVI-F		This READ/WRITE bit-field permits the user to configure the Receive STS-1 POH Processor block to automatically transmit a Path AIS

		1	
			(AIS-P) Indicator via the "downstream" traffic (e.g., towards the Transmit SONET POH Processor blocks), anytime it declares an PLM-P condition.
			0 – Does not configure the Receive STS-1 POH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the PLM-P defect.
			1 – Configures the Receive STS-1 POH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the PLM-P defect.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
3	Transmit AIS-P	R/W	Transmit Path AIS upon Detection of Unstable 1 Message:
	(Downstream) upon J1 Message Unstable		This READ/WRITE bit-field permits the user to configure the Receive STS-1 POH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Transmit SONET POH Processor blocks), anytime it detects an Unstable J1 Message condition in the "incoming" STS-1 data-stream.
			0 – Does not configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects an "Unstable J1 Message" condition.
			1 – Configures the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects an "Unstable J1 Message" condition.
		orc	Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
2	Transmit AIS-P (Downstream) upon TIM-P	R/W	Transmit Path AIS upon Detection of Path-Trace Identification Message Mismatch Defect (TIM-P):
	aroduc.	etano	This READ/WRITE bit-field permits the user to configure the Receive STS-1 POH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Transmit SONET POH Processor blocks), anytime it declares a TIM-P condition.
	Thebatant	No.	0 – Does not configure the Receive STS-1 POH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the TIM-P defect.
	%		1 – Configures the Receive STS-1 POH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the TIM-P defect.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
1	Transmit AIS-P	R/W	Transmit Path AIS upon Detection of Loss of Pointer (LOP-P):
	(Downstream) upon LOP-P		This READ/WRITE bit-field permits the user to configure the Receive STS-1 POH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Transmit SONET POH Processor blocks), anytime it declares an LOP-P condition.
		<u> </u>	0 – Does not configure the Receive STS-1 POH Processor block to

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the LOP-P defect.
			1 – Configures the Receive STS-1 POH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the LOP-P defect.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
0	Transmit AIS-P (Downstream) Enable	R/W	Automatic Transmission of AIS-P Enable:
	(Downstream) Linable		This READ/WRITE bit-field serves two purposes.
			It permits the user to configure the Receive STS-1 POH Processor block to automatically transmit the Path AIS indicator, via the downstream traffic (e.g., towards the Transmit SONET POH Processor blocks), upon detection of an UNEQ P, PLM-P, LOP-P or LOS conditions.
			It also permits the user to configure the Receive STS-1 POH Processor block to automatically transmit a Path (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Transmit SONET POH Processor blocks) anytime it detects an AIS-P condition in the "incoming " STS-1 data-stream.
			0 - Configures the Receive STS-1 POH Processor block to NOT automatically transmit the AIS-P indicator (via the "downstream" traffic) upon detection of any of the "above-mentioned" conditions.
			1 – Configures the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) upon detection of any of the "above-mentioned" condition.
		्राठ	Note: The user must also set the corresponding bit-fields (within this register) to "1" in order to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator upon detection of a given a
	Thedata	id may	not be

Table 377: Receive STS-1 Path – SONET Receive Auto Alarm Register – Byte 0 (Address Location= 0xN1C3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Transmit AIS-P (via Downstream STS-1s) upon LOP-P	Transmit AIS-P (via Downstream STS-1s) upon PLM-P	Transmit AIS-P (via Downstream STS-1s) upon LCD-P	Transmit AIS-P (via Downstream STS-1s) upon UNEQ-P	Transmit AIS-P (via Downstream STS-1s) upon TIM-P	Transmit AIS-P (via Downstream STS-1s) upon AIS-P	Transmit DS3 AIS (via Downstream DS3) upon PDI-P
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Unused	R/O	"th" ure
6	Transmit AIS-P (via	R/W	Transmit AIS-P (via Downstream STS-1s) upon LOP-P
	Downstream STS-1s) upon LOP-P	40	This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the LOP-P defect. 0 — Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the LOP-P defect.
	ر الم	OIP	1 Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the LOP-P defect.
5	Transmit AIS-P (via		Transmit AIS-P (via Downstream STS-1s) upon PLM-P:
	Transmit AIS-P (via Downstream STS-1s) upon PLM-P	lay!	This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal, anytime the Receive STS-1 POH Processor block declares the PLM-P defect.
	ॐ		0 – Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the PLM-P defect.
			1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the PLM-P defect.
4	Transmit AIS-P (via	R/W	Transmit AIS-P (via Downstream STS-1s) upon LCD-P:
	Downstream STS-1s) upon LCD-P		This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal, anytime the Receive SONET POH

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			Processor block declares the LCD-P defect.
			0 – Does not configure the corresponding Transmit STS-1 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive SONET POH Processor block declares the LCD-P defect.
			1 – Configures the corresponding Transmit STS-1 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive SONET POH Processor block declares the LCD-P defect.
3	Transmit AIS-P (via	R/W	Transmit AIS-P (via Downstream STS-1s) upon UNEQ-P:
	Downstream STS-1s) upon UNEQ-P		This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal, (within the outbound STS-3 signal) anytime the Receive STS-1 POH Processor block declares the UNEQ-P defect.
			0 – Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the UNEQ-P defect.
			1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the UNEQ-P defect.
2	Transmit AIS-P (via Downstream STS-1s) upon TIM-P	R/W	Transmit AIS-P (via Downstream STS-1s) upon TIM-P: This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the TIM-P defect.
	ne prod	No. 1	O – Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the TIM-P defect.
	theata	di	1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the TIM-P defect.
1	Transmit AIS-P (via	R/W	Transmit AIS-P (via Downstream STS-1s) upon AIS-P:
	Downstream STS-1s) upon AIS-P		This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the AIS-P defect.
			0 – Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the AIS-P defect.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal A(within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the AIS-P defect.
0	Unused	R/O	

The product or products mentioned in this are no ordered (OBS)

EXAR Experience Our Connectivit

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 378: Receive STS-1 Path – Receive J1 Byte Capture Register (Address Location= 0xN1D3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
J1_Byte_Captured_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	J1_Byte_Captured_Value[7:0]	R/O	J1 Byte Captured Value[7:0]
			These READ-ONLY bit-fields contain the value of the J1 byte, within the most recently received STS-1 frame. This particular value is stored in this register for one STS-1 frame period. During the next STS-1 frame period, this value will be overridden with a new J1 byte value.

Table 379: Receive STS-1 Path – Receive B3 Byte Capture Register (Address Location= 0xN1D7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт	Віт 2	Віт 1	Віт 0	
B3_Byte_Captured_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	0	0	0	5 60 00	0	0	0	

BIT NUMBER	Name	TYPE	DESCRIPTION
7 – 0	B3_Byte_Captured_Value[7:0]	R/O	B3 Byte Captured Value[7:0]
	roduct (alot v	These READ-ONLY bit-fields contain the value of the B3 byte within the most recently received STS-1 frame. This particular value is stored in this register for one STS-frame period. During the next STS-1 frame period, this value will be overridden with a new B3 byte value.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 380: Receive STS-1 Path - Receive C2 Byte Capture Register (Address Location= 0xN1DB)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
C2_Byte_Captured_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	C2_Byte_Captured_Value[7:0]	R/O	C2 Byte Captured Value[7:0]
			These READ-ONLY bit-fields contain the value of the C2 byte, within the most recently received STS-1 frame. This particular value is stored in this register for one STS-1 frame period. During the next STS-1 frame period, this value will be overridden with a new C2 byte value.

Table 381: Receive STS-1 Path – Receive G1 Byte Capture Register (Address Location= 0xN1DF)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	G1_Byte_Captured_Value[7:0]									
R/O	R/O	R/O	R/O	Ø RØ	R/O	R/O	R/O			
0	0	0	0	0 0	0	0	0			

BIT NUMBER	Name	Туре	DESCRIPTION
7 – 0	G1_Byte_Captured_Value[7:0]	R/O	G1 Byte Captured Value[7:0]
	ote	0	These READ-ONLY bit-fields contain the value of the G1 byte, within the most recently received STS-1 frame.
	ductar	the	This particular value is stored in this register for one STS-1 frame period. During the next STS-1 frame period, this value will be overridden with a new G1 byte value.
	The proshed in a y n		

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 382: Receive STS-1 Path – Receive F2 Byte Capture Register (Address Location=0xN1E3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	F2_Byte_Captured_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	F2_Byte_Captured_Value[7:0]	R/O	F2 Byte Captured Value[7:0]
			These READ-ONLY bit-fields contain the value of the F2 byte, within the most recently received STS-1 frame. This particular value is stored in this register for one STS-1
			frame period. During the next STS-1 frame period, this value will be overridden with a new F2 byte value.

Table 383: Receive STS-1 Path – Receive H4 Byte Capture Register (Address Location= 0xN1E7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	H4_Byte_Captured_Value[7:0]									
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O			
0	0	0	0	3	0	0	0			

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	H4_Byte_Captured_Value[7:0]	R/O	H4 Byte Captured Value[7:0]
		N POC	These READ-ONLY bit-fields contain the value of the H4 byte, within the most recently received STS-1 frame.
	duct	SION I	This particular value is stored in this register for one STS-1 frame period. During the next STS-1 frame period, this value will be overridden with a new H4 byte value.
	The proshed	3100	

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 384: Receive STS-1 Path – Receive Z3 Byte Capture Register (Address Location= 0xN1EB)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	Z3_Byte_Captured_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Z3_Byte_Captured_Value[7:0]	R/O	Z3 Byte Captured Value[7:0]
			These READ-ONLY bit-fields contain the value of the Z3 byte, within the most recently received STS-1 frame.
			This particular value is stored in this register for one STS-1 frame period. During the next STS-1 frame period, this value will be overridden with a new Z3 byte value.

Table 385: Receive STS-1 Path – Receive Z4 (K3) Byte Capture Register (Address Location= 0xN1EF)

					/		
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Z	4(K3)_Byte_Cap	ptured_Value[7:	0]		
R/O	R/O	R/O	R/O 《	R/O	R/O	R/O	R/O
0	0	0	0	0,000	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Z4(K3)_Byte_Captured_Value[7:0]	R/O	Z4 (K3) Byte Captured Value[7:0]
	lor by	o jyo	These READ-ONLY bit-fields contain the value of the Z4 (K3) byte, within the most recently received STS-1 frame.
	oduct are	0 _©	This particular value is stored in this register for one STS-1 frame period. During the next STS-1 frame period, this value will be overridden with a new Z4 (K3) byte value.
	The plata she ay !		
	*		



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 386: Receive STS-1 Path – Receive Z5 Byte Capture Register (Address Location= 0xN1F3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	Z5_Byte_Captured_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Z5_Byte_Captured_Value[7:0]	R/O	Z5 Byte Captured Value[7:0]
			These READ-ONLY bit-fields contain the value of the Z5 byte, within the most recently received STS-1 frame.
			This particular value is stored in this register for one STS-1 frame period. During the next STS-1 frame period, this value will be overridden with a new Z5 byte value.
	The product of and many	aynot	frame period. During the next \$78-1 frame period, this value will be overridden with a new Z5 byte value.

1.10 TRANSMIT ATM CELL PROCESSOR BLOCK

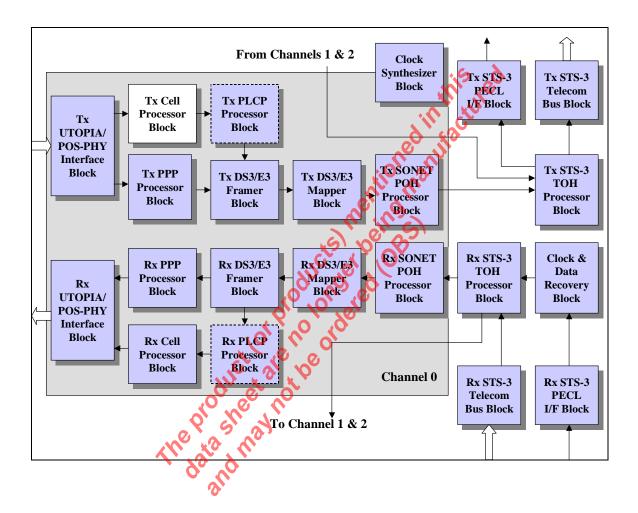
3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

The register map for the Transmit ATM Cell Processor Block is presented in the Table below. Additionally, a detailed description of each of the "Transmit ATM Cell Processor" block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33 device, with the "Transmit ATM Cell Processor Blocks "highlighted" is presented below in

Figure 9.

Figure 11: Illustration of the Functional Block Diagram of the XRT94L33 device, with the Transmit ATM Cell Processor Block "High-lighted".



XRT94L33

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS



1.10.1 TRANSMIT ATM CELL PROCESSOR BLOCK REGISTER

Table 387: Transmit ATM Cell Processor Block Register Address Map

	TRANSMIT ATM CELL PROCESSOR/ PPP PROCESSOR BLOCK REGISTERS	
Note: N repres	sents the "Channel Number" and ranges in value from 0x02 to 0x04	
0xNF00	Transmit ATM Cell Processor Control Register – Byte 3	0x00
0xNF01	Transmit ATM Cell Processor Control Register – Byte 2	0x00
0xNF02	Transmit ATM Cell Processor Control Register – Byte 1	0x00
0xNF03	Transmit ATM Cell/PPP Processor Control Register – Byte 0	0x00
0xNF04	Transmit ATM Status Register	0x00
0xNF05 – 0xNF0A	Reserved	0x00
0xNF0B	Transmit ATM Cell/PPP Processor Interrupt Status Register	0x00
0xNF0C – 0xNF0E	Reserved	0x00
0xNF0F	Transmit ATM Cell/PPP Processor Interrupt Enable Register	0x00
0xNF10 – 0xNF12	Reserved	0x00
0xNF13	Transmit ATM Cell Insertion/Extraction Memory Control Register	0x00
0xNF14	Transmit ATM Cell Insertion/Extraction Memory - Byte 3	0x00
0xNF15	Transmit ATM Cell Insertion/Extraction Memory – Byte 2	0x00
0xNF16	Transmit ATM Cell Insertion/Extraction Memory – Byte 1	0x00
0xNF17	Transmit ATM Cell Insertion/Extraction Memory – Byte 0	0x00
0xNF18	Transmit ATM Cell Idle Cell Header Byte # 1 Register	0x00
0xNF19	Transmit ATM Cell - Idle Cell Header Byte # 2 Register	0x00
0xNF1A	Transmit ATM Cell - Idle Cell Header Byte # 3 Register	0x00
0xNF1B	Transmit ATM Cell - Idle Cell Header Byte # 4 Register	0x00
0xNF1C – 0xNF1E	Reserved	0x00
0xNF1F	Transmit ATM Cell – Idle Cell Payload Byte Register	0x00
0xNF20	Transmit ATM Cell – Test Cell Header Byte # 1 Register	0x00
0xNF21	Transmit ATM Cell – Test Cell Header Byte # 2 Register	0x00
0xNF22	Transmit ATM Cell – Test Cell Header Byte # 3 Register	0x00
0xNF23	Transmit ATM Cell – Test Cell Header Byte # 4 Register	0x00
0xNF24 – 0xNF27	Reserved	0x00
0xNF28	Transmit ATM Cell – Cell Count Register – Byte 3	0x00

0xNF29	Transmit ATM Cell – Cell Count Register – Byte 2	0x00
0xNF2A	Transmit ATM Cell – Cell Count Register – Byte 1	0x00
0xNF2B	Transmit ATM Cell – Cell Count Register – Byte 0	0x00
0xNF2C	Transmit ATM Cell – Discard Cell Count Register – Byte 3	0x00
0xNF2D	Transmit ATM Cell – Discard Cell Count Register – Byte 2	0x00
0xNF2E	Transmit ATM Cell – Discard Cell Count Register – Byte 1	0x00
0xNF2F	Transmit ATM Cell – Discard Cell Count Register – Byte 0	0x00
0xNF30	Transmit ATM Cell – HEC Byte Error Count Register – Byte 3	0x00
0xNF31	Transmit ATM Cell – HEC Byte Error Count Register – Byte 2	0x00
0xNF32	Transmit ATM Cell – HEC Byte Error Count Register – Byte 1	0x00
0xNF33	Transmit ATM Cell – HEC Byte Error Count Register - Byte 0	0x00
0xNF34	Transmit ATM Cell – Parity Error Count Register - Byte 3	0x00
0xNF35	Transmit ATM Cell – Parity Error Count Register – Byte 2	0x00
0xNF36	Transmit ATM Cell – Parity Error Count Register – Byte 1	0x00
0xNF37	Transmit ATM Cell – Parity Error Count Register – Byte 0	0x00
0xNF38 – 0xNF42	Reserved	0x00
0xNF43	Transmit ATM Controller – Transmit ATM Filter # 0 Control Register	0x00
0xNF44	Transmit ATM Controller Fransmit ATM Filter # 0 Pattern – Header Byte 1	0x00
0xNF45	Transmit ATM Controller – Transmit ATM Filter # 0 Pattern – Header Byte 2	0x00
0xNF46	Transmit ATM Controller - Transmit ATM Filter # 0 Pattern - Header Byte 3	0x00
0xNF47	Transmit ATM Controller – Transmit ATM Filter # 0 Pattern – Header Byte 4	0x00
0xNF48	Transmit ATM Controller - Transmit ATM Filter # 0 Check - Header Byte 1	0x00
0xNF49	Transmit ATM Controller – Transmit ATM Filter # 0 Check – Header Byte 2	0x00
0xNF4A	Transmit ATM Controller – Transmit ATM Filter # 0 Check – Header Byte 3	0x00
0xNF4B	Transmit ATM Controller – Transmit ATM Filter # 0 Check – Header Byte 4	0x00
0xNF4C	Transmit ATM Cell – Cell Count Register – Byte 3	0x00
0xNF4D	Transmit ATM Cell – Cell Count Register – Byte 2	0x00
0xNF4E	Transmit ATM Cell – Cell Count Register – Byte 1	0x00
0xNF4F	Transmit ATM Cell – Cell Count Register – Byte 0	0x00
0xNF50 – 0xNF52	Reserved	0x00
0xNF53	Transmit ATM Controller – Transmit ATM Filter # 1 Control Register	0x00
0xNF54	Transmit ATM Controller – Transmit ATM Filter # 1 Pattern – Header Byte 1	0x00

XRT94L33

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS



Rev 2.0.0

0xNF55	Transmit ATM Controller – Transmit ATM Filter # 1 Pattern – Header Byte 2	0x00
0xNF56	Transmit ATM Controller – Transmit ATM Filter # 1 Pattern – Header Byte 3	0x00
0xNF57	Transmit ATM Controller – Transmit ATM Filter # 1 Pattern – Header Byte 4	0x00
0xNF58	Transmit ATM Controller – Transmit ATM Filter # 1 Check – Header Byte 1	0x00
0xNF59	Transmit ATM Controller – Transmit ATM Filter # 1 Check – Header Byte 2	0x00
0xNF5A	Transmit ATM Controller – Transmit ATM Filter # 1 Check – Header Byte 3	0x00
0xNF5B	Transmit ATM Controller – Transmit ATM Filter # 1 Check – Header Byte 4	0x00
0xNF5C	Transmit ATM Cell – Cell Count Register - Byte 3	0x00
0xNF5D	Transmit ATM Cell – Cell Count Register – Byte 2	0x00
0xNF5E	Transmit ATM Cell – Cell Count Register – Byte 1	0x00
0xNF5F	Transmit ATM Cell – Cell Count Register – Byte 0	0x00
0xNF60 – 0xNF62	Reserved	0x00
0xNF63	Transmit ATM Controller – Transmit ATM Filter # 2 Control Register	0x00
0xNF64	Transmit ATM Controller – Transmit ATM Filter # 2 Pattern – Header Byte 1	0x00
0xNF65	Transmit ATM Controller – Transmit ATM Filter # 2 Pattern – Header Byte 2	0x00
0xNF66	Transmit ATM Controller – Transmit ATM Filter # 2 Pattern – Header Byte 3	0x00
0xNF67	Transmit ATM Controller – Transmit ATM Filter # 2 Pattern – Header Byte 4	0x00
0xNF68	Transmit ATM Controller – Transmit ATM Filter # 2 Check – Header Byte 1	0x00
0xNF69	Transmit ATM Controller - Transmit ATM Filter # 2 Check - Header Byte 2	0x00
0xNF6A	Transmit ATM Controller - Transmit ATM Filter # 2 Check - Header Byte 3	0x00
0xNF6B	Transmit ATM Controller Transmit ATM Filter # 3 Check – Header Byte 4	0x00
0xNF6C	Transmit ATM Cell - Cell Count Register - Byte 3	0x00
0xNF6D	Transmit ATM Cell - Cell Count Register - Byte 2	0x00
0xNF6E	Transmit ATM cell - Cell Count Register - Byte 1	0x00
0xNF6F	Transmit ATM Cell Count Register – Byte 0	0x00
0xNF70 – 0xNF72	Reserved	0x00
0xNF73	Transmit ATM Controller – Transmit ATM Filter # 3 Control Register	0x00
0xNF74	Transmit ATM Controller – Transmit ATM Filter # 3 Pattern – Header Byte 1	0x00
0xNF75	Transmit ATM Controller – Transmit ATM Filter # 3 Pattern – Header Byte 2	0x00
0xNF76	Transmit ATM Controller – Transmit ATM Filter # 3 Pattern – Header Byte 3	0x00
0xNF77	Transmit ATM Controller – Transmit ATM Filter # 3 Pattern – Header Byte 4	0x00
0xNF78	Transmit ATM Controller – Transmit ATM Filter # 3 Check – Header Byte 1	0x00

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

0xNF79	Transmit ATM Controller – Transmit ATM Filter # 3 Check – Header Byte 2	0x00
0xNF7A	Transmit ATM Controller – Transmit ATM Filter # 3 Check – Header Byte 3	0x00
0xNF7B	Transmit ATM Controller – Transmit ATM Filter # 3 Check – Header Byte 4	0x00
0xNF7C	Transmit ATM Cell – Cell Count Register – Byte 3	0x00
0xNF7D	Transmit ATM Cell – Cell Count Register – Byte 2	0x00
0xNF7E	Transmit ATM Cell – Cell Count Register – Byte 1	0x00
0xNF7F	Transmit ATM Cell – Cell Count Register – Byte 0	0x00
0xNF80 – 0xN102	Reserved	0x00

The product are no products man to be ordered (OBS)

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS



Rev 2.0.0

1.10.2 TRANSMIT ATM CELL PROCESSOR BLOCK REGISTER DESCRIPTION

Table 388: Transmit ATM Cell Processor Block – Transmit ATM Control Register – Byte 3 (Address = 0xNF00)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused							

Table 389: Transmit ATM Cell Processor Block – Transmit ATM Control Register – Byte 2 (Address = 0xNF01)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт1	Віт 0		
			ni,	ctill	Transmit ATM Cell Processor Enable				
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W		
0	0	0	0	0	(0)	0	0		

BIT NUMBER	Name	TYPE	DESCRIPTION
7 - 1	Unused	R/O	meing
0	Transmit ATM Cell Processor Enable	R/W	Transmit ATM Cell Processor Block Enable: This READ/WRITE bit-field permits the user to either enable or disable the Transmit ATM Cell Processor block. If the user wishes to operate a given Channel in the ATM Mode, then he/she must enable the Transmit ATM Cell Processor Block. 0 – Disables the Transmit ATM Cell Processor Block 1. Enables the Transmit ATM Cell Processor Block Note: The user must set this bit-field to "1" before he/she begins to write ATM cell data into the Transmit UTOPIA Interface block.
	All day	ind n.	

Table 390: Transmit ATM Cell Processor Block – Transmit ATM Control Register – Byte 1 (Address = 0xNF02)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Test Cell Transmit Mode Enable	ONE SHOT MODE	GFC Insertion Enable - Bit 3	GFC Insertion Enable – Bit 2	GFC Insertion Enable – Bit 1	GFC Insertion Enable – Bit 0	COSET Polynomial Addition	Regenerate HEC Byte Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Test Cell Transmit Mode Enable	R/W	Test Cell Transmit Mode Enable: This READ/WRITE bit-field permits the user to enable the Test Cell Transmitter (within the Transmit ATM Cell Processor Block). The user must implement this configuration option in order to perform diagnostic operations with Test Cells: 0 – Disables the Test Cell Transmitter. 1 – Enables the Test Cell Transmitter. Notes: For normal operation, the user should set this bit-field to "1".
6	One Shot Mode	R/W	One Shot Mode: If the user has enabled the Test Cell Transmitter, then this READ/WRITE bit-field permits the user to either configure the Test Cell Transmitter into the "One-Shot" or in the "Continuous" Mode. If the user configures the Test Cell Transmitter into the "One-Shot" Mode, then (whenever the user implements a "0 to 1" transition within Bit Y [Test Cell Transmit Mode Enable] of this register) then the Test Cell Transmitter will generate and transmit 1024 test cells. Afterwards, the Test Cell Transmitter will halt its transmission of Test Cells until the user implements another "0 to 1 transition" within Bit 7 (Test Cell Transmit Mode Enable) within this register. If the user configures the Test Cell Transmitter into the "Continuous" Mode, then the Test Cell Transmitter will continuously generate and transmit test cells for the duration that Bit 7(Test Cell Transmit Mode Enable) is set to "1". 0 - Configures the Test Cell Transmitter to operate in the "Continuous" Mode. 1 - Configures the "Test Cell Transmitter" to operate in the "One-Shot" Mode.
5	GFC Insertion Enable – Bit 3	R/W	
4	GFC Insertion Enable – Bit 2	R/W	
3	GFC Insertion Enable – Bit 1	R/W	
2	GFC Insertion Enable – Bit 0	R/W	
1	COSET Polynomial Addition	R/W	COSET Polynomial Addition: This READ/WRITE bit-field permits the user to configure the Transmit ATM Cell Processor block to modulo-add the COSET Polynomial (e.g., x^6 + x^4 + x^2 + 1) to the HEC byte value, within each "outbound"

EXARExperience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			ATM cell.				
			0 - Configures the Transmit ATM Cell Processor block to NOT modulo-add the COSET Polynomial to the HEC byte within each outbound ATM cell.				
			1 - Configures the Transmit ATM Cell Processor block to modulo-add the COSET Polynomial to the HEC byte within each outbound ATM cell.				
0	Regenerate HEC	R/W	Regenerate HEC Byte Enable:				
	Byte Enable		This READ/WRITE bit-field permits the user to configure the Transmit ATM Cell Processor block to automatically re-compute and insert a new HEC byte into each ATM cell (that it receives from the Transmit UTOPIA Interface block) that contains an uncorrectable HEC byte.				
			0 - Does not configure the Transmit ATM Cell Processor block to compute and insert a new HEC byte into ATM cells that contains an "uncorrectable" HEC Byte error.				
			1 – Configures the Transmit ATM Cell Processor block to compute and insert a new HEC byte into ATM cells that contains an "uncorrectable" HEC Byte error.				
HEC Byte error. HEC Byte error.							

Table 391: Transmit ATM Cell Processor Block – Transmit ATM Control – Byte 0 (Address = 0xNF03)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
EC Byte Invert	HEC Byte Check Enable	Transmit UTOPIA Parity Check Enable	Transmit UTOPIA Parity Error – Discard	Transmit UTOPIA – ODD Parity	Reserved		Scrambler Enable
R/W	R/W	R/W	R/W	R/W	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	Description
7	HEC Byte Invert	R/W	HEC Byte Invert:
6	HEC Byte Check Enable	R/W	HEC Byte Check Enable. This READ/WRITE bit-field permits the user to configure the Transmit ATM Cell Processor block to perform HEC byte checking of all ATM cells that it receives via the Transmit UTOPIA Interface block. 0 — Configures the Transmit ATM Cell Processor block to NOT perform HEC byte checking on all ATM cells that it receives via the Transmit UTOPIA Interface block. 1 — Configures the Transmit ATM Cell Processor block to perform HEC byte checking on all ATM cells that it receives via the Transmit UTOPIA Interface block.
5	Transmit UTOPIA Parity Check Enable	R/W display	Transmit UTOPIA Parity Check Enable: This READ/WRITE bit-field permits the user to either enable or disable "Transmit UTOPIA Interface" Parity checking. If the user enables "Transmit UTOPIA Interface" Parity Checking, then the Transmit ATM Cell Processor block will compute either the EVEN or ODD parity value (depending upon the setting of Bit 3 within this register) of each byte or 16-bit word that is input via the Transmit UTOPIA Data Bus input pins: (TxUData[15:0]). Afterwards, the Transmit ATM Cell Processor block will compare this "locally computed" parity value with that which the ATM Layer Processor has provided to the "TxUPrty" input pin. If the Transmit ATM Cell Processor detects any discrepancies between these two parity values (e.g., any parity errors) then it will take action based upon the user's settings for Bit 4 (Transmit UTOPIA Parity Error – Discard). 0 – Disables "Transmit UTOPIA Interface" Parity Checking.
4	Transmit UTOPIA Parity Error - Discard	R/W	Transmit UTOPIA Parity Error – Discard Cell: This READ/WRITE bit-field permits the user to configure the Transmit ATM Cell Processor block to either discard or retain (for further processing) any ATM cell that contains a "Transmit UTOPIA Interface" parity error. 0 – Configures the Transmit ATM Cell Processor block to retain (for further processing) all cells that contain "Transmit UTOPIA Interface" parity errors. 1 – Configures the Transmit ATM Cell Processor block to discard all cells that contain "Transmit UTOPIA Interface" parity errors.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			Notes: This bit-field is only valid if "Transmit UTOPIA Interface" Parity Checking has been enabled.			
3	Transmit UTOPIA – Odd	R/W	Transmit UTOPIA Parity Value – ODD Parity:			
	Parity		This READ/WRITE bit-field permits the user to configure the Transmit ATM Cell Processor block to compute either the EVEN or ODD parity value for each byte or 16-bit word within each cell that it processes. Each of these parity values will ultimately be compared with the value that is input via the "TxUPrty" input pin (on the Transmit UTOPIA Interface block) coincident to when ATM cell data is being applied to the "TxUData[15:0]" input pins.			
			0 – Configures the Transmit ATM Cell Processor block to compute and verify the EVEN Parity value of each byte (or 16-bit word) of ATM cell data that it processes.			
			1 – Configures the Transmit ATM Cell Processor block to compute and verify the ODD Parity value of each byte (or 16-bit word) of ATM cell data that it processes.			
			Notes: This bit-field is only value if "Transmit UTOPIA Interface" Parity Checking has been enabled.			
2 - 1	Reserved	R/O	ane nul			
0	Scrambler Enable	70	Cell Payload Scrambler Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Cell Payload Scrambler". If the user enables the "Cell Payload Scrambler" then the Transmit ATM Cell Processor will payload self-synchronous scrambling on all cell payloads bytes (within each outbound ATM cell) with the x^43+1 polynomial. O-Disables the Cell Payload Scrambler I - Enables the Cell Payload Scrambler			
	(Within each outgoing ATM cell) with the X*43+1 polynomial. 0 Disables the Cell Payload Scrambler 1 - Enables the Cell Payload Scrambler					

Table 392: Transmit ATM Cell Processor Block – Transmit ATM Status Register (Address = 0xNF04)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused						
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION		
7 - 1	Unused	R/O			
0	One Shot DONE	R/O	One Shot DONE:		
			This READ-ONLY bit-field indicates whether or not the Test Cell Transmitter has completed its transmission of 1024 test cells, following the instant that the user has commanded the Test Cell to transmit this burst of 1024 cells.		
			0 - Indicates that the Test Cell Transmitter has NOT completed its transmission of 1024 test cells		
			1 – Indicates that the Test Cell Transmitter has completed its transmission of 1024 test cells since the last "Transmit Test Cell – One Shot" command.		
			Notes:		
			 This bit-field is only valid if (1) the Test Cell Transmitter is active and (2) if the Test Cell Transmitter has been configured to operate in the "One-Shot" Mode. Once this bit-field has been set to "1", it will remain at "1" until the user executes another "Transmit Test Cell – One Shot" command. 		
2. Once this bit-field has been set to "1", it will remain at "1" until the user executes another "Transmit Test Cell – One Shot" command.					

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 393: Transmit ATM Cell Processor Block – Transmit ATM Interrupt Status Register (Address = 0xNF0B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unu	Unused Transmit Cell Cell Insertion Extraction Interrupt Status Transmit Cell Insertion Cell Extraction Memory Overflow Interrupt Status		Transmit Cell Insertion Memory Overflow Interrupt Status	Detection of HEC Byte Error Interrupt Status	Detection of Transmit UTOPIA Parity Error Interrupt Status		
R/O	R/O	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	Description
7 - 6	Unused	R/O	All Jie
5	Transmit Cell	RUR	Transmit Cell Extraction Interrupt Status:
	Extraction Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Transmit Cell Extraction" interrupt has occurred since the last read of this register.
			The Transmit ATM Cell Processor block will generate the "Transmit Cell Extraction" Interrupt anytime it receives an incoming ATM cell (from the TxFIFO) and loads an ATM cell into the "Extraction Memory" Buffer.
			0 - Indicates that the "Transmit Cell Extraction" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Transmit Cell Extraction" Interrupt has occurred since the last read of this register.
4		RUR	Transmit Cell Insertion Interrupt
	Insertion Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Transmit Cell Insertion" interrupt has occurred since the last read of this register.
	The production of the producti	duce	The Transmit ATM Cell Processor block will generate the "Transmit Cell Insertion" Interrupt anytime a cell (residing in the Transmit Cell Insertion Buffer) is read out of the "Transmit Cell Insertion Buffer" and is loaded into the outbound ATM cell traffic.
		o Mi	0 – Indicates that the "Transmit Cell Insertion" Interrupt has NOT occurred since the last read of this register.
		and	1 – Indicates that the "Transmit Cell Insertion" Interrupt has occurred since the last read of this register.
3	Transmit Cell	RUR	Transmit Cell Extraction Memory Overflow Interrupt Status:
	Extraction Memory Overflow Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Transmit Cell Extraction Memory Overflow" Interrupt has occurred since the last read of this register.
		The Transmit ATM Cell Processor block will generate this interrupt anytime an overflow event has occurred in the "Transmit Cell Extraction Memory" Buffer.	
			0 – Indicates that the Transmit ATM Cell Processor block has NOT declared the "Transmit Cell Extraction Memory Overflow" Interrupt since the last read of this register.
			1 – Indicates that the Transmit ATM Cell Processor block has declared the "Transmit Cell Extraction Memory Overflow" interrupt since the last

RS

|--|

			read of this register.	
2	2 Transmit Cell RL Insertion Memory Overflow Interrupt Status	RUR	Transmit Cell Insertion Memory Overflow Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the Transmit Cell Insertion Memory Overflow" Interrupt has occurred since the last read of this register.	
			The Transmit ATM Cell Processor block will generate this interrupt anytime an overflow event has occurred in the "Transmit Cell Insertion Memory" Buffer.	
			0 – Indicates that the Transmit ATM Cell Processor block has NOT declared the "Transmit Cell Insertion Memory Overflow" interrupt since the last read of this register.	
			1 – Indicates that the Transmit ATM Cell Processor block has declared the "Transmit Cell Insertion Memory Overflow" interrupt since the last read of this register.	
1	Detection of HEC	RUR	Detection of HEC Byte Error Interrupt:	
	Byte Error Interrupt		This RESET-upon-READ bit-field indicates whether or not the "Transmit ATM Cell Processor block" has declared the "Detection of HEC Byte Error" Interrupt since the last read of this register.	
			The Transmit ATM Cell Processor block will generate this interrupt anytime it has received an ATM cell (from the TxFIFO) that contains a HEC byte error.	
			0 - Indicates that the Transmit ATM Cell Processor block has NOT declared the "Detection of HEC Byte Error" Interrupt since the last read of this register.	
			1 - Indicates that the Transmit ATM Cell Processor block has declared the "Detection of HEC Byte Error" Interrupt since the last read of this register.	
0	Detection of Transmit	1	Detection of Transmit UTOPIA Parity Error Interrupt:	
	producet.	odifection	il of	This RESET-upon-READ bit-field indicates whether or not the "Transmit ATM Cell Processor" block has declared the "Detection of Transmit UTOPIA Parity Error" Interrupt since the last read of this register.
			The Transmit ATM Cell Processor block will generate this interrupt anytime it has received an ATM cell byte or 16-bit word (from the Transmit UTOPIA Interface block) that contains a parity error.	
	Thedata		0 – Indicates that the Transmit ATM Cell Processor block has NOT declared the "Detection of Transmit UTOPIA Parity Error" Interrupt since the last read of this register.	
	8		1 – Indicates that the Transmit ATM Cell Processor block has declared the "Detection of Transmit UTOPIA Parity Error" Interrupt since the last read of this register.	



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 394: Transmit ATM Cell Processor Block – Transmit ATM Interrupt Enable Register (Address = 0xNF0F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unu	ised	Transmit Cell Extraction Interrupt Enable	Transmit Cell Insertion Interrupt Enable	Transmit Cell Extraction Memory Overflow Interrupt Enable	Transmit Cell Insertion Memory Overflow Interrupt Enable	Detection of HEC Byte Error Interrupt Enable	Detection of Transmit UTOPIA Parity Error Interrupt Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 6	Unused		Att ruite
5	Transmit Cell	R/W	Transmit Cell Extraction Interrupt Enable:
	Extraction Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Transmit Cell Extraction" Interrupt.
			If the user enables this feature, then the Transmit ATM Cell Processor block will generate the "Transmit Cell Extraction" Interrupt anytime it receives an incoming ATM cell (from the TxFIFO) and loads this ATM cell into the "Transmit Extraction Memory" Buffer.
			0 – Disables the Transmit Cell Extraction" Interrupt.
			1 – Enables the "Transmit Cell Extraction" Interrupt
4	Transmit Cell	R/W	Transmit Cell Insertion Interrupt Enable:
	Insertion Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Transmit Cell Insertion" Interrupt.
		,odi	If the user enables this feature, then the Transmit ATM Cell Processor block will generate the "Transmit Cell Insertion" Interrupt anytime a cell (residing in the "Transmit Cell Insertion" Buffer) is read out of the "Transmit Cell Insertion" Buffer and is loaded into the "outbound" ATM cell traffic.
		01 3	0 – Disables the Transmit Cell Insertion Interrupt.
		O NO	1 Enables the Transmit Cell Insertion Interrupt.
3	Transmit Cell	R/W	Transmit Cell Extraction Memory Overflow Interrupt Enable:
	Extraction Memory Overflow	3/1	This READ/WRITE bit-field permits the user to either enable or disable the "Transmit Cell Extraction Memory Overflow" Interrupt.
	Interrupt Enable		If the user enables this interrupt, then the Transmit ATM Cell Processor block will generate an interrupt any time an overflow event has occurred in the "Transmit Cell Extraction Memory" buffer.
			0 – Disables the Transmit Cell Extraction Memory Overflow Interrupt.
			1 – Enables the Transmit Cell Extraction Memory Overflow Interrupt.
2	Transmit Cell	R/W	Transmit Cell Insertion Memory Overflow Interrupt Enable:
	Insertion Memory Overflow		This READ/WRITE bit-field permits the user to either enable or disable the "Transmit Cell Insertion Memory Overflow" Interrupt.
	Interrupt Enable		If the user enables this interrupt, then the Transmit ATM Cell Processor block will generate an interrupt any time an overflow event has occurred in the "Transmit Cell Insertion Memory" buffer.

			0 – Disables the Transmit Cell Insertion Memory Overflow Interrupt.					
			1 – Enables the Transmit Cell Insertion Memory Overflow Interrupt.					
			1 – Enables the Transmit Cell Insertion Memory Overflow Interrupt.					
1	Detection of HEC Byte Error	R/W	Detection of HEC Byte Error Interrupt Enable:					
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of HEC Byte Error Interrupt" within the Transmit ATM Cell Processor Block.					
		If the user enables this interrupt, then the Transmit ATM Cell Processor block will generate an interrupt each time it receives an ATM cell (from the TxFIFO) that contains a HEC Byte error.						
		0 – Disables the "Detection of HEC Byte Error" Interrupt.						
			1 – Enables the "Detection of HEC Byte Error" Interrupt					
0	Detection of		Detection of Transmit UTOPIA Parity Error Interrupt Enable:					
	Transmit UTOPIA Parity Error Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Transmit UTOPIA Parity Error" Interrupt within the Transmit ATM Cell Processor block.					
			If the user enables this interrupt, then the Transmit ATM Cell Processor block will generate an interrupt each time it receives an ATM cell byte or 16-bi word (from the TxFIFO) that contains a parity error.					
			0 – Disables the "Detection of Transmit UTOPIA Parity Error" Interrupt.					
			1 – Enables the "Detection of Transmit UTOPIA Parity Error" Interrupt.					
	theda	andm	0 – Disables the "Detection of Transmit UTOPIA Parity Error" Interrupt. 1 – Enables the "Detection of Transmit UTOPIA Parity Error" Interrupt.					

sperience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 395: Transmit ATM Cell Processor Block – Transmit ATM Cell Insertion/Extraction Memory Control Register (0xNF13)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		Transmit Cell Extraction Memory RESET*	Transmit Cell Extraction Memory CLAV	Transmit Cell Insertion Memory RESET*	Transmit Cell Insertion Memory ROOM	Transmit Cell Insertion Memory WSOC
R/O	R/O	R/O	R/W	R/O	R/W	R/O	W/O
0	0	0	1	0	1	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7-5	Unused		
4	Transmit Cell Extraction	R/W	Transmit Cell Extraction Memory RESET*:
	Memory RESET*		This READ/WRITE bit-field permits the user to perform a REST operation to the Transmit Cell Extraction Memory.
			If the user writes a "1-to-0 transition" into this bit-field, then the following events will occur.
			All of the contents of the Transmit Cell Extraction Memory will be flushed.
			All READ and WRITE pointers will be reset to their default positions.
			Notes: Following this RESET event, the user must write the value "1" into this bit-field in order to enable normal operation within the Transmit Cell Extraction Memory.
3	Transmit Cell Extraction	R/O	Transmit Cell Extraction Memory – Cell Available Indicator:
	Memory CLAV	ct of	This READ-ONLY bit-field indicates whether or not there is at least ATM cell of data (residing within the Transmit Cell Extraction Memory) that needs to be read out via the Microprocessor Interface.
		ee' (0 - Indicates that the Transmit Cell Extraction Memory is empty and contains no ATM cell data.
	100 x 80	ind may.	1 – Indicates that the Transmit Cell Extraction Memory contains at least one ATM cell of data that needs to be read out.
	Thata		Notes: The user should validate each ATM cell that is being read out from the Transmit Cell Extraction memory by checking the state of this bit-field prior to reading out the contents of ATM cell data residing within the Transmit Cell Extraction Memory
2	Transmit Cell Insertion	R/W	Transmit Cell Insertion Memory RESET*:
	Memory RESET*		This READ/WRITE bit-field permits the user to perform a RESET operation to the Transmit Cell Insertion Memory.
			If the user writes a "1-to-0 transition" into this bit-field, then the following events will occur.
			All of the contents of the Transmit Cell Insertion Memory will be flushed.
			All READ and WRITE pointers will be reset to their default positions.
			Notes: Following this RESET event, the user must write the value "1" into this bit-field in order to enable normal

			operation of the Transmit Cell Insertion Memory.
1	Transmit Cell Insertion	R/O	Transmit Cell Insertion Memory – ROOM Indicator:
	Memory ROOM		This READ-ONLY bit-field indicates whether or not there is room (e.g., empty space) available for the contents of another ATM cell to be written into the Transmit Cell Insertion Memory.
			0 – Indicates that the Transmit Cell Insertion Memory does not contain enough empty space to receive another ATM cell via the Microprocessor Interface.
			1 – Indicates that the Transmit Cell Insertion Memory does contain enough empty space to receive another ATM cell via the Microprocessor Interface.
			Notes: The user should verify that the Transmit Cell Insertion Memory has sufficient empty space to accept another ATM cell of data (via the Microprocessor Interface) by polling the state of this bit-field prior to writing each cell into the Transmit Cell Insertion Memory.
0	Transmit Cell Insertion	W/O	Transmit Cell Insertion Memory – Write SOC (Start of Cell):
	Memory WSOC	3	Whenever the user is writing the contents of an ATM cell into the Transmit Cell Insertion Memory, then he/she is suppose to identify/designate the very first byte of this ATM cell by setting this bit-field to "1". Whenever the user does this, then the Transmit Cell Insertion Memory will "know" that the next octet that is written into the "Transmit ATM Cell Processor Block — Transmit Cell Insertion/Extraction Memory Data Register — Byte 3 (Address = 0xNF14) is designated as the first byte of the ATM cell currently being written into the Transmit Cell Insertion Memory.
		, oroc	This bit-field must be set to "0" during all other WRITE operations to the Transmit ATM Cell Processor – Transmit Cell Insertion/Extraction Memory Data Register
	The product of the pr	are the	Se of C



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 396: Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory Data – Byte 3 (Address = 0xNF14)

Віт 7	Віт 6	Віт 5	Віт 5 Віт 4		Віт 2	Віт 1	Віт 0	
	Transmit Cell Insertion/Extraction Memory Data[31:24]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	Transmit Cell	R/W	Transmit Cell Insertion/Extraction Memory Data[31:24]:
	Insertion/Extraction Memory Data[31:24]		These READ/WRITE bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory Data – Bytes 2 through 0" support the following functions. • They function as the address location for the user to write the
			contents of an "outbound" ATM cell into the Transmit Cell Insertion Memory, via the Microprocessor Interface.
			They function as the address location, for which the user to read out the contents of an "inbound" ATM cell from the Receive Cell Extraction Memory, via the Microprocessor Interface.
			Notes:
			1. If the user performs a WRITE operation to this (and the other three address locations), then he/she is writing ATM cell data into the Transmit Cell Insertion Memory.
			2. If the user performs a READ operation to this (and the other three address locations), then he/she is reading ATM cell data from the Transmit Cell Extraction Memory.
	N	char	3. READ and WRITE operations must be performed in a "32-bit" (4-byte "word") manner. Hence, whenever the user performs a READ/WRITE operation to these address locations, he/she must start by writing in or reading out the first byte (of this "4-byte" word) of a given ATM cell, into/from this performance.
	The production of the data and	may	Next, the user must perform the READ/WRITE operation (with the second of this "4-byte" word) to the "Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory – Byte 2 register. Afterwards, the user must perform a READ/WRITE operation (with the third of this "4-byte" word) to the Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory –
	o and		Byte 1 register. Finally, the user must perform a READ/WRITE operation (with the fourth of this "4-byte" word) to the Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory – Byte 0 register. When reading out (writing in) the next four bytes of a given ATM Cell, the user must repeat this process with a READ or WRITE operation, from/to this register location, and so on.
			4. Whenever the user is writing cell data into the Transmit Cell Insertion Memory, the size of the Cell is always 56 bytes.
			5. Whenever the user is reading cell data from the Transmit Cell Extraction Memory, the size of the Cell is always 56 bytes.

Table 397: Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory Data – Byte 2 (Address = 0xNF15)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit Cell Insertion/Extraction Memory Data[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	Transmit Cell	R/W	Transmit Cell Insertion/Extraction Memory Data[23:16]:
	Insertion/Extraction Memory Data[23:16]		These READ/WRITE bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory Data – Bytes 3, 1 and 6" support the following functions.
			They function as the address location for the user to write the contents of an "outbound" ATM cell into the Transmit Cell Insertion Memory, via the Microprocessor Interface.
			They function as the address location, for which the user to read out the contents of an "inbound" ATM cell from the Receive Cell Extraction Memory, via the Microprocessor Interface.
			Notes:
			If the user performs a WRITE operation to this (and the other three address locations), then he/she is writing ATM cell data into the Transmit Cell Insertion Memory.
The product of the pr		di	2. If the user performs a READ operation to this (and the other three address locations), then he/she is reading ATM cell data from the Transmit Cell Extraction Memory.
	NOT DE	3. READ and WRITE operations must be performed in a "32-bit" (4-byte "word") manner. Hence, whenever the user performs a READ/WRITE operation to these address locations, he/she must start by writing in or reading out the first byte (of this "4-byte" word) of a given ATM cell, into/from the Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory – Byte 3" register. Next, the user must perform the READ/WRITE operation (with the second of this "4-byte" word) to this particular address location. Afterwards, the user must perform a READ/WRITE operation (with the third of this "4-byte" word) to the Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory – Byte 1 register. Finally, the user must perform a READ/WRITE operation (with the fourth of this "4-byte" word) to the Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory – Byte 1 register. Finally, the user	
	'0		"4-byte" word) to the Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory – Byte 0 register. When reading out (writing in) the next four bytes of a given ATM Cell, the user must repeat this process with a READ or WRITE operation, from/to this register location, and so on.
			4. Whenever the user is writing cell data into the Transmit Cell Insertion Memory, the size of the Cell is always 56 bytes.
			5. Whenever the user is reading cell data from the Transmit Cell Extraction Memory, the size of the Cell is always 56 bytes.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 398: Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory Data – Byte 1 (Address = 0xNF16)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit Cell Insertion/Extraction Memory Data[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	Transmit Cell	R/W	Transmit Cell Insertion/Extraction Memory Data[15:8]:
	Transmit Cell Insertion/Extraction Memory Data[15:8]	R/W	Transmit Cell Insertion/Extraction Memory Data[15:8]: These READ/WRITE bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory Data – Bytes 3, 2 and 0" support the following functions. They function as the address location for the user to write the contents of an "outbound" ATM cell into the Transmit Cell Insertion Memory, via the Microprocessor Interface. They function as the address location, for which the user to read out the contents of an "inbound" ATM cell from the Receive Cell Extraction Memory, via the Microprocessor Interface. Notes: I. If the user performs a WRITE operation to this (and the other three address locations), then he/she is writing ATM cell data into the Transmit Cell Insertion Memory. If the user performs a READ operation to this (and the other three address locations), then he/she is reading ATM cell data
	The product	et no	 (writing in) the next four bytes of a given ATM Cell, the user must repeat this process with a READ or WRITE operation, from/to this register location, and so on. 4. Whenever the user is writing cell data into the Transmit Cell Insertion Memory, the size of the Cell is always 56 bytes.
			5. Whenever the user is reading cell data from the Transmit Cell Extraction Memory, the size of the Cell is always 56 bytes.

Table 399: Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory Data – Byte 0 (Address = 0xNF17)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit Cell Insertion/Extraction Memory Data[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
BIT NUMBER 7 - 0	NAME Transmit Cell Insertion/Extraction Memory Data[7:0]	TYPE R/W	Transmit Cell Insertion/Extraction Memory Data[7:0]: These READ/WRITE bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit Cell Insertion/Extraction Memory Data – Bytes 3, through 1" support the following functions. They function as the address location for the user to write the contents of an "outbound" ATM cell into the Transmit Cell Insertion Memory, via the Microprocessor Interface. They function as the address location, for which the user to read out the contents of an "inbound" ATM cell from the Receive Cell Extraction Memory, via the Microprocessor Interface. Notes: 1. If the user performs a WRITE operation to this (and the other three address locations), then he/she is writing ATM cell data into the Transmit Cell Insertion Memory.
	The product	or production of the productio	2. If the user performs a READ operation to this (and the other three addless locations), then he/she is reading ATM cell data from the Transmit Cell Extraction Memory. 3. READ and WRITE operations must be performed in a "32-bit" (4-byte "word") manner. Hence, whenever the user performs a READ/WRITE operation to these address locations, he/she must start by writing in or reading out the first byte (of this "4-byte" word) of a given ATM cell, into/from the Transmit ATM Cell Processor Block — Transmit Cell Insertion/Extraction Memory — Byte 3 register. Next, the user must perform the READ/WRITE operation (with the second of this "4-byte" word) to the "Transmit ATM Cell Processor Block — Transmit Cell Insertion/Extraction Memory — Byte 2 register. Afterwards, the user must perform a READ/WRITE operation (with the third of this "4-byte" word) to the "Transmit ATM Cell Processor Block — Transmit Cell Insertion/Extraction Memory — Byte 1" register. Finally, the user must perform a READ/WRITE operation (with the fourth of this "4-byte" word) to this particular register location. When reading out (writing in) the next four bytes of a given ATM Cell, the user must repeat this process with a READ or WRITE operation, from/to this register location, and so on.
			4. Whenever the user is writing cell data into the Transmit Cell Insertion Memory, the size of the Cell is always 56 bytes. 5. Whenever the user is reading cell data from the Transmit Cell
			Extraction Memory, the size of the Cell is always 56 bytes.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 400: Transmit ATM Cell Processor Block – Transmit ATM Idle Cell Header Byte 1 (Address = 0xNF18)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit Idle Cell Header Byte 1 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit Idle Cell	R/W	Transmit Idle Cell Header Byte – 1[7:0]:
	Header Byte – 1 [7:0]		These READ/WRITE register bits, along with that in "Transmit ATM Cell Processor Block – Transmit ATM Idle Cell Header Byte 2 through Byte 4" registers permit the user to define the header byte pattern of all Idle Cells that are generated by the Transmit ATM Cell Processor block. This register permits the user to define/specify the value of Header Byte # 1 within each Idle Cell that is generated and transmitted by the Transmit ATM Cell Processor block.

Table 401: Transmit ATM Cell Processor Block – Transmit ATM Idle Cell Header Byte 2 (Address = 0xNF19)

Віт 7	Віт 6	Віт 5	Bit 4 Bit 3	Віт 2	Віт 1	Віт 0	
Transmit Idle Cell Header Byte 2 [7:0]							
R/W	R/W	R/W	R/W R/W	R/W	R/W	R/W	
0	0	0	90	0	0	0	

BIT NUMBER	NAME	TYPE	1,00	DESCRIPTION
7 – 0	Transmit Idle Cell Header Byte – 2 [7:0]	RAV	These REACell Proces 4" registers Cells that a This registe Byte # 2 wi	AD/WRITE register bits, along with that in "Transmit ATM asor Block – Transmit ATM Idle Cell Header Bytes 1, 3 and permit the user to define the header byte pattern of all Idle re generated by the Transmit ATM Cell Processor block. Ber permits the user to define/specify the value of Header thin each Idle Cell that is generated and transmitted by the TM Cell Processor block.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 402: Transmit ATM Cell Processor Block – Transmit ATM Idle Cell Header Byte 3 (Address = 0xNF1A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit Idle Cell Header Byte 3 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit Idle Cell Header Byte – 3 [7:0]	R/W	Transmit Idle Cell Header Byte – 3[7:0]: These READ/WRITE register bits, along with that in "Transmit ATM Cell Processor Block – Transmit ATM Idle Cell Header Bytes 1, 2 and 4" registers permit the user to define the header byte pattern of all Idle Cells that are generated by the Transmit ATM Cell Processor block.
			This register permits the user to define/specify the value of Header Byte # 3 within each Idle Cell that is generated and transmitted by the Transmit ATM Cell Processor block.

Table 403: Transmit ATM Cell Processor Block – Transmit ATM Idle Cell Header Byte 4 (Address = 0xNF1B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit Idle Cell Header Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	99, 9	0	0	0	0	

BIT NUMBER	Name	TYPE	DESCRIPTION
7 – 0	Transmit Idle Cell Header Byte – 4 [7:0]	RW SOLD TO THE SOL	Transmit Idle Cell Header Byte – 4[7:0]: These READ/WRITE register bits, along with that in "Transmit ATM Cell Processor Block – Transmit ATM Idle Cell Header Byte 1 through Byte 3" registers permit the user to define the header byte pattern of all Idle Cells that are generated by the Transmit ATM Cell Processor block. This register permits the user to define/specify the value of Header Byte # 4 within each Idle Cell that is generated and transmitted by the Transmit ATM Cell Processor block.
	•		

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 404: Transmit ATM Cell Processor Block – Transmit ATM Idle Cell Payload Register (Address = 0xNF1F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit Idle Cell Payload Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION			
7 - 0	Transmit Idle Cell Payload Byte[7:0]	R/W	Transmit Idle Cell Payload Byte [7:0]:			
	r ayloud Byto[r.o]		These READ/WRITE register bits permit the user to define the value of the payload bytes of all Idle Cells that are generated and transmitted by the Transmit ATM Cell Processor block.			
			Notes: Each of the 48 payload bytes (within each outbound Idle Cell) will be assigned the value that is written into this register.			

Table 405: Transmit ATM Cell Processor Block – Transmit Test Cell Header Byte – Byte 1 (Address = 0xNF20)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit Test Cell Header					[7:0]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0 🏄	3, 9	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Transmit Test Cell Header Byte	R/W	Receive Test Cell Header Byte 1:
	1[7:0]	le he	These READ/WRITE register bits along with that in the Transmit ATM Cell Processor Block – Transmit Cell Header Byte – Bytes 2 through 4" permit the user to define the headers of test cells that the Transmit Test Cell Generator will generate.
	opishe a	C.	This particular register byte permits the user to define the contents of Header Byte # 1.
	The data dinic		Notes: These register bits are only active if the Transmit Test Cell Generator has been enabled.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 406: Transmit ATM Cell Processor Block – Transmit Test Cell Header Byte – Byte 2 (Address = 0xNF21)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit Test Cell Header Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit Test Cell Header Byte 2[7:0]	R/W	Receive Test Cell Header Byte 2: These READ/WRITE register bits along with that in the "Transmit ATM Cell Processor Block – Transmit Cell Header Byte – Bytes 1, 3 and 4" permit the user to define the headers of test cells that the Transmit Test Cell Generator will generate. This particular register byte permits the user to define the contents of Header Byte # 2. Notes: These register bits are only active if the Transmit Test Cell Generator has been enabled.

Table 407: Transmit ATM Cell Processor Block – Transmit Test Cell Header Byte – Byte 3 (Address = 0xNF22)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit Test Cell Header Byte 3 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0, 9, %	0	0	0	0	
	101 100 ALD							

BIT NUMBER	Name Name	TYPE	DESCRIPTION
7 – 0	Transmit Test Cell Header Byte 3[7:0]	R/W	Receive Test Cell Header Byte 3: These READ/WRITE register bits along with that in the "Transmit ATM Cell Processor Block – Transmit Cell Header Byte – Bytes 1, 2 and 4" permit the user to define the headers of test cells that the Transmit Test Cell Generator will generate. This particular register byte permits the user to define the contents of Header Byte # 3. Notes: These register bits are only active if the Transmit Test Cell Generator has been enabled.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 408: Transmit ATM Cell Processor Block – Transmit Test Cell Header Byte – Byte 4 (Address = 0xNF23)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit Test Cell Header Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit Test Cell	R/W	Receive Test Cell Header Byte 4:
	Header Byte 4[7:0]		These READ/WRITE register bits along with that in the "Transmit ATM Cell Processor Block – Transmit Cell Header Byte – Bytes 1 through 3" permit the user to define the headers of test cells that the Transmit Test Cell Generator will generate. This particular register byte permits the user to define the contents of Header Byte # 4. Notes: These register bits are only active if the Transmit Test Cell Generator has been enabled.

Table 409: Transmit ATM Cell Processor Block – Transmit ATM Cell Counter (Address = 0xNF28)

Віт 7	Віт 6	Віт 5	Віт 4	Віт.3	Віт 2	Віт 1	Віт 0
		-	Transmit ATM 🤇	ell Count[31:24]		
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0.0	9 0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit ATM Cell Count[31:24]	RUR	Transmit ATM Cell Count – Byte 3[31:24]: This RESET-upon-READ register, along with the "Transmit ATM Cell Count – Bytes 2 through 0" registers; contain a 32-bit value for the number of User/Valid cells that have been transmitted by the Transmit ATM Cell Processor block. This particular register contains the MSB (Most Significant Byte) value for this 32-bit expression. Notes: 1. The contents within these registers include all of the following: All ATM cells that have been read out from the TxFIFO, or the Transmit Cell Insertion Buffer. 2. The contents of these registers do not include the number of Idle Cells that have been generated by the Transmit ATM Cell Processor block. 3. If the number of Cells reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x000000000").

Table 410: Transmit ATM Cell Processor Block – Transmit ATM Cell Counter (Address = 0xNF29)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit ATM Cell Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	Transmit ATM Cell	RUR	Transmit ATM Cell Count – Byte 2[23:16]:
	Count[23:16]		This RESET-upon-READ register, along with the "Transmit ATM Cell Count – Bytes 3, 1 and 0" registers; contain a 32-bit value for the number of User/Valid cells that have been transmitted by the Transmit ATM Cell Processor block.
			Notes:
			The contents within these registers include all of the following: All ATM cells that have been read out from the TxFIFO, or the Transmit Cell Insertion Buffer.
			2. The contents of these registers do not include the number of Idle Cells that have been generated by the Transmit ATM Cell Processor block.
			3. If the number of Cells reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").

Table 411: Transmit ATM Cell Processor Block - Transmit ATM Cell Counter (Address = 0xNF2A)

			7, 0				
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Transmit ATM Cell Count[15:8]						
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0 *	.0 8	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit ATM Cell Count[15:8]	RUR	Transmit ATM Cell Count – Byte 1[15:8]: This RESET-upon-READ register, along with the "Transmit ATM Cell Count – Bytes 3, 2 and 0" registers; contain a 32-bit value for the number of User/Valid cells that have been transmitted by the Transmit ATM Cell Processor block.
		O'	Notes:
			1. The contents within these registers include all of the following: All ATM cells that have been read out from the TxFIFO, or the Transmit Cell Insertion Buffer.
			2. The contents of these registers do not include the number of Idle Cells that have been generated by the Transmit ATM Cell Processor block.
			3. If the number of Cells reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 412: Transmit ATM Cell Processor Block – Transmit ATM Cell Counter (Address = 0xNF2B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit ATM Cell Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION				
7 - 0	Transmit ATM	RUR	Transmit ATM Cell Count – Byte 0[7:0]:				
	Cell Count[7:0]		This RESET-upon-READ register, along with the "Transmit ATM Cell Count – Bytes 3 through 1" registers; contain a 32-bit value for the number of User/Valid cells that have been transmitted by the Transmit ATM Cell Processor block.				
			This particular register contains the LSB (Least Significant Byte) value for this 32-bit expression.				
			Notes:				
			1. The contents within these registers include all of the following: All ATM cells that have been read out from the TxFIFO, or the Transmit Cell Insertion Buffer.				
		2. The contents of these registers do not include the number of Idle Cells that have been generated by the Transmit ATM Cell Processor block.					
			3. If the number of Cells reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").				
	The	or of the standard of the stan	3. If the number of Cells reaches the value "OXFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x0000000").				

Table 413: Transmit ATM Cell Processor Block – Transmit ATM Cell Discard Cell Count – Byte 3 (Address = 0xNF2C)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit – Discard Cell Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	Transmit – Discard	RUR	Transmit – Discard Cell Count – Byte 3[7:0]:
	Cell Count[31:24]		This RESET-upon-READ register, along with the "Transmit ATM Cell Processor Block – Transmit ATM Cell Discard Cell Count – Bytes 2 through 0" registers; contain a 32-bit value for the number of ATM cells that have been discarded by the Transmit ATM Cell Processor block. This particular register contains the MSB (Most Significant Byte) value of this 32-bit expression. Notes: 1. The contents within these register includes all ATM cells that contain either a HEC Byte error or a "Transmit UTOPIA Parity" error. 2. If the number of Cells reaches the value "0xFFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x000000000").

Table 414: Transmit ATM Cell Processor Block - Transmit ATM Cell Discard Cell Count - Byte 2 (Address = 0xNF2D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit - Discard Cell Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0
	100 20° 20°						

		V	
BIT NUMBER	NAME (TYPE	DESCRIPTION
7 - 0	Transmit – Discard	RUR	Transmit – Discard Cell Count – Byte 2[7:0]:
	Cell Count[23:16]	910	This RESET-upon-READ register, along with the "Transmit ATM Cell Processor Block – Transmit ATM Cell Discard Cell Count – Bytes 3, 1 and 0" registers; contain a 32-bit value for the number of ATM cells that have been discarded by the Transmit ATM Cell Processor block.
			Notes:
			The contents within these register includes all ATM cells that contain either a HEC Byte error or a "Transmit UTOPIA Parity" error.
			2. If the number of Cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 415: Transmit ATM Cell Processor Block – Transmit ATM Cell Discard Cell Count – Byte 1 (Address = 0xNF2E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit – Discard Cell Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	Transmit – Discard	RUR	Transmit – Discard Cell Count – Byte 1[7:0]:
	Cell Count[15:8]		This RESET-upon-READ register, along with the "Transmit ATM Cell Processor Block – Transmit ATM Cell Discard Cell Count – Bytes 3, 2 and 0" registers; contain a 32-bit value for the number of ATM cells that have been discarded by the Transmit ATM Cell Processor block. Notes: 1. The contents within these register includes all ATM cells that contain either a HEC Byte error or a "Transmit UTOPIA Parity" error. 2. If the number of Cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").

Table 416: Transmit ATM Cell Processor Block Transmit ATM Cell Discard Cell Count – Byte 0 (Address = 0xNF2F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		7	「ransmit − Discard	Cell Count[7:	0]		
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0, 0,	0	0	0	0

BIT NUMBER	Name	TYPE	DESCRIPTION
7 - 0	Transmit – Discard Cell Count[7:0]	RUR	Transmit – Discard Cell Count – Byte 0[7:0]: This RESET-upon-READ register, along with the "Transmit ATM Cell Processor Block – Transmit ATM Cell Discard Cell Count – Bytes 3 through 1" registers; contain a 32-bit value for the number of ATM cells that have been discarded by the Transmit ATM Cell Processor block. This particular register contains the LSB (Least Significant Byte) value of this 32-bit expression. Notes: 1. The contents within these register includes all ATM cells that contain either a HEC Byte error or a "Transmit UTOPIA Parity" error. 2. If the number of Cells reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 417: Transmit ATM Cell Processor Block – Transmit ATM HEC Byte Error Count Register – Byte 3 (Address = 0xNF30)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit – HEC Byte Error Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit – HEC Byte	RUR	Transmit – HEC Byte Error Count – Byte 3[7:0]:
	Error Count[31:24]		This RESET-upon-READ register, along with the "Transmit ATM Cell Processor Block — Transmit ATM HEC Byte Error Count Register — Bytes 2 through 0" register; contain a 32-bit value for the number of ATM cells that contain HEC byte errors (as detected by the Transmit ATM Cell Processor block). This particular register functions as the MSB (Most Significant Byte) for this 32-bit expression. Notes: 1. This register is valid if the Transmit ATM Cell Processor block has been configured to compute and verify the HEC byte of each ATM cell that it receives from the TxFIFO or the "Transmit Cell Insertion Buffer". 2. If the number of cells reaches the value "0xFFFFFFFF", then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").

Table 418: Transmit ATM Cell Processor Block Transmit ATM HEC Byte Error Count Register – Byte 2 (Address = 0xNF31)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Transmit HEC Byte Error Count[23:16]						
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME 0	TYPE	DESCRIPTION
BIT NUMBER 7 - 0	NAME Transmit - HEC Byte Error Count[23:16]	RUR	Transmit – HEC Byte Error Count – Byte 2[7:0]: This RESET-upon-READ register, along with the "Transmit ATM Cell Processor Block – Transmit ATM HEC Byte Error Count Register – Bytes 3, 1 and 0" register; contain a 32-bit value for the number of ATM cells that contain HEC byte errors (as detected by the Transmit ATM Cell Processor block). Notes: 1. This register is valid if the Transmit ATM Cell Processor block has been configured to compute and verify the HEC byte of each ATM cell that it receives from the TxFIFO or the "Transmit Cell Insertion Buffer". 2. If the number of cells reaches the value "0xFFFFFFFF", then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x00000000").

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 419: Transmit ATM Cell Processor Block – Transmit ATM HEC Byte Error Count Register – Byte 1 (Address = 0xNF32)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit – HEC Byte Error Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit – HEC Byte	RUR	Transmit – HEC Byte Error Count – Byte 1[7:0]:
	Error Count[15:8]		This RESET-upon-READ register, along with the "Transmit ATM Cell Processor Block – Transmit ATM HEC Byte Error Count Register – Bytes 3, 2 and 0" register; contain a 32-bit value for the number of ATM cells that contain HEC byte errors (as detected by the Transmit ATM Cell Processor block). **Notes:** 1. This register is valid if the Transmit ATM Cell Processor block has been configured to compute and verify the HEC byte of each ATM cell that it receives from the TxFIFO or the "Transmit Cell Insertion Buffer". 2. If the number of cells reaches the value "0xFFFFFFFF", then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x000000000").

Table 420: Transmit ATM Cell Processor Block — Transmit ATM HEC Byte Error Count Register – Byte 0 (Address = 0xNF33)

0 () (000	- J			10 (
Віт 7	Віт 6	Віт 5	Віт 4	BIT 3	Віт 2	Віт 1	Віт 0
		Tra	ansmit HEC By	te Error Count[7:0]		
RUR	RUR	RUR	RURO	RUR	RUR	RUR	RUR
0	0	0		0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit – HEC Byte Error Count[7:0]	RUR	Transmit – HEC Byte Error Count – Byte 0[7:0]: This RESET-upon-READ register, along with the "Transmit ATM Cell Processor Block – Transmit ATM HEC Byte Error Count Register – Bytes 3 through 1" register; contain a 32-bit value for the number of ATM cells that contain HEC byte errors (as detected by the Transmit ATM Cell Processor block). This particular register functions as the LSB (Least Significant Byte) for this 32-bit expression. Notes: 1. This register is valid if the Transmit ATM Cell Processor block has been configured to compute and verify the HEC byte of each ATM cell that it receives from the TxFIFO or the "Transmit Cell Insertion Buffer". 2. If the number of cells reaches the value "0xFFFFFFF", then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x000000000").

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 421: Transmit ATM Cell Processor Block – Transmit UTOPIA Parity Error Count Register – Byte 3 (Address = 0xNF34)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit UTOPIA – Parity Error Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	Transmit UTOPIA – Parity Error Count[31:24]	RUR	Transmit UTOPIA Parity Error Count – Byte 3[7:0]: This RESET-upon-READ register, along with the "Transmit ATM Cell Processor Block – Transmit UTOPIA Parity Error Count Register – Bytes 2 through 0" registers; contains a 32-bit value for the number of ATM cells that contain "Transmit UTOPIA" Parity (byte or word) errors (as detected by the Transmit ATM Cell Processor block). This particular register functions as the MSB (Most Significant Byte) for this 32-bit expression. Notes: if the number of cells reaches the value "0xFFFFFFFF", then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x000000000").

Table 422: Transmit ATM Cell Processor Block - Transmit UTOPIA Parity Error Count Register – Byte 2 (Address = 0xNF35)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0		
		Transm	nit UTOPIA - Par	ty Error Coun	t[23:16]				
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	,00,0	0	0	0	0		

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit UTOPIA Parity Error Count[23:16]	BUR O Inay	Transmit UTOPIA Parity Error Count – Byte 2[7:0]: This RESET-upon-READ register, along with the "Transmit ATM Cell Processor Block – Transmit UTOPIA Parity Error Count Register – Bytes 3, 1 and 0" registers; contains a 32-bit value for the number of ATM cells that contain "Transmit UTOPIA" Parity (byte or word) errors (as detected by the Transmit ATM Cell Processor block). Notes: if the number of cells reaches the value "0xFFFFFFFF", then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x000000000").

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 423: Transmit ATM Cell Processor Block – Transmit UTOPIA Parity Error Count Register – Byte 1 (Address = 0xNF36)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Transr	nit UTOPIA – P	arity Error Cour	nt[15:8]		
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	Transmit UTOPIA –	RUR	Transmit UTOPIA Parity Error Count – Byte 1[7:0]:
	Parity Error Count[15:8]		This RESET-upon-READ register, along with the "Transmit ATM Cell Processor Block – Transmit UTOPIA Parity Error Count Register – Bytes 3, 2 and 0" registers; contains a 32-bit value for the number of ATM cells that contain "Transmit UTOPIA" Parity (byte or word) errors (as detected by the Transmit ATM Cell Processor block). Notes: if the number of cells reaches the value "0xFFFFFFFF, then these registers will saturate to and remain at this value (e.g., it will NOT overflow to "0x000000000").

Table 424: Transmit ATM Cell Processor Block – Transmit UTOPIA Parity Error Count Register – Byte 0 (Address = 0xNF37)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Э Віт 2	Віт 1	Віт 0
		Trans	mit UTOPIA - Parit	y Error Cou	nt[7:0]		
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	90	8	0	0	0

BIT NUMBER	Name	TYPE	DESCRIPTION	
7 - 0	Transmit UTOPIA – Parity Error Count[7:0]	RUR	Transmit UTOPIA Parity Error Count – Byte 0[7:0]: This RESET-upon-READ register, along with the "Transmit ATM C Processor Block – Transmit UTOPIA Parity Error Count Register Bytes 3 through 1" registers; contains a 32-bit value for the number ATM cells that contain "Transmit UTOPIA" Parity (byte or word) error (as detected by the Transmit ATM Cell Processor block). This particular register functions as the LSB (Least Significant Byte) of this 32-bit expression. Notes: if the number of cells reaches the value "0xFFFFFFFF", then these registers will saturate to and remain at this value (e.g. it will NOT overflow to "0x000000000").	of ors

Table 425: Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Filter 0 (Address = 0xNF43)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		Transmit User Cell Filter # 0 Enable	Copy Cell Enable	Discard Cell Enable	Filter if Pattern Match	
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3	Transmit User Cell Filter # 0	R/W	Transmit User Cell Filter #0 – Enable:
	Enable		This READ/WRITE bit-field permits the user to either enable or disable Transmit User Cell Filter # 0.
			If the user enables Transmit User Cell Filter # 0, then Transmit User Cell Filter # 0 will function per the configuration settings in Bits 2 through 0, within this register.
			If the user disables Transmit User Cell Filter # 0, then Transmit User Cell Filter # 0 then all cells that are applied to the input of Transmit User Cell Filter # 0 will pass through to the output of Transmit User Cell Filter # 0.
		N.C	0 - Disables Transmit User Cell Filter # 0.
		11/02	Enables Transmit User Cell Filter # 0.
2	Copy Cell Enable	R/W	Copy Cell Enable – Transmit User Cell Filter # 0:
	Copy Cell Enable	rpe of	This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 0 (within the Transmit ATM Cell Processor Block) to copy all cells that have header byte patterns that comply with the "user-defined" criteria, per Transmit User Cell Filter # 0, or to NOT copy any of these cells.
	the proshee in		If the user configures Transmit User Cell Filter # 0 to copy all cells complying with a certain "header-byte" pattern, then a copy (or replicate) of this "compliant" ATM cell will be routed to the Transmit Cell Extraction Buffer.
	dand.		If the user configures Transmit User Cell Filter # 0 to NOT copy all cells complying with a certain "header-byte" pattern, then NO copies (or replicates) of these "compliant" ATM cells will be made nor will any be routed to the Transmit Cell Extraction Buffer.
			0 – Configures Transmit User Cell Filter # 0 to NOT copy any cells that have header byte patterns which are compliant with the "user-defined" filtering criteria.
			1 – Configures Transmit User Cell Filter # 0 to copy any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria, and to route these copies (of cells) to the Transmit Cell Extraction Buffer.
			Notes: This bit-field is only active if "Transmit User Cell Filter # 0" has been enabled.
1	Discard Cell Enable	R/W	Discard Cell Enable – Transmit User Cell Filter # 0:
			This READ/WRITE bit-field permits the user to either

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			configure Transmit User Cell Filter # 0 (within the Transmit ATM Cell Processor Block) to discard all cells that have header byte patterns that comply with the "user-defined" criteria, per Transmit User Cell Filter # 0, or NOT discard any of these cells.
			If the user configures Transmit User Cell Filter # 0 to NOT discarded any cells that is compliant with a certain "header-byte" pattern, then the cell will be retained for further processing.
			0 – Configures Transmit User Cell Filter # 0 to NOT discard any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria.
			Configures Transmit User Cell Filter # 0 to discard any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria.
			Notes: This bit-field is only active if "Transmit User Cell Filter # 0" has been enabled.
0	Filter if Pattern Match	R/W	Filter if Pattern Match Transmit User Cell Filter # 0:
			This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 0 to filter (based upon the configuration settings for Bits 1 and 2, in this register) ATM cells with header bytes that match the "user-defined" header byte patterns, or to filter ATM cells with header bytes that do NOT match the "user-defined" header byte patterns.
			0 Configures Transmit User Cell Filter # 0 to filter user cells that do NOT match the header byte patterns (as defined in the ""registers).
		Plod	1 Configures Transmit User Cell Filter # 0 to filter user cells that do match the header byte patterns (as defined in the " " registers).
			Notes: This bit-field is only active if "Transmit User Cell Filter # 0" has been enabled.
	The product of the standing and man	not	

Table 426: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 1 (Address = 0xNF44)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit User Cell Filter # 0 – Pattern Register – Byte 1 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 0 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 0 – Pattern Register – Header Byte 1:
		oducte	The User Cell filtering criteria (for Transmit User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 Control Register. This READ/WRITE register, along with the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Register - Header Byte 1" permits the user to define the User Cell Filtering criteria for "Octet # 1" of the incoming User Cell. The user will write the header byte pattern (for Octet 1) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Register - Header Byte 1" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of and may no	the of	

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 427: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 2 (Address = 0xNF45)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit User Cell Filter # 0 – Pattern Register – Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 0 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 0 – Pattern Register – Header Byte 2:
	2		The User Cell filtering criteria (for Transmit User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 Control Register.
		prodi	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Register – Header Byte 2" permits the user to define the User Cell Filtering criteria for "Octet # 2" of the incoming User Cell. The user will write the header byte pattern (for Octet 2) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Register – Header Byte 2" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of the data she and man	are to	z otto

Table 428: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 3 (Address = 0xNF46)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	Transmit User Cell Filter # 0 – Pattern Register – Byte 3 [7:0]									
R/W R/W R/W R/W R/W R/W R/W										
0	0	0	0	0	0	0	0			

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 0 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 0 – Pattern Register – Header Byte 3:
	3		The User Cell filtering criteria (for Transmit User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 Control Register.
		oducte	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Register – Header Byte 3" permits the user to define the User Cell Filtering criteria for "Octet # 3" of the incoming User Cell. The user will write the header byte pattern (for Octet 3) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Register – Header Byte 3" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of product are	the of	

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 429: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 4 (Address = 0xNF47)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 0 – Pattern Register – Byte 4 [7:0]									
R/W R/W R/W R/W R/W R/W R/W									
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 0 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 0 – Pattern Register – Header Byte 4:
	4		The User Cell filtering criteria (for Transmit User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 Control Register.
		prodi	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Register – Header Byte 4" permits the user to define the User Cell Filtering criteria for "Octet # 4" of the incoming User Cell. The user will write the header byte pattern (for Octet 4) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Register – Header Byte 4" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of and ma	are to	2 of C

Table 430: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Register – Byte 1 (Address = 0xNF48)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	Transmit User Cell Filter # 0 – Check Register – Byte 1 [7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0	0	0	0	0	0	0	0			

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 0 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 0 – Check Register – Header Byte 1:
	1		The User Cell filtering criteria (for Transmit User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 Control Register.
		odució	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 1" permits the user to define the User Cell Filtering criteria for "Octet # 1" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 1" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 1" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	roduct or k	to of	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 1" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 1".
	The product or product are		Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 1" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 1" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 1").



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 431: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Register – Byte 2 (Address = 0xNF49)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 0 – Check Register – Byte 2 [7:0]									
R/W R/W R/W R/W R/W R/W R							R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 0 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 0 - Check Register - Header Byte 2:
	2		The User Cell filtering criteria (for Transmit User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 Control Register.
		prodi	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 2" permits the user to define the User Cell Filtering criteria for "Octet # 2" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 2" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 2" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	roduct	ale to	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 2" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 2".
	The product of and man		Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 2" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 2" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 2").

Table 432: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Register – Byte 3 (Address = 0xNF4A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	Transmit User Cell Filter # 0 – Check Register – Byte 3 [7:0]									
R/W R/W R/W R/W R/W R/W R/W										
0	0	0	0	0	0	0	0			

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 0 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 0 - Check Register - Header Byte 3:
	3		The User Cell filtering criteria (for Transmit User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 0 Control Register.
		odució	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 3" permits the user to define the User Cell Filtering criteria for "Octet # 3" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 3" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 3" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	roduct or k	the of	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 3" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 3".
	The product or product are		Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 3" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 3" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 3").



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 433: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Register – Byte 4 (Address = 0xNF4B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 0 – Check Register – Byte 4 [7:0]									
R/W R/W R/W R/W R/W R/W R									
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 0 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 0 - Check Register - Header Byte 4:
	4		The User Cell filtering criteria (for Transmit User Cell Filter # 0) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 Control Register.
		orodi	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 4" permits the user to define the User Cell Filtering criteria for "Octet # 4" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 4" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 4" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	roduct C	sie to	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 4" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 4".
	The product of and man	•	Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 4" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 4" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Pattern Register – Header Byte 4").

Table 434: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Filtered Cell Count – Byte 3 (Address = 0xNF4C)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Transmit User Cell Filter # 0 – Filtered Cell Count[31:24]						
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell	RUR	Transmit User Cell Filter # 0 – Filtered Cell Count[31:24]:
	Filter # 0 – Filtered Cell Count[31:24]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Filtered Cell Count – Bytes 2" through "0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 0 since the last read of this register.
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – User Cell Filter # 0" Register (Address = 0xNF43), these register bits will be incremented anytime User Cell Filter # 0 performs any of the following functions.
			Discards an incoming "User Cell".
			 Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer.
			Both the above actions.
			This particular register contains the MSB (Most Significant Byte) value for this 32-bit expression.
		, of	Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x000000000").
	, odi	ct at	ot be
	The production	may	
	· ·		



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 435: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Filtered Cell Count – Byte 2 (Address = 0xNF4D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit User Cell Filter # 0 – Filtered Cell Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION				
7 – 0	Transmit User Cell	RUR	Transmit User Cell Filter # 0 - Filtered Cell Count[23:16]:				
	Filter # 0 – Filtered Cell Count[23:16]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Filtered Cell Count – Bytes 3, 1 and 0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 0 since the last read of this register.				
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Transmit User Cell Filter # 0" Register (Address = 0xNF43), these register bits will be incremented anytime User Cell Filter # 0 performs any of the following functions. • Discards an incoming "User Cell".				
			Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer.				
			Both the above actions.				
			Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x000000000").				
	Notes: If the number of "filtered cells" reaches the value "0xFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").						

Table 436: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Filtered Cell Count – Byte 1 (Address = 0xNF4E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Transmit User Cell Filter # 0 - Filtered Cell Count[15:8]						
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

NAME	Түре	DESCRIPTION				
7 – 0 Transmit User Cell Filter # 0 – Filtered Cell Count[15:8]	RUR	Transmit User Cell Filter # 0 - Filtered Cell Count[15:8]:				
		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Filtered Cell Count – Bytes 3, 2 and 0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 0 since the last read of this register.				
		Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Transmit User Cell Filter # 0" Register (Address = 0xNF43), these register bits will be incremented anytime Transmit User Cell Filter # 0 performs any of the following functions				
		Discards an incoming "User Cell".				
		Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer.				
		Both the above actions.				
		Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").				
Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").						
	Transmit User Cell Filter # 0 – Filtered Cell Count[15:8]	Transmit User Cell Filter # 0 – Filtered Cell Count[15:8]				

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 437: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Filtered Cell Count – Byte 0 (Address = 0xNF4F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit User Cell Filter # 0 – Filtered Cell Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION			
7 – 0	Transmit User Cell	RUR	Transmit User Cell Filter # 0 - Filtered Cell Count[7:0]:			
	Filter # 0 – Filtered Cell Count[7:0]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 0 – Filtered Cell Count – Bytes 3" through "1" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 0 since the last read of this register.			
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Transmit User Cell Filter # 0" Register (Address = 0xNF43), these register bits will be incremented anytime Transmit User Cell Filter # 0 performs any of the following functions.			
			Discards an incoming "User Cell".			
			 Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer. Both the above actions. 			
			This particular register contains the LSB (Least Significant Byte) value for this 32-bit expression.			
			Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x000000000").			
	**Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").					

Table 438: Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Filter 1 (Address = 0xNF53)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused		Transmit User Cell Filter # 1 Enable	Copy Cell Enable	Discard Cell Enable	Filter if Pattern Match		
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3	Transmit User Cell Filter # 1	R/W	Transmit User Cell Filter #1 - Enable:
	Enable		This READ/WRITE bit-field permits the user to either enable or disable Transmit User Cell Filter # 1.
			If the user enables Transmit User Cell Filter # 1, then Transmit User Cell Filter # 1 will function per the configuration settings in Bits 2 through 0, within this register.
			If the user disables Transmit User Cell Filter # 1, then Transmit User Cell Filter # 1 then all cells that are applied to the input of Transmit User Cell Filter # 1 will pass through to the output of Transmit User Cell Filter # 1.
		, C	0 - Disables Transmit User Cell Filter # 1.
		11/02	Enables Transmit User Cell Filter # 1.
2	Copy Cell Enable	R/W	Copy Cell Enable – Transmit User Cell Filter # 1:
	Copy Cell Enable	rpe do	This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 1 (within the Transmit ATM Cell Processor Block) to copy all cells that have header byte patterns that comply with the "user-defined" criteria, per Transmit User Cell Filter # 1, or to NOT copy any of these cells.
	the proshee in		If the user configures Transmit User Cell Filter # 1 to copy all cells complying with a certain "header-byte" pattern, then a copy (or replicate) of this "compliant" ATM cell will be routed to the Transmit Cell Extraction Buffer.
	dand.		If the user configures Transmit User Cell Filter # 1 to NOT copy all cells complying with a certain "header-byte" pattern, then NO copies (or replicates) of these "compliant" ATM cells will be made nor will any be routed to the Transmit Cell Extraction Buffer.
			0 – Configures Transmit User Cell Filter # 1 to NOT copy any cells that have header byte patterns which are compliant with the "user-defined" filtering criteria.
			1 – Configures Transmit User Cell Filter # 1 to copy any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria, and to route these copies (of cells) to the Transmit Cell Extraction Buffer.
			Notes: This bit-field is only active if "Transmit User Cell Filter # 1" has been enabled.
1	Discard Cell Enable	R/W	Discard Cell Enable – Transmit User Cell Filter # 1:
			This READ/WRITE bit-field permits the user to either

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			configure Transmit User Cell Filter # 1 (within the Transmit ATM Cell Processor Block) to discard all cells that have header byte patterns that comply with the "user-defined" criteria, per Transmit User Cell Filter # 1, or NOT discard any of these cells.
			If the user configures Transmit User Cell Filter # 1 to NOT discarded any cells that is compliant with a certain "headerbyte" pattern, then the cell will be retained for further processing.
			0 – Configures Transmit User Cell Filter # 1 to NOT discard any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria.
			1 – Configures Transmit User Cell Filter # 1 to discard any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria.
			Notes: This bit-field is only active if "Transmit User Cell Filter # 1" has been enabled.
0	Filter if Pattern Match	R/W	Filter if Pattern Match — Transmit User Cell Filter # 1: This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 1 to filter (based upon the configuration settings for Bits 1 and 2, in this register) ATM cells with header bytes that match the "user-defined" header byte patterns, or to filter ATM cells with header bytes that do NOT match the "user-defined" header byte patterns. O = Configures Transmit User Cell Filter # 1 to filter user cells that do NOT match the header byte patterns (as defined in the ""registers). 1. Configures Transmit User Cell Filter # 1 to filter user cells that do match the header byte patterns (as defined in the "registers). Notes: This bit-field is only active if "Transmit User Cell Filter # 1" has been enabled.
	The product of and man	not	

Table 439: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 1 (Address = 0xNF54)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Transmit User Cell Filter # 1 – Pattern Register – Byte 1 [7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 1 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 1 – Pattern Register – Header Byte 1:
	'		The User Cell filtering criteria (for Transmit User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 Control Register.
		oducte	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Register – Header Byte 1" permits the user to define the User Cell Filtering criteria for "Octet # 1" of the incoming User Cell. The user will write the header byte pattern (for Octet 1) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Register – Header Byte 1" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of product are	in of	

EXARExperience *Qur* Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 440: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 2 (Address = 0xNF55)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Transmit User Cell Filter # 1 – Pattern Register – Byte 2 [7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 1 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 1 – Pattern Register – Header Byte 2:
	2		The User Cell filtering criteria (for Transmit User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 Control Register.
		orodi	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Register – Header Byte 2" permits the user to define the User Cell Filtering criteria for "Octet # 2" of the incoming User Cell. The user will write the header byte pattern (for Octet 2) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Register – Header Byte 2" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of and ma	are to	2010

Table 441: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 3 (Address = 0xNF56)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	Transmit User Cell Filter # 1 – Pattern Register – Byte 3 [7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 1 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 1 – Pattern Register – Header Byte 3:
	3		The User Cell filtering criteria (for Transmit User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 Control Register.
		oducte	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Register – Header Byte 3" permits the user to define the User Cell Filtering criteria for "Octet # 3" of the incoming User Cell. The user will write the header byte pattern (for Octet 3) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Register – Header Byte 3" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of product are	the of	

EXARExperience *Qur* Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 442: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 4 (Address = 0xNF57)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Transmit User Cell Filter # 1 – Pattern Register – Byte 4 [7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 1 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 1 – Pattern Register – Header Byte 4:
	4		The User Cell filtering criteria (for Transmit User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 Control Register.
		prodi	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Register – Header Byte 4" permits the user to define the User Cell Filtering criteria for "Octet # 4" of the incoming User Cell. The user will write the header byte pattern (for Octet 4) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Register – Header Byte 4" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of and man	are to	

Table 443: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Register – Byte 1 (Address = 0xNF58)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	Transmit User Cell Filter # 1 – Check Register – Byte 1 [7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 1 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 1 – Check Register – Header Byte 1:
	1		The User Cell filtering criteria (for Transmit User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 Control Register.
		odució	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 1" permits the user to define the User Cell Filtering criteria for "Octet # 1" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 1" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 1" by the User Cell
	The product or product are	no or	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 1" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 1".
	The Pisheay,		Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 1" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 1" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 1").



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 444: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Register – Byte 2 (Address = 0xNF59)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 1 – Check Register – Byte 2 [7:0]									
							R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 1 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 1 – Check Register – Header Byte 2:
	2		The User Cell filtering criteria (for Transmit User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 Control Register.
		, prod	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 2" permits the user to define the User Cell Filtering criteria for "Octet # 2" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 2" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 2" by the User Cell Filter, when determine whether to "filter" a given User Cell. Wtiting a "1" to a particular bit-field in this register, forces the
	roduct (c	are to	Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 2" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 2".
	The product of the data and ma	•	Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 2" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 2" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 2").

Table 445: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Register – Byte 3 (Address = 0xNF5A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 1 – Check Register – Byte 3 [7:0]									
R/W R/W							R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 1 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 1 – Check Register – Header Byte 3:
	3		The User Cell filtering criteria (for Transmit User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 1 Control Register.
		odució	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 3" permits the user to define the User Cell Filtering criteria for "Octet # 3" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 3" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 3" by the User Cell
	The product or product are	toe of	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 3" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 3".
	The Pisheay,		Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 3" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 3" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 3").

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 446: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Register – Byte 4 (Address = 0xNF5B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 1 – Check Register – Byte 4 [7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 1 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 1 – Check Register – Header Byte 4:
	4		The User Cell filtering criteria (for Transmit User Cell Filter # 1) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 Control Register.
		Prod	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 4" permits the user to define the User Cell Filtering criteria for "Octet # 4" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 4" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 4" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	roduct C	are to	Witing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 4" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 4".
	The product of the data and ma	S	Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 4" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 4" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Pattern Register – Header Byte 4").

Table 447: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Filtered Cell Count – Byte 3 (Address = 0xNF5C)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 1 – Filtered Cell Count[31:24]									
RUR RUR RUR RUR RUR RUR RUR RUR RUR							RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION							
7 – 0	Transmit User Cell	RUR	Transmit User Cell Filter # 1 – Filtered Cell Count[31:24]:							
	Filter # 1 – Filtered Cell Count[31:24]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Filtered Cell Count – Bytes 2" through "0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 1 since the last read of this register.							
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – User Cell Filter # 1" Register (Address = 0xNF53), these register bits will be incremented anytime User Cell Filter # 1 performs any of the following functions.							
			Discards an incoming "User Cell".							
			• Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer.							
			Both the above actions.							
			This particular register contains the MSB (Most Significant Byte) value for this 32-bit expression.							
		, of	Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x000000000").							
	"0xFFFFFFF" then these registers will saturate to and remain									

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 448: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Filtered Cell Count – Byte 2 (Address = 0xNF5D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 1 – Filtered Cell Count[23:16]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION						
7 – 0	Transmit User Cell Filter # 1 – Filtered	RUR	Transmit User Cell Filter # 1 – Filtered Cell Count[23:16]:						
	Cell Count[23:16]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Filtered Cell Count – Bytes 3, 1 and 0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 1 since the last read of this register.						
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Transmit User Cell Filter # 1" Register (Address = 0xNF53), these register bits will be incremented anytime User Cell Filter # 1 performs any of the following functions. • Discards an incoming "User Cell".						
			Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer.						
			Both the above actions. All the above actions.						
			Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").						

Table 449: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Filtered Cell Count – Byte 1 (Address = 0xNF5E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 1 – Filtered Cell Count[15:8]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell	RUR	Transmit User Cell Filter # 1 - Filtered Cell Count[15:8]:
	Filter # 1 – Filtered Cell Count[15:8]	These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Filtered Cell Count – Bytes 3, 2 and 0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 1 since the last read of this register.	
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Transmit User Cell Filter # 1" Register (Address = 0xNF53), these register bits will be incremented anytime Transmit User Cell Filter # 1 performs any of the following functions
			Discards an incoming "User Cell". Online (Continue) and incoming "User Cell" and another the "continue".
		Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer.	
		Both the above actions.	
			Notes: If the number of "filtered cells" reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x000000000").
	The production	neet at	eno ord

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 450: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Filtered Cell Count – Byte 0 (Address = 0xNF5F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Transmit User Cell Filter # 1 – Filtered Cell Count[7:0]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell	RUR	Transmit User Cell Filter # 1 – Filtered Cell Count[7:0]:
	Filter # 1 – Filtered Cell Count[7:0]	These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 1 – Filtered Cell Count – Bytes 3" through "1" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 1 since the last read of this register.	
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Transmit User Cell Filter # 1" Register (Address = 0xNF53), these register bits will be incremented anytime Transmit User Cell Filter # 1 performs any of the following functions.
			Discards an incoming "User Cell".
			 Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer. Both the above actions.
			This particular register contains the LSB (Least Significant Byte) value for this 32-bit expression.
			Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x000000000").
	Thepr	andn	"OxFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").

Table 451: Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Filter 2 (Address = 0xNF63)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused				Transmit User Cell Filter # 2 Enable	Copy Cell Enable	Discard Cell Enable	Filter if Pattern Match
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3	Transmit User Cell Filter # 2	R/W	Transmit User Cell Filter #2 – Enable:
	Enable		This READ/WRITE bit-field permits the user to either enable or disable Transmit User Cell Filter # 2.
			If the user enables Transmit User Cell Filter # 2, then Transmit User Cell Filter # 2 will function per the configuration settings in Bits 2 through 0, within this register.
			If the user disables Transmit User Cell Filter # 2, then Transmit User Cell Filter # 2 then all cells that are applied to the input of Transmit User Cell Filter # 2 will pass through to the output of Transmit User Cell Filter # 2.
			0 - Disables Transmit User Cell Filter # 2. 1- Enables Transmit User Cell Filter # 2.
2	Copy Cell Enable	R/W	Copy Cell Enable – Transmit User Cell Filter # 2:
	Copy Cell Enable	to of	This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 2 (within the Transmit ATM Cell Processor Block) to copy all cells that have header byte patterns that comply with the "user-defined" criteria, per Transmit User Cell Filter # 2, or to NOT copy any of these cells. If the user configures Transmit User Cell Filter # 2 to copy all cells complying with a certain "header-byte" pattern, then a copy (or replicate) of this "compliant" ATM cell will be routed
	Th data di		to the Transmit Cell Extraction Buffer. If the user configures Transmit User Cell Filter # 2 to NOT copy all cells complying with a certain "header-byte" pattern, then NO copies (or replicates) of these "compliant" ATM cells will be made nor will any be routed to the Transmit Cell Extraction Buffer.
			0 – Configures Transmit User Cell Filter # 2 to NOT copy any cells that have header byte patterns which are compliant with the "user-defined" filtering criteria.
			1 – Configures Transmit User Cell Filter # 2 to copy any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria, and to route these copies (of cells) to the Transmit Cell Extraction Buffer.
			Notes: This bit-field is only active if "Transmit User Cell Filter # 2" has been enabled.
1	Discard Cell Enable	R/W	Discard Cell Enable – Transmit User Cell Filter # 2:
			This READ/WRITE bit-field permits the user to either

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			configure Transmit User Cell Filter # 2 (within the Transmit ATM Cell Processor Block) to discard all cells that have header byte patterns that comply with the "user-defined" criteria, per Transmit User Cell Filter # 2, or NOT discard any of these cells.
			If the user configures Transmit User Cell Filter # 2 to NOT discarded any cells that is compliant with a certain "header-byte" pattern, then the cell will be retained for further processing.
			0 – Configures Transmit User Cell Filter # 2 to NOT discard any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria.
			Configures Transmit User Cell Filter # 2 to discard any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria.
			Notes: This bit-field is only active if "Transmit User Cell Filter # 2" has been enabled.
0	Filter if Pattern Match	R/W	Filter if Pattern Match Transmit User Cell Filter # 2:
			This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 2 to filter (based upon the configuration settings for Bits 1 and 2, in this register) ATM cells with header bytes that match the "user-defined" header byte patterns, or to filter ATM cells with header bytes that do NOT match the "user-defined" header byte patterns.
			0 Configures Transmit User Cell Filter # 2 to filter user cells that do NOT match the header byte patterns (as defined in the ""registers).
		Pio	1 Configures Transmit User Cell Filter # 2 to filter user cells that do match the header byte patterns (as defined in the " " registers).
			Notes: This bit-field is only active if "Transmit User Cell Filter # 2" has been enabled.
	The product of the standing and man	not	

Table 452: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 1 (Address = 0xNF64)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	Transmit User Cell Filter # 2 – Pattern Register – Byte 1 [7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 2 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 2 – Pattern Register – Header Byte 1:
		oducte	The User Cell filtering criteria (for Transmit User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 Control Register. This READ/WRITE register, along with the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Register - Header Byte 1" permits the user to define the User Cell Filtering criteria for "Octet # 1" of the incoming User Cell. The user will write the header byte pattern (for Octet 1) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Register - Header Byte 1" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of product are and may no	the of	

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 453: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 2 (Address = 0XNF65)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Transmit User Cell Filter # 2 – Pattern Register – Byte 2 [7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 2 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 2 – Pattern Register – Header Byte 2:
	2		The User Cell filtering criteria (for Transmit User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 Control Register.
		prodi	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Check Register – Header Byte 2" permits the user to define the User Cell Filtering criteria for "Octet # 2" of the incoming User Cell. The user will write the header byte pattern (for Octet 2) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Check Register – Header Byte 2" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The data sheet	are to	201

Table 454: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 3 (Address = 0xNF66)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	Transmit User Cell Filter # 2 – Pattern Register – Byte 3 [7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 2 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 2 – Pattern Register – Header Byte 3:
	3	oducte	The User Cell filtering criteria (for Transmit User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 Control Register. This READ/WRITE register, along with the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Register - Header Byte 3" permits the user to define the User Cell Filtering criteria for "Octet # 3" of the incoming User Cell. The user will write the header byte pattern (for Octet 3) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Register - Header Byte 3" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of product of product are	the of	

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 455: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 4 (Address = 0xNF67)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit User Cell Filter # 2 – Pattern Register – Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 2 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 2 – Pattern Register – Header Byte 4:
	4		The User Cell filtering criteria (for Transmit User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 Control Register.
		prodi	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Check Register – Header Byte 4" permits the user to define the User Cell Filtering criteria for "Octet # 4" of the incoming User Cell. The user will write the header byte pattern (for Octet 4) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Check Register – Header Byte 4" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of and man	are to	

Table 456: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Check Register – Byte 1 (Address = 0xNF68)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit User Cell Filter # 2 – Check Register – Byte 1 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 2 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 2 – Check Register – Header Byte 1:
	1		The User Cell filtering criteria (for Transmit User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 Control Register.
		oducte	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 1" permits the user to define the User Cell Filtering criteria for "Octet # 1" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 1" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 1" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	roduct or h	toe	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 1" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 1".
	The product or product are		Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 1" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 1" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 1").



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 457: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Check Register – Byte 2 (Address = 0xNF69)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit User Cell Filter # 2 – Check Register – Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 2 – Check Register – Header Byte 2	R/W	Transmit User Cell Filter # 2 – Check Register – Header Byte 2:
			The User Cell filtering criteria (for Transmit User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 Control Register.
		produc	This READWRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 2" permits the user to define the User Cell Filtering criteria for "Octet # 2" within the incoming User Cell. More specifically, these READWRITE register bits permit the user to specify which bit(s) in "Octet 2" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 2" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	The product of	othe	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 2" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 2".
	The data dinas		Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 2" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 2" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 2").

Table 458: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Check Register – Byte 3 (Address = 0xNF6A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Transmit User Cell Filter # 2 – Check Register – Byte 3 [7:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 2 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 2 - Check Register - Header Byte 3:
	3		The User Cell filtering criteria (for Transmit User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 2 Control Register.
		oducto	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 3" permits the user to define the User Cell Filtering criteria for "Octet # 3" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 3" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 3" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	roduct or s	no of	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 3" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 3".
	The product or product are		Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 3" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 3" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 3").



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 459: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Check Register – Byte 4 (Address = 0xNF6B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit User Cell Filter # 2 – Check Register – Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 2 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 2 – Check Register – Header Byte 4:
	4		The User Cell filtering criteria (for Transmit User Cell Filter # 2) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 Control Register.
		prodi	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 4" permits the user to define the User Cell Filtering criteria for "Octet # 4" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 4" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 4" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	roduct Co	ale to	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 4" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 4".
	The product of and man		Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 4" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 4" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Pattern Register – Header Byte 4").

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 460: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Filtered Cell Count – Byte 3 (Address = 0xNF6C)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit User Cell Filter # 2 – Filtered Cell Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 2 – Filtered	RUR	Transmit User Cell Filter # 2 – Filtered Cell Count[31:24]:
	Cell Count[31:24]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Filtered Cell Count – Bytes 2" through "0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 2 since the last read of this register.
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – User Cell Filter # 2" Register (Address = 0xNF63), these register bits will be incremented anytime User Cell Filter # 2 performs any of the following functions.
			Discards an incoming "User Cell".
			 Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer.
			Both the above actions.
			This particular register contains the MSB (Most Significant Byte) value for this 32-bit expression.
		, of	Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").
	The production	neet at	et be o

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 461: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Filtered Cell Count – Byte 2 (Address = 0xNF6D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 2 – Filtered Cell Count[23:16]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell	RUR	Transmit User Cell Filter # 2 – Filtered Cell Count[23:16]:
	Filter # 2 – Filtered Cell Count[23:16]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Filtered Cell Count – Bytes 3, 1 and 0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 2 since the last read of this register.
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Transmit User Cell Filter # 2" Register (Address = 0xNF63), these register bits will be incremented anytime User Cell Filter # 2 performs any of the following functions. • Discards an incoming "User Cell".
			Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer.
			Both the above actions. Notes: If the number of "filtered cells" reaches the value "OxFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x000000000").
	Thep	oduct	Notes: If the number of "filtered cells" reaches the value "0xFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").

Table 462: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Filtered Cell Count – Byte 1 (Address = 0xNF6E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 2 - Filtered Cell Count[15:8]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell	RUR	Transmit User Cell Filter # 2 – Filtered Cell Count[15:8]:
	Filter # 2 – Filtered Cell Count[15:8]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Filtered Cell Count – Bytes 3, 2 and 0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 2 since the last read of this register.
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Transmit User Cell Filter # 2" Register (Address = 0xNF63), these register bits will be incremented anytime Transmit User Cell Filter # 2 performs any of the following functions.
			Discards an incoming "User Cell".
			 Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer.
			Both the above actions.
			Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x000000000").
	The production	neet al	e no ord

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 463: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Filtered Cell Count – Byte 0 (Address = 0xNF6F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 2 – Filtered Cell Count[7:0]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 2 – Filtered	RUR	Transmit User Cell Filter # 2 – Filtered Cell Count[7:0]:
	Cell Count[7:0]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 2 – Filtered Cell Count – Bytes 3" through "1" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 2 since the last read of this register.
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Transmit User Cell Filter # 2" Register (Address = 0xNF63), these register bits will be incremented anytime Transmit User Cell Filter # 2 performs any of the following functions.
			Discards an incoming "User Cell".
			 Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer. Both the above actions.
			This particular register contains the LSB (Least Significant Byte) value for this 32-bit expression.
			Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x000000000").
	Thepr	andn	"OxFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").

Table 464: Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Filter 3 (Address = 0xNF63)

Віт 7	Віт 6	Віт 5 Віт 4		Віт 3	Віт 2	Віт 1	Віт 0
	Unused				Copy Cell Enable	Discard Cell Enable	Filter if Pattern Match
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3	Transmit User Cell Filter # 3	R/W	Transmit User Cell Filter #3 – Enable:
	Enable		This READ/WRITE bit-field permits the user to either enable or disable Transmit User Cell Filter # 3.
			If the user enables Transmit User Cell Filter # 3, then Transmit User Cell Filter # 3 will function per the configuration settings in Bits 2 through 0, within this register.
			If the user disables Transmit User Cell Filter # 3, then Transmit User Cell Filter # 3 then all cells that are applied to the input of Transmit User Cell Filter # 3 will pass through to the output of Transmit User Cell Filter # 3.
		N.C	0 - Disables Transmit User Cell Filter # 3.
		1110	Enables Transmit User Cell Filter # 3.
2	Copy Cell Enable	R/W	Copy Cell Enable – Transmit User Cell Filter # 3:
	Copy Cell Enable	rpe of	This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 3 (within the Transmit ATM Cell Processor Block) to copy all cells that have header byte patterns that comply with the "user-defined" criteria, per Transmit User Cell Filter # 3, or to NOT copy any of these cells.
	the proshee in		If the user configures Transmit User Cell Filter # 3 to copy all cells complying with a certain "header-byte" pattern, then a copy (or replicate) of this "compliant" ATM cell will be routed to the Transmit Cell Extraction Buffer.
	da and		If the user configures Transmit User Cell Filter # 3 to NOT copy all cells complying with a certain "header-byte" pattern, then NO copies (or replicates) of these "compliant" ATM cells will be made nor will any be routed to the Transmit Cell Extraction Buffer.
			0 – Configures Transmit User Cell Filter # 3 to NOT copy any cells that have header byte patterns which are compliant with the "user-defined" filtering criteria.
			1 – Configures Transmit User Cell Filter # 3 to copy any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria, and to route these copies (of cells) to the Transmit Cell Extraction Buffer.
			Notes: This bit-field is only active if "Transmit User Cell Filter # 3" has been enabled.
1	Discard Cell Enable	R/W	Discard Cell Enable – Transmit User Cell Filter # 3:
			This READ/WRITE bit-field permits the user to either

EXAR

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			configure Transmit User Cell Filter # 3 (within the Transmit ATM Cell Processor Block) to discard all cells that have header byte patterns that comply with the "user-defined" criteria, per Transmit User Cell Filter # 3, or NOT discard any of these cells.
			If the user configures Transmit User Cell Filter # 3 to NOT discarded any cells that is compliant with a certain "header-byte" pattern, then the cell will be retained for further processing.
			0 – Configures Transmit User Cell Filter # 3 to NOT discard any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria.
			1 – Configures Transmit User Cell Filter # 3 to discard any cells that have header byte patterns that are compliant with the "user-defined" filtering criteria.
			Notes: This bit-field is only active if "Transmit User Cell Filter # 3" has been enabled.
0	Filter if Pattern Match	R/W	Filter if Pattern Match Transmit User Cell Filter # 3:
			This READ/WRITE bit-field permits the user to either configure Transmit User Cell Filter # 3 to filter (based upon the configuration settings for Bits 1 and 2, in this register) ATM cells with header bytes that match the "user-defined" header byte patterns, or to filter ATM cells with header bytes that do NOT match the "user-defined" header byte patterns.
			0 Configures Transmit User Cell Filter # 3 to filter user cells that do NOT match the header byte patterns (as defined in the ""registers).
		Pio	1 Configures Transmit User Cell Filter # 3 to filter user cells that do match the header byte patterns (as defined in the " " registers).
	c. C		Notes: This bit-field is only active if "Transmit User Cell Filter # 3" has been enabled.
	The product of and man	not	

Table 465: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 1 (Address = 0xNF64)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	Transmit User Cell Filter # 3 – Pattern Register – Byte 1 [7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W			
0	0	0	0	0	0	0	0			

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 3 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 3 – Pattern Register – Header Byte 1:
	'		The User Cell filtering criteria (for Transmit User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 Control Register.
		oducte	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Register – Header Byte 1" permits the user to define the User Cell Filtering criteria for "Octet # 1" of the incoming User Cell. The user will write the header byte pattern (for Octet 1) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Register – Header Byte 1" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of product are	in of	

EXARExperience *Qur* Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 466: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 2 (Address = 0xNF65)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Transmit User Cell Filter # 3 – Pattern Register – Byte 2 [7:0]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 3 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 3 – Pattern Register – Header Byte 2:
	2		The User Cell filtering criteria (for Transmit User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 Control Register.
		orodi	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Register – Header Byte 2" permits the user to define the User Cell Filtering criteria for "Octet # 2" of the incoming User Cell. The user will write the header byte pattern (for Octet 2) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Register – Header Byte 2" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.
	The product of and ma	are to	zotto

Table 467: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 3 (Address = 0xNF66)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Transmit User Cell Filter # 3 – Pattern Register – Byte 3 [7:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION			
7 – 0	Transmit User Cell Filter # 3 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 3 – Pattern Register – Header Byte 3:			
	3	oducte	The User Cell filtering criteria (for Transmit User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 Control Register. This READ/WRITE register, along with the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Register - Header Byte 3" permits the user to define the User Cell Filtering criteria for "Octet # 3" of the incoming User Cell. The user will write the header byte pattern (for Octet 3) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Register - Header Byte 3" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.			
indicates which bits within the first octet of the incoming are to be compared with the contents of this register.						

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 468: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 4 (Address = 0xNF67)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit User Cell Filter # 3 – Pattern Register – Byte 4 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION			
7 – 0	Transmit User Cell Filter # 3 – Pattern Register – Header Byte	R/W	Transmit User Cell Filter # 3 – Pattern Register – Header Byte 4:			
	4		The User Cell filtering criteria (for Transmit User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 Control Register.			
		prodi	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Register – Header Byte 4" permits the user to define the User Cell Filtering criteria for "Octet # 4" of the incoming User Cell. The user will write the header byte pattern (for Octet 4) that he/she wishes to use as part of the "User Cell Filtering" criteria, into this register. The user will also write in a value into the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Register – Header Byte 4" that indicates which bits within the first octet of the incoming cells are to be compared with the contents of this register.			
Cell Filter # 3 — Check Register — Header Byte 4" the indicates which bits within the first octet of the incoming cell are to be compared with the contents of this register.						

Table 469: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Register – Byte 1 (Address = 0xNF68)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Transmit User Cell Filter # 3 – Check Register – Byte 1 [7:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 3 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 3 – Check Register – Header Byte 1:
	1		The User Cell filtering criteria (for Transmit User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 Control Register.
		oducte	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 1" permits the user to define the User Cell Filtering criteria for "Octet # 1" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 1" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 1" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	roduct or h	toeo	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 1" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 1".
	The product or product are		Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 1" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 1" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 1").

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 470: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Register – Byte 2 (Address = 0xNF69)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit User Cell Filter # 3 – Check Register – Byte 2 [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 3 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 3 – Check Register – Header Byte 2:
	2		The User Cell filtering criteria (for Transmit User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 Control Register.
		prodi	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 2" permits the user to define the User Cell Filtering criteria for "Octet # 2" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 2" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 2" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	roduct	aie to	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 2" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 2".
	The product of and man		Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 2" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 2" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 2").

Table 471: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Register – Byte 3 (Address = 0xNF6A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Transmit User	Cell Filter # 3 -	Check Registe	r – Byte 3 [7:0]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 3 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 3 – Check Register – Header Byte 3:
	3		The User Cell filtering criteria (for Transmit User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Pattern Registers", the four "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 - Check Registers" and the "Transmit ATM Cell Processor Block - Transmit User Cell Filter # 3 Control Register.
		oducte	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 3" permits the user to define the User Cell Filtering criteria for "Octet # 3" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 3" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 3" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	roduct or k	the of	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 3" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 3".
	The product or product are		Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 3" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 3" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 3").

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 472: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Register – Byte 4 (Address = 0xNF6B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Transmit User	Cell Filter # 3 -	Check Registe	r – Byte 4 [7:0]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell Filter # 3 – Check Register – Header Byte	R/W	Transmit User Cell Filter # 3 – Check Register – Header Byte 4:
	4		The User Cell filtering criteria (for Transmit User Cell Filter # 3) is defined based upon the contents of 9 read/write registers. These registers are the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Registers", the four "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Check Registers" and the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 Control Register.
		orodi	This READ/WRITE register, along with the "Transmit ATM Cell Processor Block – Transmit User Cell Filter #3 – Pattern Register – Header Byte 4" permits the user to define the User Cell Filtering criteria for "Octet # 4" within the incoming User Cell. More specifically, these READ/WRITE register bits permit the user to specify which bit(s) in "Octet 4" of the incoming user cell (in the Transmit ATM Cell Processor Block) are to be checked against the corresponding bit-fields within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter #3 – Pattern Register – Header Byte 4" by the User Cell Filter, when determine whether to "filter" a given User Cell.
	roduct co	ale to	Writing a "1" to a particular bit-field in this register, forces the Transmit User Cell Filter to check and compare the corresponding bit in "Octet # 4" (of the incoming user cell) with the corresponding bit in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 4".
	The product of and man		Writing a "0" to a particular bit-field in this register causes the Transmit User Cell Filter to treat the corresponding bit within "Octet # 4" (in the incoming user cell) as a "don't care" (e.g., to forgo the comparison between the corresponding bit in "Octet # 4" of the incoming user cell with the corresponding bit-field in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Pattern Register – Header Byte 4").

Table 473: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Filtered Cell Count – Byte 3 (Address = 0xNF6C)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Transmit Use	er Cell Filter # 3	- Filtered Cell	Count[31:24]		
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell	RUR	Transmit User Cell Filter # 3 – Filtered Cell Count[31:24]:
	Filter # 3 – Filtered Cell Count[31:24]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Filtered Cell Count – Bytes 2" through "0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 3 since the last read of this register.
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – User Cell Filter # 3" Register (Address = 0xNF63), these register bits will be incremented anytime User Cell Filter # 3 performs any of the following functions.
			Discards an incoming "User Cell".
			 Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer.
			Both the above actions.
			This particular register contains the MSB (Most Significant Byte) value for this 32-bit expression.
		, of	Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").
	The production	neet at	e be

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 474: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Filtered Cell Count – Byte 2 (Address = 0xNF6D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Transmit Use	er Cell Filter # 3	- Filtered Cell	Count[23:16]		
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

ATM Cell Processor Block – Transmit User Cell Filter # 3 – Filtered Ce Count – Bytes 3, 1 and 0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 3 since the last read of this register. Depending upon the configuration settings within the "Transmit ATM Ce Processor Block – Transmit User Cell Filter Control – Transmit User Ce Filter # 3" Register (Address = 0xNF63), these register bits will be incremented anytime User Cell Filter # 3 performs any of the following functions. • Discards an incoming "User Cell". • Copies (or Replicates) an incoming "User Cell" and routes the "copy to the Transmit Cell Extraction Buffer. • Both the above actions. Notes: If the number of "filtered cells" reaches the value	BIT NUMBER	Name	Түре	DESCRIPTION
These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Filtered Ce Count – Bytes 3, 1 and 0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 3 since the last read of this register. Depending upon the configuration settings within the "Transmit ATM Ce Processor Block – Transmit User Cell Filter Control – Transmit User Ce Filter # 3" Register (Address = 0xNF63), these register bits will be incremented anytime User Cell Filter # 3 performs any of the following functions. • Discards an incoming "User Cell". • Copies (or Replicates) an incoming "User Cell" and routes the "copy to the Transmit Cell Extraction Buffer. • Both the above actions.	7 – 0		RUR	Transmit User Cell Filter # 3 – Filtered Cell Count[23:16]:
Processor Block – Transmit User Cell Filter Control – Transmit User Ce Filter # 3" Register (Address = 0xNF63), these register bits will be incremented anytime User Cell Filter # 3 performs any of the following functions. • Discards an incoming "User Cell". • Copies (or Replicates) an incoming "User Cell" and routes the "copy to the Transmit Cell Extraction Buffer. • Both the above actions.				These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Filtered Cell Count – Bytes 3, 1 and 0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 3 since the last read of this register.
to the Transmit Cell Extraction Buffer. • Both the above actions.				
1000				Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer.
Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").				
The product of he or the order				Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x000000000").
		Thepi	oduct, and many	at not be of o

Table 475: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Filtered Cell Count – Byte 1 (Address = 0xNF6E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Transmit Us	er Cell Filter # 3	3 – Filtered Cell	Count[15:8]		
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell	RUR	Transmit User Cell Filter # 3 – Filtered Cell Count[15:8]:
	Filter # 3 – Filtered Cell Count[15:8]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Filtered Cell Count – Bytes 3, 2 and 0" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 3 since the last read of this register.
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Transmit User Cell Filter # 3" Register (Address = 0xNF63), these register bits will be incremented anytime Transmit User Cell Filter # 3 performs any of the following functions
			Discards an incoming "User Cell".
			Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer.
			Both the above actions.
			Notes: If the number of "filtered cells" reaches the value "0xFFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x000000000").
	The production	neet at	eno ord

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 476: Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Filtered Cell Count – Byte 0 (Address = 0xNF6F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Transmit Us	ser Cell Filter #	3 – Filtered Cel	l Count[7:0]		
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Transmit User Cell	RUR	Transmit User Cell Filter # 3 – Filtered Cell Count[7:0]:
	Filter # 3 – Filtered Cell Count[7:0]		These RESET-upon-READ bit-fields, along with that in the "Transmit ATM Cell Processor Block – Transmit User Cell Filter # 3 – Filtered Cell Count – Bytes 3" through "1" register contain a 32-bit expression for the number of User Cells that have been filtered by Transmit User Cell Filter # 3 since the last read of this register.
			Depending upon the configuration settings within the "Transmit ATM Cell Processor Block – Transmit User Cell Filter Control – Transmit User Cell Filter # 3" Register (Address = 0xNF63), these register bits will be incremented anytime Transmit User Cell Filter # 3 performs any of the following functions.
			Discards an incoming "User Cell".
			 Copies (or Replicates) an incoming "User Cell" and routes the "copy" to the Transmit Cell Extraction Buffer. Both the above actions.
			This particular register contains the LSB (Least Significant Byte) value for this 32-bit expression.
			Notes: If the number of "filtered cells" reaches the value "0xFFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x000000000").
	Thepr	andn	"OxFFFFFF" then these registers will saturate to and remain at this value (e.g., it will not overflow to "0x00000000").

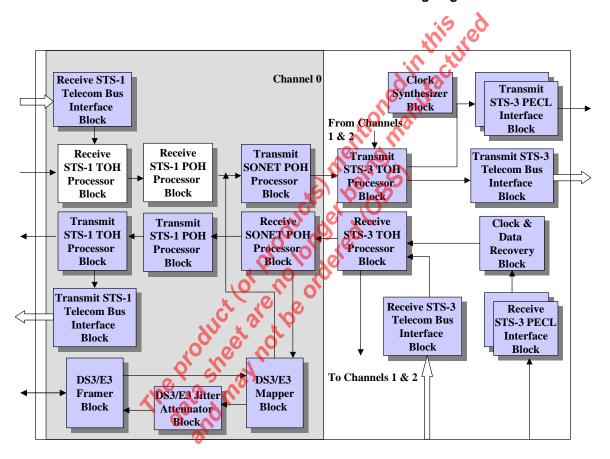
1.11 RECEIVE STS-1 TOH AND POH PROCESSOR BLOCK

The register map for the Receive STS-1 TOH and POH Processor Block is presented in the Table below. Additionally, a detailed description of each of the "Receive STS-1 TOH and POH Processor" block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33 device, with the "Receive STS-1 TOH and POH Processor Blocks "highlighted" is presented below in

Figure 10

Figure 12: Illustration of the Functional Block Diagram of the XRT94L33 device, with the Receive STS-1 TOH and POH Processor Blocks "High-lighted".







1.11.1 RECEIVE STS-1 TOH AND POH PROCESSOR BLOCK REGISTER

Table 477: Receive STS-1 TOH and POH Processor Block Control Register Address Map

Individual Register Address	Address Location	REGISTER NAME	DEFAULT VALUES
0x00 - 0x02	0xN000 - 0xN102	Reserved	0x00
0x03	0xN103	Receive STS-1 Transport Control Register – Byte 0	0x00
0x04, 0x05	0xN104 – 0xN105	Reserved	0x00
0x06	0xN106	Receive STS-1 Transport Status Register – Byte 1	0x00
0x07	0xN107	Receive STS-1 Transport Status Register – Byte 0	0x02
0x08	0xN108	Reserved	0x00
0x09	0xN109	Receive STS-1 Transport Interrupt Status Register – Byte 2	0x00
0x0A	0xN10A	Receive STS-1 Transport Interrupt Status Register – Byte 1	0x00
0x0B	0xN10B	Receive STS-1 Transport Interrupt Status Register – Byte 0	0x00
0x0C	0xN10C	Reserved	0x00
0x0D	0xN10D	Receive STS-1 Transport Interrupt Enable Register – Byte 2	0x00
0x0E	0xN10E	Receive STS-1 Transport Interrupt Enable Register – Byte 1	0x00
0x0F	0xN10F	Receive STS-1 Transport Intetrupt Enable Register – Byte 0	0x00
0x10	0xN110	Receive STS-1 Transport B1 Byte Error Count – Byte 3	0x00
0x11	0xN111	Receive STS-1 Transport B1 Byte Error Count – Byte 2	0x00
0x12	0xN112	Receive STS-1 Transport B1 Byte Error Count – Byte 1	0x00
0x13	0xN113	Receive STS-1 Transport B1 Byte Error Count – Byte 0	0x00
0x14	0xN114	Receive STS-1 Transport B2 Byte Error Count – Byte 3	0x00
0x15	0xN115	Receive STS-1 Transport B2 Byte Error Count – Byte 2	0x00
0x16	0xN116	Receive STS-1 Transport B2 Byte Error Count – Byte 1	0x00
0x17	0xN117	Receive STS-1 Transport B2 Byte Error Count – Byte 0	0x00
0x18	0xN118	Receive STS-1 Transport REI-L Error Count – Byte 3	0x00
0x19	0xN119	Receive STS-1 Transport REI-L Error Count – Byte 2	0x00
0x1A	0xN11A	Receive STS-1 Transport REI-L Error Count – Byte 1	0x00
0x1B	0xN11B	Receive STS-1 Transport REI-L Error Count – Byte 0	0x00
0x1C	0xN11C	Reserved	0x00
0x1D, 0x1E	0xN11D – 0xN11E	Reserved	0x00
0x1F	0xN11F	Receive STS-1 Transport – Received K1 Byte Value Register	0x00

Individual Register Address	Address Location	REGISTER NAME	DEFAULT VALUES
0x20 - 0x22	0xN120 - 0xN122	Reserved	0x00
0x23	0xN123	Receive STS-1 Transport – Received K2 Byte Value Register	0x00
0x24 - 0x26	0xN124 – 0xN126	Reserved	0x00
0x27	0xN127	Receive STS-1 Transport – Received S1 Byte Value Register	0x00
0x28 – 0x2D	0xN128 – 0xN12D	Reserved	0x00
0x2E	0xN12E	Receive STS-1 Transport – LOS Threshold Value – MSB	0xFF
0x2F	0xN12F	Receive STS-1 Transport – LOS Threshold Value LSB	0xFF
0x30	0xN130	Reserved	0x00
0x31	0xN131	Receive STS-1 Transport – Receive SF Set Monitor Interval – Byte 2	0x00
0x32	0xN132	Receive STS-1 Transport – Receive SF Set Monitor Interval – Byte 1	0x00
0x33	0xN133	Receive STS-1 Transport - Receive SF Set Monitor Interval - Byte 0	0x00
0x34, 0x35	0xN134, 0xN135	Reserved	0x00
0x36	0xN136	Receive STS-1 Transport - Receive SF Set Threshold - Byte 1	0x00
0x37	0xN137	Receive STS-1 Transport - Receive SF Set Threshold - Byte 0	0x00
0x38, 0x39	0xN138 - 0xN139	Reserved	0x00
0x3A	0xN13A	Receive STS-1 Transport – Receive SF Clear Threshold – Byte 1	0x00
0x3B	0xN13B	Receive STS-1 Transport – Receive SF Clear Threshold – Byte 0	0x00
0x3C	0xN13C	Reserved	0x00
0x3D	0xN13D	Receive STS-1 Transport – Receive SD Set Monitor Interval – Byte	0x00
0x3E	0xN13E	Receive STS-1 Transport – Receive SD Set Monitor Interval – Byte	0x00
0x3F	0xN13F	Receive STS-1 Transport – Receive SD Set Monitor Interval – Byte 0	0x00
0x40, 0x41	0xN140 - 0xN141	Reserved	0x00
0x42	0xN142	Receive STS-1 Transport – Receive SD Set Threshold – Byte 1	0x00
0x43	0xN143	Receive STS-1 Transport – Receive SD Set Threshold – Byte 0	0x00
0x44, 0x45	0xN144, 0xN145	Reserved	0x00
0x46	0xN146	Receive STS-1 Transport – Receive SD Clear Threshold – Byte 1	0x00

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

INDIVIDUAL REGISTER ADDRESS	Address Location	REGISTER NAME	DEFAULT VALUES
0x47	0xN147	Receive STS-1 Transport – Receive SD Clear Threshold – Byte 0	0x00
0x48 – 0x4A	0xN14B - 0xN14A	Reserved	0x00
0x4B	0xN14B	Receive STS-1 Transport – Force SEF Condition	0x00
0x4C - 0x4E	0xN14C - 0xN14E	Reserved	0x00
0x4F	0xN14F	Receive STS-1 Transport – Receive J0 Byte Trace Buffer Control Register	0x00
0x50 – 0x51	0xN150 – 0xN151	Reserved	
0x52	0xN152	Receive STS-1 Transport – Receive SD Burst Error Count Tolerance – Byte 1	0x00
0x53	0xN153	Receive STS-1 Transport – Receive SD Burst Error Count Tolerance – Byte 0	0x00
0x54, 0x55	0xN154, 0xN155	Reserved	0x00
0x56	0xN156	Receive STS-1 Transport – Receive ST Burst Error Count Tolerance – Byte 1	0x00
0x57	0xN157	Receive STS-1 Transport Receive SF Burst Error Count Tolerance – Byte 0	0x00
0x58	0xN158	Reserved	0x00
0x59	0xN159	Receive STS-Transport Receive SD Clear Monitor Interval – Byte 2	0x00
0x5A	0xN15A	Receive STS-1 Transport - Receive SD Clear Monitor Interval - Byte 1	0x00
0x5B	0xN15B	Receive STS-1 Transport - Receive SD Clear Monitor Interval - Byte 0	0x00
0x5C	0xN15C	Reserved	0x00
0x5D	0xN15D	Receive STS-1 Transport – Receive SF Clear Monitor Interval – Byte 2	0x00
0x5E	0xN15E	Receive STS-1 Transport – Receive SF Clear Monitor Interval – Byte 1	0x00
0x5F	0xN15F	Receive STS-1 Transport – Receive SF Clear Monitor Interval – Byte 0	0x00
0x60 - 0x62	0xN160 - 0xN162	Reserved	0x00
0x63	0xN163	Receive STS-1 Transport – Auto AIS Control Register	0x00
0x64 - 0x6A	0xN164 – 0xN16A	Reserved	0x00
0x6B	0xN16B	Receive STS-1 Transport – Auto AIS (in Downstream STS-1s) Control Register	0x00

Individual Register Address	Address Location	REGISTER NAME	DEFAULT VALUES
0x6C - 0x82	0xN16C - 0xN182	Reserved	0x00
0x83	0xN183	Receive STS-1 Path – Control Register – Byte 2	0x00
0x84, 0x85	0xN184 - 0xN185	Reserved	0x00
0x86	0xN186	Receive STS-1 Path – Control Register – Byte 1	
0x87	0xN187	Receive STS-1 Path – Status Register – Byte 0	0x00
0x88	0xN188	Reserved	0x00
0x89	0xN189	Receive STS-1 Path – Interrupt Status Register – Byte 2	0x00
0x8A	0xN18A	Receive STS-1 Path – Interrupt Status Register – Byte 1	0x00
0x8B	0xN18B	Receive STS-1 Path – Interrupt Status Register – Byte 0	0x00
0x8C	0xN18C	Reserved	0x00
0x8D	0xN18D	Receive STS-1 Path – Interrupt Enable Register – Byte 2	0x00
0x8E	0xN18E	Receive STS-1 Path – Interrupt Enable Register – Byte 1	0x00
0x8F	0xN18F	Receive STS-1 Path Interrupt Enable Register – Byte 0	0x00
0x90 - 0x92	0xN190 - 0xN192	Reserved	0x00
0x93	0xN193	Receive STS Path SONET Receive RDI-P Register	0x00
0x94, 0x95	0xN194, 0xN195	Reserved	0x00
0x96	0xN196	Receive STS-1 Path - Received Path Label Value (C2 Byte) Register	0x00
0x97	0xN197	Receive STS-1 Path – Expected Path Label Value (C2 Byte) Register	0x00
0x98	0xN198	Receive STS-1 Path – B3 Error Count Register – Byte 3	0x00
0x99	0xN199	Receive STS-1 Path – B3 Error Count Register – Byte 2	0x00
0x9A	0xN19A	Receive STS-1 Path – B3 Error Count Register – Byte 1	0x00
0x9B	0xN19B	Receive STS-1 Path – B3 Error Count Register – Byte 0	0x00
0x9C	0xN19C	Receive STS-1 Path – REI-P Error Count Register – Byte 3	0x00
0x9D	0xN19D	Receive STS-1 Path – REI-P Error Count Register – Byte 2	0x00
0x9E	0xN19E	Receive STS-1 Path – REI-P Error Count Register – Byte 1	0x00
0x9F	0xN19F	Receive STS-1 Path – REI-P Error Count Register – Byte 0	0x00
0xA0 - 0xA5	0xN1A0 – 0xN1A5	Reserved	0x00
0xA6	0xN1A6	Receive STS-1 Path – Pointer Value Register – Byte 1	0x00
0xA7	0xN1A7	Receive STS-1 Path – Pointer Value Register – Byte 0	0x00

XRT94L33

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

INDIVIDUAL REGISTER ADDRESS	Address Location	REGISTER NAME	DEFAULT VALUES
0xA8 – 0xBA	0xN1A8 – 0xN1BA	Reserved	0x00
0xBB	0xN1BB	Receive STS-1 Path – AUTO AIS Control Register	0x00
0xBC - 0xBE	0xN1BC – 0xN1BE	Reserved	0x00
0xBF	0xN1BF	Receive STS-1 Path – Serial Port Control Register	0x00
0xC0 - 0xC2	0xN1C0 - 0xN1C2	Reserved	0x00
0xC3	0xN1C3	Receive STS-1 Path – SONET Receive Auto Alarm Register – Byte 0	0x00
0xC4 - 0xD2	0xN1C4 – 0xN1D2	Reserved	
0xD3	0xN1D3	Receive STS-1 Path – Receive J1 Byte Capture Register	0x00
0xC4-0xC6	0xN1C4 - 0xN1C6	Reserved	0x00
0xD7	0xN1D7	Receive STS-1 Path – Receive B3 Byte Capture Register	0x00
0xD8 – 0xDA	0xN1D8 – 0xN1DA	Reserved	0x00
0xDB	0xN1DB	Receive STS-1 Path – Receive C2 Byte Capture Register	0x00
0xDC - 0xDE	0xN1DC – 0xN1DE	Reserved	0x00
0xDF	0xN1DF	Receive STS-1 Path - Receive G1 Byte Capture Register	0x00
0xE0 - 0xE2	0xN1E0 - 0xN1E2	Reserved	0x00
0xE3	0xN1E3	Receive STS-1 Path - Receive F2 Byte Capture Register	0x00
0xE4 - 0xE6	0xN1E4 – 0xN1E6	Reserved	0x00
0xE7	0xN1E7	Receive STS-1 Path – Receive H4 Byte Capture Register	0x00
0xE8 - 0xEA	0xN1E8- 0xN1EA	Reserved	0x00
0xEB	0xN1EB	Receive STS-1 Path – Receive Z3 Byte Capture Register	0x00
0xEC - 0xEE	0xN1EC – 0xN1EE	Reserved	0x00
0xEF	0xN1EF	Receive STS-1 Path – Receive Z4 (K3) Byte Capture Register	0x00
0xF0 - 0xF2	0xN1F0 – 0xN1F2	Reserved	0x00
0xF3	0xN1F3	Receive STS-1 Path – Receive Z5 Byte Capture Register	0x00
0xF6 - 0xFF	0xN1F6 – 0xN1FF	Reserved	0x00

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

1.11.2 RECEIVE STS-1 TOH AND POH PROCESSOR BLOCK REGISTER DESCRIPTION

Table 478: Receive STS-1 Transport Control Register – Byte 0 (Address Location = 0xN103)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	SF Detect Enable	SD Detect Enable	Descramble Disable	Unused	REI-L Error Type	B2 Error Type	B1 Error Type
R/O	R/W	R/W	R/W	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Unused	R/O	nis ed
6	SF Detect	R/W	Signal Failure (SF) Detect Enable:
	Enable		This READ/WRITE bit-field permits the user to enable or disable SF Detection by the Receive STS-1 TOH Processor block.
			0 – SF Detection is disabled.
			1 – SF Detection is enabled
5	SD Detect	R/W	Signal Degrade (SD) Detect Enable:
	Enable		This READ/WRITE bit-field permits the user to enable or disable SD Detection by the Receive STS-1 TOH Processor block.
			0 – SD Detection is disabled.
			1 – SD Detection is enabled.
4	Descramble	R/W	De-Scramble Disable:
	Disable		This READ/WRITE bit-field permits the user to either enable or disable descrambling by the Receive STS-1 TOH Processor block, associated with channel N.
		Alle	0 – De Scrambling is enabled.
		10 he	1 De-Scrambling is disabled.
3	Unused	R/O	
2	REI-L Error	7 R/W	REI-L Error Type:
	Type	3/1	This READ/WRITE bit-field permits the user to specify how the "Receive Transport REI-L Error Count" register is incremented.
			0 – Configures the Receive STS-1 TOH Processor block to count REI-L Bit Errors.
			In this case the "Receive Transport REI-L Error Count" register will be incremented by the value of the lower nibble within the M0/M1 byte.
			1 – Configures the Receive STS-1 TOH Processor block to count REI-L Frame Errors.
			In this case the "Receive Transport REI-L Error Count" register will be incremented each time the Receive STS-1 TOH Processor block receives a "non-zero" M0/M1 byte.
1	B2 Error	R/W	B2 Error Type:
	Type		This READ/WRITE bit-field permits the user to specify how the "Receive

EXAR

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

		,			
		Transport B2 Error Count" register is incremented.			
		0 - Configures the Receive STS-1 TOH Processor block to count B2 bit errors.			
		In this case, the "Receive Transport B2 Error Count" register will be incremented by the number of bits, within the B2 value, that is in error.			
		1 – Configures the Receive STS-1 TOH Processor block to count B2 frame errors.			
		In this case, the "Receive Transport B2 Error Count" register will be incremented by the number of erred STS-1 frames.			
B1 Error	R/W	B1 Error Type:			
Туре		This READ/WRITE bit-field permits the user to specify how the "Receive Transport B1 Error Count" register is incremented.			
		0 - Configures the Receive STS-1 TOH Processor block to count B1 bit errors.			
		In this case, the "Receive Transport B1 Error Count" register will be incremented by the number of bits, within the B1 value, that is in error.			
		1 - Configures the Receive STS-1 TOH Processor block to count B2 bit errors.			
		In this case, the "Receive Transport B1 Error Count" register will be incremented by the number of erred STS-1 frames.			
In this case, the "Receive Transport B1 Error Count" register will be incremented by the number of erred STS-1 frames.					
	Туре	Туре			

Table 479: Receive STS-1 Transport Status Register – Byte 1 (Address Location= 0xN106)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Unused	J0 Message Mismatch	J0 Message Unstable	AIS_L Detected		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	Description
7 – 3	Unused	R/O	
2	J0 Message Mismatch	R/O	J0 – Section Trace Mismatch Indicator: This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring the Section Trace Mismatch condition. The Receive STS-1 TOH Processor block will declare a J0 (Section Trace) Mismatch condition, whenever it accepts a J0 Message that differs from the "Expected J0 Message". 0 – Section Trace Mismatch Condition is NOT declared. 1 – Section Trace Mismatch Condition is currently declared.
1	J0 Message Unstable	R/O	J0 – Section Trace Unstable Indicator: This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring the Section Trace Instability condition. The Receive STS-1 TOH Processor block will declare a J0 (Section Trace) Unstable condition, whenever the "J0 Unstable" counter reaches the value 8. The "J0 Unstable" counter will be incremented for each time that it receives a J0 message that differs from the "Expected J0 Message". The "J0 Unstable" counter is cleared to "0" whenever the Receive STS-3 TOH Processor block has received a given J0 Message 3 (or 5) consecutive times. Note: Receiving a given J0 Message 3 (or 5) consecutive times also sets this bit-field to "0". 1 – Section Trace Instability condition is NOT declared.
0	AIS_L Detected	R/O	This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently detecting an AIS-L (Line AIS) pattern in the incoming STS-1 data stream. AIS-L is declared if bits 6, 7 and 8 (e.g., the Least Significant Bits, within the K2 byte) value the value "1, 1, 1" for five consecutive STS-1 frames. 0 – AIS-L is NOT currently declared. 1 – AIS-L is currently being declared.

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 480: Receive STS-1 Transport Status Register – Byte 0 (Address Location = 0xN107)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
RDI-L	S1 Unstable	APS	SF	SD	LOF	SEF	LOS
Declared		Unstable	Detected	Detected	Defect	Defect	Defect
					Detected	Declared	Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	RDI-L Declared	R/O	RDI-L Indicator: This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is detecting a Line-Remote Defect Indicator, in the incoming STS-1 signal. RDI-L is declared when bits 6, 7 and 8 (e.g., the three least significant bits) of the K2 byte contains the "1, 1, 0" pattern in 5 consecutive STS-1 frames. 0 – RDI-L is NOT being declared.
6	S1 Unstable	R/O	S1 Unstable Condition: This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring the "S1 Byte Instability" condition. The Receive STS-1 TOH Processor block will declare an "S1 Byte Instability" condition whenever the "S1 Byte Unstable Counter" reaches the value 32. The "S1 Byte Unstable Counter" is incremented for each time that the Receive STS-1 TOH Processor block receives an S1 byte that differs from the previously received S1 byte. The "S1 Byte Unstable Counter" is cleared to "0" when the same S1 byte is received for 8 consecutive STS-1 frames. Note: Receiving a given S1 byte, in 8 consecutive STS-1 frames also sets this bit-field to "0". 0 S1 Instability Condition is NOT declared.
5	APS Unstable	RO	APS (K1, K2 Byte) Instability: This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring the "K1, K2 Byte Unstable" condition. The Receive STS-1 TOH Processor block will declare a "K1, K2 Byte Unstable" condition whenever the Receive STS-1 TOH Processor block fails to receive the same set of K1, K2 bytes, in 12 consecutive STS-1 frames. The "K1, K2 Byte Instability" condition is cleared whenever the STS-1 Receiver receives a given set of K1, K2 byte values in three consecutive STS-1 frames. 0 – K1, K2 Instability Condition is NOT declared. 1 – K1, K2 Instability Condition is currently declared.
4	SF Detected	R/O	SF (Signal Failure) Defect Indicator: This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring the SF defect. The SF defect is declared when the number of B2 errors observed over a given time interval exceeds a certain threshold. 0 – SF Defect is NOT being declared. This bit is set to "0" when the number of B2 errors (accumulated over a given

		I	
			interval of time) does not exceed the "SF Declaration" threshold.
			1 – SF Defect is being declared.
			This bit is set to "1" when the number of B2 errors (accumulated over a given interval of time) does exceed the "SF Declaration" threshold.
3	SD Detected	R/O	SD (Signal Degrade) Defect Indicator:
			This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring the SD defect. The SD defect is declared when the number of B2 errors observed over a given time interval exceeds a certain threshold.
			0 – SD Defect is NOT being declared.
			This bit is set to "0" when the number of B2 errors (accumulated over a given interval of time) does not exceed the "SD Declaration" threshold.
			1 – SD Defect is being declared. 🎺 👌
			This bit is set to "1" when the number of B2 errors (accumulated over a given interval of time) does exceed the "SD Declaration" threshold.
2	LOF	R/O	LOF (Loss of Frame) Indicator:
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring the LOF defect. The Receive STS-1 TOH Processor block will declare the LOF defect if it has been declaring the SEF condition for 24 consecutive STS-1 frame periods. Once the LOF defect is declared, then the Receive STS-1 TOH Processor block will clear the LOF defect if it has not been declaring the SEF condition for 3ms (or 24 consecutive STS-1 frame periods).
			 0 - The Receive STS-1 TOH Processor block is NOT currently declaring the LOF condition. 1 - The Receive STS-1 TOH Processor block is currently declaring the LOF condition.
1	SEF	R/O	SEF (Severely Errored Frame):
	Defect Declared	roduct	This READ ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring an SEF condition. The Receive STS-1 TOH Processor block will declare an SEF condition if it detects Framing Alignment byte errors in four consecutive STS-1 frames. Once the SEF condition is declared the Receive STS-1 TOH Processor block will clear the SEF condition if it detects two consecutive STS-1 frames with un-erred framing alignment bytes.
	1,9	9,19,	0 – Indicates that the Receive STS-1 TOH Processor block is NOT declaring the SEF condition.
		♂	1 – Indicates that the Receive STS-1 TOH Processor block is currently declaring the SEF condition.
0	LOS	R/O	LOS (Loss of Signal) Indicator:
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive STS-1 TOH Processor block is currently declaring an LOS (Loss of Signal) condition. The Receive STS-1 TOH Processor block will declare an LOS condition if it detects "LOS_THRESHOLD[15:0]" consecutive "All Zero" bytes in the incoming STS-1 data stream.
			Note: The user can set the "LOS_THRESHOLD[15:0]" value by writing the appropriate data into the "Receive STS-1 Transport – LOS Threshold Value" Register (Address Location= 0xN12E and 0xN12F).
			0 - Indicates that the Receive STS-1 TOH Processor block is NOT currently

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

declaring an LOS condition.				
1 – Indicates that the Receive STS-1 TOH Processor block is currently declaring an LOS condition.				

The product are no longered (OBS)

The product are no longered (OBS)

The product are no be ordered (OBS)

Table 481: Receive STS-1 Transport Interrupt Status Register – Byte 2 (Address Location= 0xN109)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused						Change of RDI-L Interrupt Status
R/O	R/O	R/O	R/O	R/O	R/O	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 2	Unused	R/O	
1	Change of AIS-L Interrupt Status	RUR	Change of AIS-L (Line AIS) Condition Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change of AIS-L Condition" interrupt has occurred since the last read of this register. 0 – The "Change of AIS-L Condition" interrupt has not occurred since the last read of this register. 1 – The "Change of AIS-L Condition" interrupt has occurred since the last read of this register. Note: The user can obtain the current state of AIS-L by reading the contents of Bit 0 (AIS-L Defect Declared) within the "Receive STS-1 Transport Status Register – Byte 1" (Address Location= 0xN106).
0	Change of RDI-L Interrupt Status	RUR	Change of RDI-L (Line - Remote Defect Indicator) Condition Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change of RDI-L Condition" interrupt has occurred since the last read of this register. 0 - The "Change of RDI-L Condition" interrupt has not occurred since the last read of this register. 1 - The "Change of RDI-L Condition" interrupt has occurred since the last read of this register. 1 - The "Change of RDI-L Condition" interrupt has occurred since the last read of this register. 1 - The "Change of RDI-L Condition" interrupt has occurred since the last read of this register. 1 - The "Change of RDI-L Condition" interrupt has occurred since the last read of this register. 1 - The "Change of RDI-L Condition" interrupt has occurred since the last read of this register. 1 - The "Change of RDI-L Condition" interrupt has occurred since the last read of this register. 2 - The "Change of RDI-L Condition" interrupt has occurred since the last read of this register. 3 - The "Change of RDI-L Condition" interrupt has occurred since the last read of this register. 4 - The "Change of RDI-L Condition" interrupt has occurred since the last read of this register. 5 - The user can obtain the current state of RDI-L by reading out the state of Bit 7 (RDI-L Declared) within the "Receive STS-1 Transport Status Register - Byte 0" (Address Location=0xN107).

Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 482: Receive STS-1 Transport Interrupt Status Register – Byte 1 (Address Location= 0xN10A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
New S1 Byte Interrupt Status	Change in S1 Unstable State Interrupt Status	Change in J0 Unstable State Interrupt Status	New J0 Message Interrupt Status	J0 Mismatch Interrupt Status	Unused	Change in APS Unstable State Interrupt Status	NEW K1K2 Byte Interrupt Status
RUR	RUR	RUR	RUR	RUR	R/O	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	Description
7	New S1 Byte Value Interrupt Status	RUR	New S1 Byte Value Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "New S1 Byte Value" Interrupt has occurred since the last read of this register. 0 – Indicates that the "New S1 Byte Value" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "New S1 Byte Value" interrupt has occurred since the last read of this register. Note: The user can obtain the value for this most recently accepted value of the S1 byte by reading the "Receive STS-1 Transport S1 Value" register (Address Location= 0xN127).
6	Change in S1 Byte Unstable State Interrupt Status Change in J0 Message Unstable State Interrupt	RUR	Change in S1 Byte Unstable State – Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change in S1 Byte Unstable State" Interrupt has occurred since the last read of this register. Indicates that the "Change in S1 Byte Unstable State" Interrupt has occurred since the last read of this register. I – Indicates that the "Change in S1 Byte Unstable State" Interrupt has not occurred since the last read of this register. Note: The user can obtain the current "S1 Unstable" state by reading the contents of Bit 6 (S1 Unstable) within the "Receive STS-1 Transport Status Register – Byte 0" (Address Location= 0xN107).
5	Change in J0 Message Unstable State Interrupt Status	RUR	Change of J0 (Section Trace) Message Unstable condition – Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change of J0 (Section Trace) Message Instability" condition interrupt has occurred since the last read of this register. 0 – Indicates that the "Change of J0 (Section Trace) Message Instability" condition interrupt has not occurred since the last read of this register. 1 – Indicates that the "Change of J0 (Section Trace) Message Instability" condition interrupt has occurred since the last read of this register.
4	New J0 Message Interrupt Status	RUR	New J0 Trace Message Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the

_			
			"New J0 Trace Message" interrupt has occurred since the last read of this register.
			0 – Indicates that the "New J0 Trace Message Interrupt" has not occurred since the last read of this register.
			1 – Indicates that the "New J0 Trace Message Interrupt" has occurred since the last read of this register.
			Note: The user can read out the contents of the "Receive J0 Trace Buffer", which is located at Address Locations 0xN300 through 0xN33F.
3	J0 Mismatch Interrupt Status	RUR	Change in J0 – Section Trace Mismatch Condition" Interrupt Status:
			This RESET-upon-READ bit-field indicates whether or not the "Change in J0 – Section Trace Mismatch Condition" interrupt has occurred since the last read of this register.
			0 – Indicates that the "Change in J0 – Section Trace Mismatch Condition" interrupt has not occurred since the last read of this register.
			1 – Indicates that the "Change in J0 – Section Trace Mismatch Condition" interrupt has occurred since the last read of this register.
			Note: The user can determine whether the "J0 – Section Trace Mismatch" condition is "cleared" or "declared" by reading the state of Bit 2 (J0_MIS) within the "Receive STS-1 Transport Status Register – Byte 1 (Address Location= 0xN106).
2	Unused	R/O	9,4
1	Change in APS Unstable State Interrupt Status	RUR	Change of APS (K1, K2 Byte) Instability Condition – Interrupt Status:
	Change in APS Unstable State Interrupt Status	Me ve	This RESET-upon-READ bit-field indicates whether or not the Change of APS (K1, K2 Byte) Instability Condition" interrupt has occurred since the last read of this register.
	orodine di	ynot	0 – Indicates that the "Change of APS (K1, K2 Byte) Instability Condition" interrupt has NOT occurred since the last read of this register.
	The data nd m		1 – Indicates that the "Change of APS (K1, K2 Byte) Instability Condition" interrupt has occurred since the last read of this register.
	A.		Note: The user can determine whether the "K1, K2 Instability Condition" is being declared or cleared by reading out the contents of Bit 5 (APS_INV), within the "Receive STS-1 Transport Status Register – Byte 0" (Address Location= 0xN107).
0	New K1K2 Byte Interrupt	RUR	New K1, K2 Byte Value Interrupt Status:
	Status		This RESET-upon-READ bit-field indicates whether or not the "New K1, K2 Byte Value" Interrupt has occurred since the last read of this register.
			0 - Indicates that the "New K1, K2 Byte Value" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "New K1, K2 Byte Value" Interrupt has occurred since the last read of this register.
			Note: The user can obtain the contents of the new K1 byte by

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

reading out the contents of the "Receive STS-1 Transport K1 Value" Register (Address Location= 0xN11F). Further, the user can also obtain the contents of the new K2 byte by reading out the contents of the "Receive STS-1 Transport K2 Value"
Register (Address Location= 0xN123).

The product of products in the product of products in the product of products in the product of the product of

Table 483: Receive STS-1 Transport Interrupt Status Register – Byte 0 (Address Location= 0xN10B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Change of SF Condition Interrupt Status	Change of SD Condition Interrupt Status	Detection of REI-L Error Interrupt Status	Detection of B2 Error Interrupt Status	Detection of B1 Error Interrupt Status	Change of LOF Condition Interrupt Status	Change of SEF Interrupt Status	Change of LOS Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7	Change of SF	RUR	Change of Signal Failure (SF) Condition Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of SF Interrupt" has occurred since the last read of this register.
			0 - The "Change of SF Condition Interrupt" has NOT occurred since the last read of this register.
			1 – The "Change of SF Condition Interrupt" has occurred since the last read of this register.
			Note: The user can determine the current "SF" condition by reading out the state of Bit 4(SF Declared) within the "Receive STS-1 Transport Status Register – Byte 0 (Address Location= 0xN107).
6	Change of SD Condition	RUR	Change of Signal Degrade (SD) Condition Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of SD Condition Interrupt" has occurred since the last read of this register.
			0 - The "Change of SD Condition Interrupt" has NOT occurred since the last read of this register.
		ري.	1 – The "Change of SD Condition Interrupt" has occurred since the last read of this register.
	of	odule	Note: The user can determine the current "SD" condition by reading out the state of Bit 3 (SD Declared) within the "Receive STS-1 Transport Status Register – Byte 0 (Address Location= 0xN107).
5	Detection of	RUR	Detection of Line – Remote Error Indicator Interrupt Status:
	REI-L Interrupt Status	and	This RESET-upon-READ bit-field indicates whether or not the "Detection of Line – Remote Error Indicator" Interrupt has occurred since the last read of this register.
			0 - The "Detection of Line - Remote Error Indicator" Interrupt has NOT occurred since the last read of this register.
			1 – The "Detection of Line – Remote Error Indicator" Interrupt has occurred since the last read of this register.
4	Detection of B2	RUR	Detection of B2 Error Interrupt Status:
	Error Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of B2 Error Interrupt" has occurred since the last read of this register.
			0 - The "Detection of B2 Error Interrupt" has NOT occurred since the last read of this register.
			1- The "Detection of B2 Error Interrupt" has occurred since the last read of this register.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

3	Detection of B1	RUR	Detection of B1 Error Interrupt Status:				
	Error Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of B1 Error Interrupt" has occurred since the last read of this register.				
			$\bf 0$ - The "Detection of B1 Error Interrupt" has NOT occurred since the last read of this register.				
			1 - The "Detection of B1 Error Interrupt" has occurred since the last read of this register				
2	Change of LOF	RUR	Change of Loss of Frame (LOF) Condition Interrupt Status:				
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of LOF Condition" interrupt has occurred since the last read of this register.				
			0 – The "Change of LOF Condition" interrupt has NOT occurred since the last read of this register.				
			1 – The "Change of LOF Condition" interrupt has occurred since the last read of this register.				
			Note: The user can determine the current "LOF" condition by reading out the state of Bit 2 (LOF Defect Declared) within the "Receive STS-1 Transport Status Register – Byte 0 (Address Location= 0xN107).				
1	Change of SEF	RUR	Change of SEF Condition Interrupt Status:				
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of SEF Condition" Interrupt has occurred since the last read of this register.				
			0 – The "Change of SEF Condition" Interrupt has NOT occurred since the last read of this register				
			1 – The "Change of SEF Condition" Interrupt has occurred since the last read of this register.				
			Note: The user can determine the current "SEF" condition by reading out the state of Bit 1 (SEF Defect Declared) within the "Receive STS-1 Transport Status Register – Byte 0 (Address Location= 0xN107).				
0	Change of LOS	RUR	Change of Loss of Signal (LOS) Condition Interrupt Status:				
	Condition Interrupt Status	6	This RESET upon-READ bit-field indicates whether or not the "Change of LOS Condition" interrupt has occurred since the last read of this register.				
		, bio	The "Change of LOS Condition" Interrupt has NOT occurred since the last read of this register.				
	1/1/2	7313	1 The "Change of LOS Condition" Interrupt has occurred since the last rea of this register.				
			Note: The user can determine the current "LOS" status by reading out the contents of Bit 0 (LOS Defect Declared) within the Receive STS-1 Transport Status Register – Byte 0 (Address Location= 0xN107).				

Table 484: Receive STS-1 Transport Interrupt Enable Register – Byte 2 (Address Location= 0xN10D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Change of AIS-L Condition Interrupt Enable	Change of RDI-L Condition Interrupt Enable				
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 2	Unused	R/O	
1	Change of AIS-L Condition Interrupt Enable	R/W	Change of AIS-L (Line AIS) Condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change of AIS-L Condition" interrupt. If the user enables this interrupt, then the XRT94L33 device will generate an interrupt in response to either of the following conditions. • When the Receive STS-1 TOH Processor block declares the "AIS-L" condition. • When the STS-1 Receiver clears the "AIS-L" condition. 0 – Disables the "Change of AIS-L Condition" Interrupt. 1 – Enables the "Change of AIS-L Condition" Interrupt.
0	Change of RDI-L Condition Interrupt Enable	R/W	Change of RDI-L (Line Remote Defect Indicator) Condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change of RDI-L Condition" interrupt. If the user enables this interrupt, then the XRT94L33 device will generate an interrupt in response to either of the following conditions. When the Receive STS-1 TOH Processor block declares the "RDI-L" condition. When the Receive STS-1 TOH Processor clears the "RDI-L" condition. 0 – Disables the "Change of RDI-L Condition" Interrupt. 1 – Enables the "Change of RDI-L Condition" Interrupt.

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 485: Receive STS-1 Transport Interrupt Enable Register – Byte 1 (Address Location= 0xN10E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
New S1 Byte Interrupt Enable	Change in S1 Byte Unstable State Interrupt Enable	Change in J0 Message Unstable State Interrupt Enable	New J0 Message Interrupt Enable	J0 Mismatch Interrupt Enable	Unused	Change in APS Unstable State Interrupt Enable	New K1K2 Byte Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	New S1 Byte Value	R/W	New S1 Byte Value Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to enable or disable the "New S1 Byte Value" Interrupt. If the user enables this interrupt, then the Receive STS-1 TOH Processor block will generate this interrupt anytime it receives and accepts a new S1 byte value. The Receive STS-1 TOH Processor block will accept a new S1 byte after it has received it for 8 consecutive STS-1 frames.
			0 – Disables the "New \$1 Byte Value" Interrupt.
			1 – Enables the "New S1 Byte Value" Interrupt.
6	Change in S1	R/W	Change in S1 Byte Unstable State Interrupt Enable:
	Unstable State Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in \$1 Byte Unstable State" Interrupt. If the user enables this bit-field, then the Receive STS-1 TOH Processor block will generate an interrupt in response to either of the following conditions.
		1 4.	When the Receive STS-1 TOH Processor block declares the "S1 Byte Instability" condition.
		duc	When the Receive STS-1 TOH Processor block clears the "S1 Byte Instability" condition.
		6	0 - Disables the "Change in S1 Byte Unstable State" Interrupt.
	· · ·	6	Enables the "Change in S1 Byte Unstable State" Interrupt.
5	Change in J0 Message Unstable	R/W	Change of J0 (Section Trace) Message Instability condition Interrupt Enable:
	State Interrupt Enable	3	This READ/WRITE bit-field permits the user to either enable or disable the "Change of J0 Message Instability Condition" Interrupt. If the user enables this interrupt, then the Receive STS-1 TOH Processor block will generate an interrupt in response to either of the following conditions.
			Whenever the Receive STS-1 TOH Processor block declares the "Jo Message Instability" condition.
			Whenever the Receive STS-1 TOH Processor block clears the "Jo Message Instability" condition.
			0 – Disable the "Change of J0 Message Instability" Interrupt.
			1 – Enables the "Change of J0 Message Instability" Interrupt.
4	New J0 Message	R/W	New J0 Trace Message Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to enable or disable the "New J0 Trace Message" interrupt. If the user enables this interrupt, then the

			Receive STS-1 TOH Processor block will generate this interrupt anytime it receives and accepts a new J0 Trace Message. The Receive STS-1 TOH Processor block will accept a new J0 Trace Message after it has received it 3 (or 5) consecutive times. 0 – Disables the "New J0 Trace Message" Interrupt. 1 – Enables the "New J0 Trace Message" Interrupt.
3	J0 Mismatch Interrupt Enable	R/W	Change in "J0 - Section Trace Mismatch Condition" interrupt enable:
			This READ/WRITE bit-field permits the user to either enable or disable the "Change in J0 – Section Trace Mismatch condition" interrupt. If the user enables this interrupt, then the Receive STS-1 TOH Processor block will generate an interrupt in response to either of the following events.
			c. The Receive STS-1 TOH Processor block declares a "J0 – Section Trace Mismatch" condition.
			d. The Receive STS-1 TOH Processor block clears the "J0 – Section Trace Mismatch" condition.
			Note: The user can determine whether the "J0 – Section Trace Mismatch" condition is "cleared or "declared" by reading the state of Bit 2 (J0_MIS) within the "Receive STS-1 Transport Status Register - Byte 1 (Address Location= 0xN106).
2	Unused	R/O	endi
1	Change in APS	R/W	Change of APS (K1, K2 Byte) Instability Condition - Interrupt Enable:
	Unstable State Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of APS (K1, K2 Byte) Instability condition" interrupt. If the user enables this interrupt, then the Receive STS-1 TOH Processor block will generate an Interrupt in response to either of the following events.
			c. If the Receive STS-1 TOH Processor block declares a "K1, K2 Instability" condition.
		, ct. 0	d. If the Receive STS-1 TOH Processor block clears the "K1, K2 Instability" condition.
0	New K1K2 Byte Interrupt Enable	R/W	New K1, K2 Byte Value Interrupt Enable:
	The Tupt Eliable	dnay	This READ/WRITE bit-field permits the user to either enable or disable the "New K1, K2 Byte Value" Interrupt. If the user enables this interrupt, then the Receive STS-1 TOH Processor block will generate this interrupt anytime it receives and accepts a new K1, K2 byte value. The Receive STS-1 TOH Processor block will accept a new K1, K2 byte value, after it has received it within 3 (or 5) consecutive STS-1 frames.
	•		0 – Disables the "New K1, K2 Byte Value" Interrupt.
			1 – Enables the "New K1, K2 Byte Value" Interrupt.



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 486: Receive STS-1Transport Interrupt Status Register – Byte 0 (Address Location= 0xN10F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Change of SF Condition Interrupt Enable	Change of SD Condition Interrupt Enable	Detection of REI-L Error Interrupt Enable	Detection of B2 Error Interrupt Enable	Detection of B1 Error Interrupt Enable	Change of LOF Condition Interrupt Enable	Change of SEF Condition Interrupt Enable	Change of LOS Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7	Change of SF	R/W	Change of Signal Failure (SF) Condition Interrupt Enable:
	Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of Signal Failure (SF) Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 device will generate an interrupt anytime the Receive STS-1 TOH Processor block detects an SF condition.
			0 – Disables the "Change of SF Condition Interrupt".
			1 – Enables the "Change of SF Condition Interrupt".
6	Change of SD	R/W	Change of Signal Degrade (SD) Condition Interrupt Enable:
	Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of Signal Degrade (SD) Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 device will generate an interrupt anytime the Receive STS-170H Processor block detects an SD condition.
			0 – Disables the "Change of SD Condition Interrupt".
			1 – Enables the "Change of SD Condition Interrupt".
5	Detection of	R/W	Detection of Line – Remote Error Indicator Interrupt Enable:
	REI-L Interrupt Enable	odu	This READWRITE bit-field permits the user to either enable or disable the "Detection of Line – Remote Error Indicator" interrupt. If the user enables this interrupt, then the XRT94L33 device will generate an interrupt anytime the Receive STS-1 TOH Processor block detects an REI-L condition.
		6. 9	0 Disables the "Line - Remote Error Indicator" Interrupt.
	11/2	NO.	Enables the "Line – Remote Error Indicator" Interrupt.
4	Detection of B2	R/W	Detection of B2 Error Interrupt Enable:
	Error Interrupt Enable	&	This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B2 Error" Interrupt. If the user enables this interrupt, then the XRT94L33 device will generate an interrupt anytime the Receive STS-1 TOH Processor block detects a B2 error.
			0 – Disables the "Detection of B2 Error Interrupt".
			1 – Enables the "Detection of B2 Error Interrupt".
3	Detection of B1	R/W	Detection of B1 Error Interrupt Enable:
	Error Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B1 Error" Interrupt. If the user enables this interrupt, then the XRT94L33 device will generate an interrupt anytime the Receive STS-1 TOH Processor block detects a B1 error.
			0 – Disables the "Detection of B1 Error Interrupt".
			1 – Enables the "Detection of B1 Error Interrupt".

Change of LOF	R/W	Change of Loss of Frame (LOF) Condition Interrupt Enable:
Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of LOF Condition" interrupt. If the user enables this interrupt, then the XRT94L33 device will generate an interrupt in response to either of the following conditions.
		• When the Receive STS-1 TOH Processor block declares the "LOF" condition.
		• When the Receive STS-1 TOH Processor block clears the "LOF" condition.
		0 – Disables the "Change of LOF Condition Interrupt.
		1 – Enables the "Change of LOF Condition" Interrupt.
Change of SEF	R/W	Change of SEF Condition Interrupt Enable:
Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of SEF Condition" Interrupt. If the user enables this interrupt, then the XRT94L33 device will generate an interrupt in response to either of the following conditions.
		When the Receive STS-1 TOH Processor block declares the "SEF" condition.
		When the Receive STS-1 TOH Processor block clears the "SEF" condition.
		0 – Disables the "Change of SEF Condition Interrupt".
		1 – Enables the "Change of SEF Condition Interrupt".
Change of LOS	R/W	Change of Loss of Signal (LOS) Condition Interrupt Enable:
Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of LOF Condition" interrupt. If the user enables this interrupt, then the XRT94L33 device will generate an interrupt in response to either of the following conditions.
	ici	• When the Receive STS-1 TOH Processor block declares the "LOF" condition.
4	odicet	When the Receive STS-1 TOH Processor block clears the "LOF" condition.
6	5 0	0 – Disables the "Change of LOF Condition Interrupt.
The	s W.	1 – Enables the "Change of LOF Condition" Interrupt.
	Change of SEF Condition Interrupt Enable Change of LOS Condition Interrupt Enable	Condition Interrupt Enable Change of SEF Condition Interrupt Enable Change of LOS Condition R/W

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 487: Receive STS-1 Transport – B1 Error Count Register – Byte 3 (Address Location= 0xN110)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
B1_Error_Count[31:24]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	B1_Error_Count[31:24]	RUR	B1 Error Count – MSB:
			This RESET-upon-READ register, along with "Receive Transport – B1 Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a B1 byte error. Note: 1. If the B1 Error Type is configured to be "bit errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of bits, within the B1 value that are in error 2. If the B1 Error Type is configured to be "frame errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B1 bytes.

Table 488: Receive STS-1 Transport – B1 Error Count Register – Byte 2 (Address Location= 0xN111)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 2	Віт 1	Віт 0		
B1_Error_Count[23:16]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0,00,00	0	0	0		

BIT NUMBER	NAME	YPE	DESCRIPTION
7 - 0	B1_Error_Count[23:16] R	RUR	B1 Error Count (Bits 23 through 16):
	the basing his	87	This RESET-upon-READ register, along with "Receive Transport – B1 Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a B1 byte error.
	'		Note:
			1. If the B1 Error Type is configured to be "bit errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of bits, within the B1 value that are in error.
			2. If the B1 Error Type is configured to be "frame errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B1 bytes.

Table 489: Receive STS-1 Transport – B1 Error Count Register – Byte 1 (Address Location= 0xN112)

	Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
--	-------	-------	-------	-------	-------	-------	-------	-------

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

	B1_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	B1_Error_Count[15:8]	RUR	B1 Error Count – (Bits 15 through 8)
			This RESET-upon-READ register, along with "Receive Transport – B1 Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a B1 byte error.
			Note:
			1. If the B1 Error Type is configured to be "bit errors", then the Receive STS-1 TOH Processor, block will increment this 32 bit counter by the number of bits, within the B1 value that are in error
			2. If the B1 Error Type is configured to be "frame errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B1 bytes.

Table 490: Receive STS-1 Transport – B1 Error Count Register – Byte 0 (Address Location= 0xN113)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
			B1_Error_	Count[7:0]					
RUR	RUR	RUR	RUR 0	RUR	RUR	RUR	RUR		
0	0	0	000	0	0	0	0		
	Oly 10 Yell								

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B1_Error_Count[7:0]	RUR	B1 Error Count – LSB:
	Producet a	not	This RESET-upon-READ register, along with "Receive Transport – B1 Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a B1 byte error.
	The to We		Note:
	y gand		1. If the B1 Error Type is configured to be "bit errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of bits, within the B1 value that are in error.
			2. If the B1 Error Type is configured to be "frame errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B1 bytes.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 491: Receive STS-1 Transport – B2 Error Count Register – Byte 3 (Address Location= 0xN114)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
B2_Error_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	B2_Error_Count[31:24]	RUR	B2 Error Count – MSB:
			This RESET-upon-READ register, along with "Receive STS-1 Transport – B2 Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a B2 byte error. Note: 1. If the B2 Error Type is configured to be "bit errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of bits, within the B2 value that are in error. 2. If the B2 Error Type is configured to be "frame errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B2 bytes.

Table 492: Receive STS-1 Transport – B2 Error Count Register – Byte 2 (Address Location= 0xN115)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 2	Віт 1	Віт 0	
B2_Error_Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0 00 0	0	0	0	

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	B2_Error_Count[23:16]	RUR	B2 Error Count (Bits 23 through 16):
	The bata	Lay	This RESET-upon-READ register, along with "Receive Transport – B2 Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a B2 byte error.
	'		Note:
			1. If the B2 Error Type is configured to be "bit errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of bits, within the B2 value that are in error.
			2. If the B2 Error Type is configured to be "frame errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B2 bytes.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 493: Receive STS-1 Transport – B2 Error Count Register – Byte 1 (Address Location= 0xN116)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
B2_Error_Count[15:8]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	B2_Error_Count[15:8]	RUR	B2 Error Count – (Bits 15 through 8)
			This RESET-upon-READ register, along with "Receive Transport – B2 Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a B2 byte error. Note: 1. If the B2 Error Type is configured to be "bit errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of bits, within the B2 value that are in error. 2. If the B2 Error Type is configured to be "frame errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B2 bytes.

Table 494: Receive STS-1 Transport – B2 Error Count Register – Byte 0 (Address Location= 0xN117)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0
B2_Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0 (0	000	0	0	0	0

BIT NUMBER	Name	TXPE	DESCRIPTION
7 - 0	B2_Error_Count[7:0]	RUR	B2 Error Count – LSB:
	The Hatas	May	This RESET-upon-READ register, along with "Receive Transport – B2 Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a B2 byte error.
	'0 '		Note:
			1. If the B2 Error Type is configured to be "bit errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of bits, within the B2 value that are in error.
			2. If the B2 Error Type is configured to be "frame errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of frames that contain erred B2 bytes.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 495: Receive STS-1 Transport - REI-L Error Count Register - Byte 3 (Address Location = 0xN118)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
REI_L_Error_Count[31:24]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	REI_L_Error_Count[31:24]	RUR	REI-L Error Count – MSB:
			This RESET-upon-READ register, along with "Receive Transport – REI-L Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a Line - Remote Error Indicator.
			Note: 1. If the REI-L Error Type is configured to be "bit errors", then the Receive STS-1 TOP Processor block will increment this 32 bit
			counter by the nibble-value within the REI-L field of the M0 byte.
			2. If the REI-L Error Type is configured to be "frame errors", then the Receive STS-1 TOH Processor block will increment this 32 bit
			counter by the number of frames that contain non-zero REI-L values.

Table 496: Receive STS-1 Transport – REI 1 Error Count Register – Byte 2 (Address Location= 0xN119)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	REI_L_Erro Count[23:16]						
RUR	RUR	RUR 💍	RUR	RUR	RUR	RUR	RUR
0	0	0 👋	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	REI_L_Error_Count[23:16]	RUR	REI-L Error Count (Bits 23 through 16):
	o and		This RESET-upon-READ register, along with "Receive Transport – REI-L Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a Line – Remote Error Indicator.
			Note:
			1. If the REI-L Error Type is configured to be "bit errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the nibble-value within the REI-L field of the M0 byte.
			2. If the REI-L Error Type is configured to be "frame errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of frames that contain non-zero REI-L values.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 497: Receive STS-1 Transport - REI_L Error Count Register - Byte 1 (Address Location= 0xN11A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			REI_L_Error	_Count[15:8]			
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	REI_L_Error_Count[15:8]	RUR	REI-L Error Count – (Bits 15 through 8)
			This RESET-upon-READ register, along with "Receive Transport – REI-L Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a Line – Remote Error Indicator.
			Note:
			1. If the REI-L Error Type is configured to be "bit errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the nibble-value within the REI-L field of the M0 byte.
			2. If the REI-L Error Type is configured to be "frame errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of frames that contain non-zero REI-L values.

Table 498: Receive STS-1 Transport - REI_L Error Count Register - Byte 0 (Address Location= 0xN11B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	REI_L(Error_Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	
	NO NEE NO							

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	REI_L_Error_Count[7:0]	RUR	REI-L Error Count – LSB:
	o sho		This RESET-upon-READ register, along with "Receive Transport – REI-L Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STS-1 TOH Processor block detects a Line – Remote Error Indicator.
			Note:
			1. If the REI-L Error Type is configured to be "bit errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the nibble-value within the REI-L field of the M0 byte.
			2. If the REI-L Error Type is configured to be "frame errors", then the Receive STS-1 TOH Processor block will increment this 32 bit counter by the number of frames that contain non-zero REI-L values.

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 499: Receive STS-1 Transport – Received K1 Byte Value (Address Location= 0xN11F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Filtered_K1_Value[7:0]						
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Filtered_K1_Value[7:0]	R/O	Filtered/Accepted K1 Value:
			These READ-ONLY bit-fields contain the value of the most recently "filtered" K1 value, that the Receive STS-1 TOH Processor block has received. These bit-fields are valid if the K1/K2 pair (to which it belongs) has been received for 3 consecutive STS-1 frames. This register should be polled by Software in order to determine various APS codes.

Table 500: Receive STS-1Transport – Received K2 Byte Value (Address Location= 0xN123)

Віт 7	Віт 6	Віт 5	Віт 4	Brt 3	Віт 2	Віт 1	Віт 0
			Filtered_K2	_Value[7:0]			
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	9,0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Filtered_K2_Value[7:0]	R/O	Filtered/Accepted K2 Value:
	o pro	district of the state of the st	These READ-ONLY bit-fields contain the value of the most recently "filtered" K2 value, that the Receive STS-1 TOH Processor block has received. These bit-fields are valid if the K1/K2 pair (to which it belongs) has been received for 3 consecutive STS-1 frames. This register should be polled by Software in order to determine various APS codes.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 501: Receive STS-1 Transport - Received S1 Byte Value (Address Location= 0xN127)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			Filtered_S1	_Value[7:0]			
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Filtered_S1_Value[7:0]	R/O	Filtered/Accepted S1 Value:
			These READ-ONLY bit-fields contain the value of the most recently "filtered" S1 value that the Receive STS-1 TOH Processor block has received. These bit-fields are valid if it has been received for 8 consecutive STS-1 frames.

Table 502: Receive STS-1 Transport – LOS Threshold Value MSB (Address Location= 0xN12E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			LOS_THRES	SHOLD[15:8]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1 🔇	1	1	1	1

BIT NUMBER	Name	TYPE	DESCRIPTION
7 - 0	LOS_THRESHOLD[15:8]	R/W	LOS Threshold Value – MSB:
	uct or p	he ho	These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – LOS Threshold Value – LSB" register specify the number of consecutive (All Zero) bytes that the Receive STS-1 TOH Processor block must detect before it can declare an LOS condition.
	The produces in)*	

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 503: Receive STS-1 Transport – LOS Threshold Value - LSB (Address Location= 0xN12F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			LOS_THRE	SHOLD[7:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	Name	TYPE	DESCRIPTION
7 - 0	LOS_THRESHOLD[7:0]	R/W	LOS Threshold Value – LSB:
			These READ/WRITE bits, along the contents of the "Receive STS-1Transport – LOS Threshold Value – MSB" register specify the number of consecutive (All Zero) bytes that the Receive STS-1 TOH Processor block must detect before it can declare an LOS condition.

Table 504: Receive STS-1 Transport – Receive SF SET Monitor Interval – Byte 2 (Address Location= 0xN131)

					- 1/ V		
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
SF_SET_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	5/000	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_SET_MONITOR_WINDOW[23:1	R/W	SF_SET_MONITOR_INTERVAL - MSB:
	The product of and may not and and may not	pe of	These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF SET Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the number of STS-1 Frame periods that will constitute a SET Sub-Interval for SF (Signal Failure). When the Receive STS-1 TOH Processor block is checking for SF, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors exceeds that of programmed into the "Receive Transport SF SET Threshold" register, then an SF condition will be declared.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 505: Receive STS-1 Transport – Receive SF SET Monitor Interval – Byte 1 (Address Location= 0xN132)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	SF_SET_MONITOR_WINDOW[15:8]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SF_SET_MONITOR_WINDOW[15:8]	R/W	SF_SET_MONITOR_INTERVAL (Bits 15 through 8):
		net	These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF SET Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the number of STS-1 Frame periods that will constitute a SET Sub-Interval for SF (Signal Failure). When the Receive STS-1 TOH Processor block is checking for SF, it will accumulate B2 bit errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 bit errors exceeds that of programmed into the "Receive STS-1 Transport SF SET Threshold" register, then an SF condition will be declared.

Table 506: Receive STS-1 Transport – Receive SF SET Monitor Interval – Byte 0 (Address Location= 0xN133)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0
		S	F_SET_MONITO	DR_WINDOW[7	:0]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	10		1	1	1	1

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SF_SET_MONITOR_WINDOW[7:0	R/W	SF_SET_MONITOR_INTERVAL - LSB:
	1, 93 ug		These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF SET Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the number of STS-1 Frame periods that will constitute a SET Sub-Interval for SF (Signal Failure).
			When the Receive STS-1 TOH Processor block is checking for SF, it will accumulate B2 bit errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 bit errors exceeds that of programmed into the "Receive STS-1 Transport SF SET Threshold" register, then an SF condition will be declared.

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 507: Receive STS-1 Transport - Receive SF SET Threshold - Byte 1 (Address Location= 0xN136)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
SF_SET_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SF_SET_THRESHOLD[15:8]	R/W	SF_SET_THRESHOLD - MSB:
			These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF SET Threshold – Byte 0" registers permit the user to specify the number of B2 bit errors that will cause the Receive STS-1 TOH Processor block to declare an SF (Signal Failure) condition. When the Receive STS-1 TOH Processor block is checking for SF, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors exceeds that of programmed into this and the "Receive STS-1 Transport SF SET Threshold – Byte 0" register, then an SF condition will be declared.

Table 508: Receive STS-1 Transport - Receive SF SET Threshold - Byte 0 (Address Location= 0xN137)

Віт 7	Віт 6	Віт 5	Віт 4	Bit 3	Віт 2	Віт 1	Віт 0
SF_SET_THRESHOLD[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1, 0,	1	1	1	1
	"ic, al be						

BIT NUMBER	NAME TYPE	Description
7 - 0	SF_SET_THRESHOLD[7:0] R/W	DESCRIPTION SF_SET_THRESHOLD – LSB: These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF SET Threshold – Byte 1" registers permit the user to specify the number of B2 bit errors that will cause the Receive STS-1 TOH Processor block to declare an SF (Signal Failure) condition.
		When the Receive STS-1 TOH Processor block is checking for SF, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors exceeds that of programmed into this and the "Receive STS-1 Transport SF SET Threshold – Byte 1" register, then an SF condition will be declared.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 509: Receive STS-1 Transport – Receive SF CLEAR Threshold – Byte 1 (Address Location= 0xN13A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SF_CLEAR_THRESHOLD[15:8]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SF_CLEAR_THRESHOLD	R/W	SF_CLEAR_THRESHOLD - MSB:
	[15:8]		These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF CLEAR Threshold – Byte 0" registers permit the user to specify the upper limit for the number of B2 bit errors that will cause the Receive STS-1 TOH Processor block to clear the SF (Signal Failure) condition. When the Receive STS-1 TOH Processor block is checking for clearing SF, it will accumulate B2 errors for a total of 8 CLEAR Sub-Interval periods. If the number of accumulated B2 errors is less than that programmed into this and the "Receive STS-1 Transport SF CLEAR Threshold – Byte 0" register, then an SF condition will be cleared.

Table 510: Receive STS-1 Transport - Receive SF CLEAR Threshold - Byte 0 (Address Location= 0xN13B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			SF_CLEAR_TH	RESHOLD[7:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	,0 b	1	1	1	1
	AUC A A LIVE						

BIT NUMBER	NAME	ТҮРЕ	DESCRIPTION
7 - 0	SF_CLEAR_THRESHOLD	R/W	SF_CLEAR_THRESHOLD - LSB:
	They of the		These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF CLEAR Threshold – Byte 1" registers permit the user to specify the upper limit for the number of B2 bit errors that will cause the Receive STS-1 TOH Processor block to clear the SF (Signal Failure) condition.
			When the Receive STS-1 TOH Processor block is checking for clearing SF, it will accumulate B2 errors for a total of 8 CLEAR Sub-Interval periods. If the number of accumulated B2 errors is less than that programmed into this and the "Receive STS-1 Transport SF CLEAR Threshold – Byte 1" register, then an SF condition will be cleared.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 511: Receive STS-1 Transport – Receive SD Set Monitor Interval – Byte 2 (Address Location= 0xN13D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	SD_SET_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW [23:16]	R/W	SF_SET_MONITOR_INTERVAL – MSB: These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF SET Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the number of STS-1 Frame periods that will constitute a SET Sub-Interval for SD (Signal Degrade) declaration. When the Receive STS-1 TOH Processor block is checking for SD, it will accumulate B2 bit errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 bit errors exceeds that of programmed into the "Receive STS-1 Transport SD SET Threshold" register, then an SD condition will be declared.

Table 512: Receive STS-1 Transport – Receive SD Set Monitor Interval – Byte 1 (Address Location= 0xN13E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
SD_SET_MONITOR_WINDOW[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	.00 0	0	0	0	0
	Allo tal the						

BIT NUMBER	NAME O	YPE	DESCRIPTION
7-0	SD_SET_MONITOR_WINDOW \	R/W	SD_SET_MONITOR_INTERVAL – Bits 15 through 8:
	[15:8] data mid		These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SD SET Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the number of STS-1 Frame periods that will constitute a SET Sub-Interval for SD (Signal Degrade) declaration.
			When the Receive STS-1 TOH Processor block is checking for SD, it will accumulate B2 bit errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 bit errors exceeds that of programmed into the "Receive STS-1 Transport SD SET Threshold" register, then an SD condition will be declared.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 513: Receive STS-1 Transport – Receive SD Set Monitor Interval – Byte 0 (Address Location= 0xN13F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SD_SET_MONITOR_WINDOW[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION
7-0			SD_SET_MONITOR_INTERVAL – LSB: These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SD SET Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the number of STS-1 Frame periods that will constitute a SET Sub-Interval for SD (Signal Degrade) declaration.
			When the Receive STS-1 TOH Processor block is checking for SD, it will accumulate B2 bit errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 bit errors exceeds that of programmed into the "Receive STS-1 Transport SD SET Threshold" register, then an SD condition will be declared.

Table 514: Receive STS-1 Transport - Receive SD SET Threshold - Byte 1 (Address Location= 0xN142)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
			SD_SET_THR	SHOLD[15:8]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	.O 5.	1	1	1	1	
	Aug at at the							

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SD_SET_THRESHOLD[15.8] R/W		SD_SET_THRESHOLD – MSB: These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SD SET Threshold – Byte 0" registers permit the user to specify the number of B2 bit errors that will cause the Receive STS-1 TOH Processor block to declare an
			SD (Signal Degrade) condition. When the Receive STS-1 TOH Processor block is checking for SD, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors exceeds that of programmed into this and the "Receive STS-1 Transport SD SET Threshold – Byte 0" register, then an SD condition will be declared.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 515: Receive STS-1 Transport - Receive SD SET Threshold - Byte 0 (Address Location= 0xN143)

Віт 7	Віт 6	Віт 5	Віт 5 Віт 4		Віт 3 Віт 2		Віт 0	
SD_SET_THRESHOLD[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SD_SET_THRESHOLD[7:0]	R/W	SD_SET_THRESHOLD - LSB:
			These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SD SET Threshold – Byte 1" registers permit the user to specify the number of B2 bit errors that will cause the Receive STS-1 TOH Processor block to declare an SD (Signal Degrade) condition. When the Receive STS-1 TOH Processor block is checking for SD, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors exceeds that of programmed into this and the "Receive STS-1 Transport SD SET Threshold – Byte 1" register, then an SD condition will be declared.

Table 516: Receive STS-1 Transport – Receive SD CLEAR Threshold – Byte 1 (Address Location= 0xN146)

Віт 7	Віт 6	Віт 5	Віт4	Віт 3	Віт 2	Віт 1	Віт 0	
	SD_CLEAR_THRESHOLD[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	10 0	1	1	1	1	
	Auc. air be							

BIT NUMBER	NAME TYPE	DESCRIPTION
7 - 0	SD_CLEAR_THRESHOLD R/W	SD_CLEAR_THRESHOLD - MSB: These READ/WRITE bits, along the contents of the "Receive STS-1 Transport - SD CLEAR Threshold - Byte 0" registers
	alle	permit the user to specify the upper limit for the number of B2 bit errors that will cause the Receive STS-1 TOH Processor block to clear the SD (Signal Degrade) condition.
		When the Receive STS-1 TOH Processor block is checking for clearing SD, it will accumulate B2 errors for a total of 8 CLEAR Sub-Interval periods. If the number of accumulated B2 errors is less than that programmed into this and the "Receive STS-1 Transport SD CLEAR Threshold – Byte 0" register, then an SD condition will be cleared.

Table 517: Receive STS-1 Transport – Receive SD CLEAR Threshold – Byte 1 (Address Location= 0xN147)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SD_CLEAR_THRESHOLD[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SD_CLEAR_THRESHOLD[7:0]	R/W	SD_CLEAR_THRESHOLD - LSB:
			These READ/WRITE bits, along the contents of the "Receive STS-1 Transport - SD CLEAR Threshold - Byte 1" registers permit the user to specify the upper limit for the number of B2 bit errors that will cause the Receive STS-1 TOH Processor block to clear the SD (Signal Degrade) condition. When the Receive STS-1 TOH Processor block is checking for clearing SD, it will accumulate B2 errors for a total of 8 CLEAR Sub-Interval periods. If the number of accumulated B2 errors is less than that programmed into this and the "Receive STS-1 Transport SD CLEAR Threshold - Byte 1" register, then an SD condition will be cleared.

Table 518: Receive STS-1 Transport – Force SEF Condition Register (Address Location= 0xN14B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
			Unused	10			SEF FORCE	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W	
0	0	0	0 0	0	0	0	0	
	Auch alat pe							

BIT NUMBER	Name 🎸	TYPE	DESCRIPTION
7 – 1	Unused	<i>B</i> /O	
0	SEF FORCE	R/W	SEF Force:
	. 90	and	This READ/WRITE bit-field permits the user to force the Receive STS-1 TOH Processor block (within Channel N) to declare an SEF defect. The Receive STS-1 TOH Processor block will then attempt to reacquire framing.
			Writing a "1" into this bit-field configures the Receive STS-1 TOH Processor block to declare the SEF defect. The Receive STS-1 TOH Processor block will automatically set this bit-field to "0" once it has reacquired framing (e.g., has detected two consecutive STS-1 frames with the correct A1 and A2 bytes).

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 519: Receive STS-1 Transport – Receive J0 Trace Buffer Control Register (Address Location= 0xN14F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		READ SEL	ACCEPT THRD	MSG TYPE	MSG LENGTH	
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION							
7 – 5	Unused	R/O								
4	READ SEL	R/W	J0 Buffer Read Selection:							
			This READ/WRITE bit-field permits a user to specify which of the following buffer segments to read.							
			c. Valid Message Buffer							
			d. Expected Message Buffer							
			0 - Executing a READ to the Receive J0 Trace Buffer, will return contents within the "Valid Message" buffer.							
			1 – Executing a READ to the Receive J0 Trace Buffer, will return contents within the "Expected Message Buffer".							
			Note: In the case of the Receive STS-3 TOH Processor block, the "Receive J0 Trace Buffer" is located at Address Location 0xN300 through 0xN33F.							
3	ACCEPT THRD	R/W	Message Accept Threshold:							
			This READ/WRITE bit-field permits a user to select the number of consecutive times that the Receive STS-1 TOH Processor block must receive a given J0 Trace Message, before it is accepted, as described below.							
		8	0 – The Receive STS-1 TOH Processor block accepts the J0 Message after it has received it the third time in succession.							
		Pro.	12 The Receive STS-1 TOH Processor block accepts the J0 Message after it has received in the fifth time in succession.							
2	MSG TYPE	R/W	Message Alignment Type:							
		9,0 of	This READ/WRITE bit-field permits a user to specify have the Receive STS-1 TOH Processor block will locate the boundary of the J0 Trace Message, as indicated below.							
			0 – Message boundary is indicated by "Line Feed".							
			1 – Message boundary is indicated by the presence of a "1" in the MSB of the first byte (within the J0 Trace Message).							
1 - 0	MSG LENGTH	R/W	J0 Message Length:							
			These READ/WRITE bit-fields permit the user to specify the length of the J0 Trace Message, that the Receive STS-1 TOH Processor block will receive. The relationship between the content of these bit-fields and the corresponding J0 Trace Message Length is presented below.							
			MSG LENGTH Resulting J0 Trace Message Length							



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

00	1 Byte	
01	16 Bytes	
10/11	64 Bytes	

Table 520: Receive STS-1 Transport – Receive SD Burst Error Tolerance – Byte 1 (Address Location= 0xN152)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SD_BURST_TOLERANCE[15:8]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SD_BURST_TOLERANCE [15:8]	Produ	SD_BURST_TOLERANCE - MSB: These READ/WRITE bits, along with the contents of the "Receive STS-1 Transport - SD BURST Tolerance - Byte 0" registers permit the user to specify the maximum number of B2 bit errors that the corresponding Receive STS-1 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-1 frame period), when determining whether or not to declare an SD (Signal Degrade) defect condition. Note: The purpose of this feature is to permit the user to provide some level of B2 error burst filtering, when the Receive STS-1 TOH Processor block is accumulating B2 byte errors in order to declare the SD defect condition. The user can implement this feature in order to configure the Receive STS-1 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SD defect condition.
	The producet and may	, no	

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 521: Receive STS-1 Transport – Receive SD Burst Error Tolerance – Byte 0 (Address Location= 0xN153)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SD_BURST_TOLERANCE[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SD_BURST_TOLERANCE[7:0]	R/W	SD_BURST_TOLERANCE - LSB:
		***	These READ/WRITE bits, along with the contents of the "Receive STS-1 Transport – SD BURST Tolerance – Byte 1" registers permit the user to specify the maximum number of B2 bit errors that the corresponding Receive STS-1 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-1 frame period), when determining whether or not to declare an SD (Signal Degrade) condition. *Note: The purpose of this feature is to permit the user to provide some level of B2 error burst filtering, when the Receive STS-1 TOH Processor block is accumulating B2 byte errors in order to declare the SD defect condition. The user can implement this feature in order to configure the Receive STS-1 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SD defect condition.
	The product of and man	are to	e ordered

Table 522: Receive STS-1 Transport – Receive SF Burst Error Tolerance – Byte 1 (Address Location= 0xN156)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SF_BURST_TOLERANCE[15:8]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SF_BURST_TOLERANCE[15:8]	R/W	SF_BURST_TOLERANCE - MSB:
		duct's	These READ/WRITE bits, along with the contents of the "Receive STS-1 Transport - SF BURST Tolerance – Byte 0" registers permit the user to specify the maximum number of B2 bit errors that the corresponding Receive STS-1 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-1 frame period), when determining whether or not to declare an SF (Signal Failure) condition. *Note: The purpose of this feature is to permit the user to provide some level of B2 error burst filtering, when the Receive STS-1 TOH Processor block is accumulating B2 byte errors in order to declare the SF defect condition. The user can implement this feature in order to configure the Receive STS-1 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SF defect condition.
	The product or product are and may no	no or	Series .

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 523: Receive STS-1 Transport – Receive SF Burst Error Tolerance – Byte 0 (Address Location= 0xN157)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
SF_BURST_TOLERANCE[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SF_BURST_TOLERANCE[7:0]	R/W	SF_BURST_TOLERANCE - LSB:
			These READ/WRITE bits, along with the contents of the "Receive STS-1 Transport – SF BURST Tolerance – Byte 1" registers permit the user to specify the maximum number of B2 bit errors that the corresponding Receive STS-1 TOH Processor block can accumulate during a single Sub-Interval period (e.g., an STS-1 frame period), when determining whether or not to declare an SF (Signal Failure) condition. **Note:** The purpose of this feature is to permit the user to provide some level of B2 error burst filtering, when the Receive STS-1 TOH Processor block is accumulating B2 byte errors in order to declare the SF defect condition. The user can implement this feature in order to configure the Receive STS-1 TOH Processor block to detect B2 bit errors in multiple "Sub-Interval" periods before it will declare the SF defect condition.

Table 524: Receive STS-1 Transport – Receive SD Clear Monitor Interval – Byte 2 (Address Location= 0xN159)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0	
	SD_CLEAR_MONITOR_WINDOW[23:16]							
R/W	R/W	R/W	RAV	R/W	R/W	R/W	R/W	
1	1	0) 11	1	1	1	1	1	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW [23:16]	R/W	SD_CLEAR_MONITOR_INTERVAL - MSB:
			These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SD Clear Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the number of STS-1 Frame periods that will constitute a CLEAR Sub-Interval for SD (Signal Degrade).
			When the Receive STS-1 TOH Processor block is checking for clearing the SD defect, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors is less than that of programmed into the "Receive STS-1 Transport SD Clear Threshold" register, then the SD defect will be cleared.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 525: Receive STS-1 Transport – Receive SD Clear Monitor Interval – Byte 1 (Address Location= 0xN15A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SD_CLEAR_MONITOR_WINDOW[15:8]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW [15:8]	R/W	SD_CLEAR_MONITOR_INTERVAL - Bits 15 through 8:
		74	These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SD Clear Monitor Interval – Byte 2 and Byte 0" tegisters permit the user to specify the number of STS-1 Frame periods that will constitute a CLEAR Sub-Interval for SD (Signal Degrade). When the Receive STS-1 TOH Processor block is checking for clearing the SD defect, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors is less than that of programmed into the "Receive STS-1 Transport SD Clear Threshold" register, then the SD defect will be cleared.

Table 526: Receive STS-1 Transport – Receive SD Clear Monitor Interval – Byte 0 (Address Location= 0xN15B)

Віт 7	Віт 6	Віт 5	Вт 4	Віт 3	Віт 2	Віт 1	Віт 0	
SD_CLEAR_MONITOR_WINDOW[7:0]								
R/W	R/W	R/W	RW	R/W	R/W	R/W	R/W	
1	1	4)	1	1	1	1	1	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SD_CLEAR_MONITOR_WINDOW [7:0]	R/W	SD_CLEAR_MONITOR_INTERVAL – LSB: These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SD Clear Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the number of STS-1 Frame periods that will constitute a
			CLEAR Sub-Interval for SD (Signal Degrade). When the Receive STS-1 TOH Processor block is checking for clearing the SD defect, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors is less than that of programmed into the "Receive STS-1 Transport SD Clear Threshold" register, then the SD defect will be cleared.



Rev 2.0.0

Table 527: Receive STS-1 Transport – Receive SF Clear Monitor Interval – Byte 2 (Address Location= 0xN15D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
SF_CLEAR_MONITOR_WINDOW[23:16]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
1	1	1	1	1	1	1	1	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	NAME SF_CLEAR_MONITOR_WINDOW [23:16]	TYPE R/W	SF_CLEAR_MONITOR_INTERVAL – MSB: These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF Clear Monitor Interval – Byte 1 and Byte 0" registers permit the user to specify the number of STS-1 Frame periods that will constitute a CLEAR Sub-Interval for SF (Signal Failure).
			When the Receive STS-1 TOH Processor block is checking for clearing the SF defect, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors is less than that of programmed into the "Receive STS-1 Transport SF Clear Threshold" register, then the SF defect will be cleared.

Table 528: Receive STS-1 Transport – Receive SF Clear Monitor Interval – Byte 1 (Address Location= 0xN15E)

Віт 7	Віт 6	Віт 5	Віт4	Віт 3	Віт 2	Віт 1	Віт 0		
SF_CLEAR_MONITOR_WINDOW[15:8]									
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	0 0	1	1	1	1		
	170, 21, 10								

		7	
BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDOW [15:8]	R/W	SF_CLEAR_MONITOR_INTERVAL - Bits 15 through 8:
	dand		These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF Clear Monitor Interval – Byte 2 and Byte 0" registers permit the user to specify the number of STS-1 Frame periods that will constitute a CLEAR Sub-Interval for SF (Signal Failure).
			When the Receive STS-1 TOH Processor block is checking for clearing the SF defect, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors is less than that of programmed into the "Receive STS-1 Transport SF Clear Threshold" register, then the SF defect will be cleared.

Table 529: Receive STS-1 Transport – Receive SF Clear Monitor Interval – Byte 0 (Address Location= 0xN15F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	SF_CLEAR_MONITOR_WINDOW[7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
1	1	1	1	1	1	1	1		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	SF_CLEAR_MONITOR_WINDOW	R/W	SF_CLEAR_MONITOR_INTERVAL - LSB:
	[7:0]		These READ/WRITE bits, along the contents of the "Receive STS-1 Transport – SF Clear Monitor Interval – Byte 2 and Byte 1" registers permit the user to specify the number of STS-1 Frame periods that will constitute a CLEAR Sub-Interval for SF (Signal Failure).
			When the Receive STS-1 TOH Processor block is checking for clearing the SF defect, it will accumulate B2 errors for a total of 8 SET Sub-Interval periods. If the number of accumulated B2 errors is less than that of programmed into the "Receive STS-1 Transport SF Clear Threshold" register, then the SF defect will be cleared.
	The data she et and the data and may not be	inde Jorde	ko jok



Table 530: Receive STS-1 Transport – Auto AIS Control Register (Address Location= 0xN163)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit AIS-P (Down- stream) upon J0 Message Unstable	Transmit AIS-P (Down- stream) Upon Section Trace Message Mismatch	Transmit AIS-P (Down- stream) upon SF	Transmit AIS-P (Down- stream) upon SD	Unused	Transmit AIS-P (Down- stream) upon LOF	Transmit AIS-P (Down- stream) upon LOS	Transmit AIS-P (Down- stream) Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

	J		.6 8
BIT NUMBER	Name	Түре	DESCRIPTION
7	Transmit AIS-P (Downstream) upon J0 Message Unstable	R/W	Transmit Path AIS upon Detection of Unstable Section Trace (J0): This READ/WRITE bit-field permits the user to configure the Receive STS-1 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive STS-1 POH Processor blocks), anytime it detects an Unstable Section Trace (J0) condition in the "incoming" STS-1 data-stream. 0 – Does not configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects an "Unstable Section Trace" condition. 1 — Configures the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects an "Unstable Section Trace" condition. Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
6	Transmit AIS-P (Downstream) Upon J0 Message Mismatch	RW	Transmit Path AIS (AIS-P) upon Detection of Section Trace (J0) Mismatch: This READ/WRITE bit-field permits the user to configure the Receive STS-1 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive STS-1 POH Processor blocks), anytime it detects a Section Trace (J0) Mismatch condition in the "incoming" STS-1 data stream. 0 – Does not configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects a "Section Trace Mismatch" condition. 1 – Configures the Receive STS-1 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects a "Section Trace Mismatch" condition. Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
	Transmit AIS-P (Down-	R/W	

			STS-1 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive STS-1 POH Processor block), anytime it declares an SF condition.
			0 – Does not configure the Receive STS-1 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the SF defect.
			1 – Configures the Receive STS-1 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the SF detect.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
4	Transmit AIS-P (Down-	R/W	Transmit Path AIS upon Signal Degrade (SD):
	stream) upon SD		This READ/WRITE bit-field permits the user to configure the Receive STS-1 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive STS-1 POH Processor block) anytime it declares an SD condition.
			0 – Does not configure the Receive STS-1 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the SD defect.
			1 – Configures the Receive STS-1 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the SD defect.
		, pro	Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
3	Unused	R/O	, 0,
2	Transmit AIS-P (Down	R/W	Transmit Path AIS upon Loss of Frame (LOF):
	stream) upon LOF	at no	This READ/WRITE bit-field permits the user to configure the Receive STS-1 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive STS-1 POH Processor block), anytime it declares an LOF condition.
	, gard		0-Does not configure the Receive STS-1 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the LOF defect.
			1 – Configures the Receive STS-1 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the LOF defect.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
1	Transmit AIS-P (Down-	R/W	Transmit Path AIS upon Loss of Signal (LOS):
	stream) upon LOS		This READ/WRITE bit-field permits the user to configure the Receive STS-1 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive STS-1 POH Processor block), anytime it declares an LOS condition.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			0 – Does not configure the Receive STS-1 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) anytime it declares the LOS defect.
			1 – Configures the Receive STS-1 TOH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) anytime it declares the LOS defect.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
0	AUTO AIS	R/W	Automatic Transmission of AIS-P Enable:
			This READ/WRITE bit-field serves two purposes.
			It permits the user to configure the Receive STS-1 TOH Processor block to automatically transmit the Path AlS (AIS-P) indicator, via the down-stream traffic (e.g., towards the Receive STS-1 POH Processor block), upon detection of an SF, SD, Section Trace Mismatch, Section Trace Unstability, LOF or LOS conditions.
			It also permits the user to configure the Receive STS-1 TOH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive STS-1 POH Processor block) anytime it detects an AIS-L condition in the "incoming" STS-1 datastream.
			O – Configures the Receive STS-1 TOH Processor block to NOT automatically transmit the AIS-P indicator (via the "downstream" traffic) upon detection of the AIS-L or any of the "above-mentioned" conditions. 1 – Configures the Receive STS-1 TOH Processor block to
		4	automatically transmit the AIS-P indicator (via the "downstream" traffic) upon detection of the AIS-L or any of the "above-mentioned"
		ucit o	Note: The user must also set the corresponding bit-fields (within this register) to "1" in order to configure the Receive STS-1 TOH Processor block to automatically transmit the AIS-P indicator upon detection of a given a
	the production of the data	id may	

Table 531: Receive STS-1 Transport – Auto AIS (in Downstream STS-1s) Control Register (Address Location= 0xN16B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused		Transmit AIS-P (via Downstream STS-1s) upon LOS	Transmit AIS-P (via Downstream STS-1s) upon LOF	Transmit AIS-P (via Downstream STS-1s) upon SD	Transmit AIS-P (via Downstream STS-1s) upon SF	Unused	Transmit AIS-P (via Downstream STS-1s) Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/O	R/W
0			0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 6	Unused	R/O	"His red
5	Transmit AIS-P (via Downstream STS-1s) upon LOS	R/W R/W	Transmit AIS-P (via Downstream STS-1s) upon LOS (Loss of Signal): This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (in the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares the LOS defect. O – Does not configure the corresponding Transmit SONET POH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares the LOS defect. Configure the corresponding Transmit SONETPOH Processor blocks to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares the LOS defect. Note: In the "long-run" the function of this bit-field is exactly the same as that of Bit 1 (Transmit AIS-P Down-stream — Upon LOS), within the Receive STS-1 Transport — Auto AIS Control Register (Address Location= 0xN163). The only difference is that this register bit will cause the corresponding "downstream" Transmit SONET POH Processor block to IMMEDIATELY begin to transmit the AIS-P condition whenever the Receive STS-1 TOH Processor block declares the LOS defect. This will permit the user to easily comply with the Telcordia GR-
	***		253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the NE declaring the LOS defect. In the case of Bit 1 (Transmit AIS-P Downstream – Upon LOS), several SONET frame periods are required (after the Receive STS-1 TOH Processor block has declared the LOS defect), before the corresponding Transmit SONET POH Processor block will begin the process of transmitting the AIS-P indicator.
			2. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STS-1s Enable) within this register, in order enable this feature.
4	Transmit AIS-P (via Downstream STS-1s)	R/W	Transmit AIS-P (via Downstream STS-1s) upon LOF (Loss of Frame):
	upon LOF		This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (in the corresponding channel) to

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares the LOF defect.
			0 - Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares the LOF defect.
			1 — Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares the LOF defect.
			Note:
			1. In the "long-run" the function of this bit-field is exactly the same as that of Bit 2 (Transmit AIS-P Down-stream – Upon LOF), within the Receive STS-1 Transport – Auto AIS Control Register (Address Location= 0xN163). The only difference is that this register bit will cause the corresponding downstream" Transmit SONET POH Processor blocks to IMMEDIATELY begin to transmit the AIS-P condition whenever the Receive STS-1 TOH Processor block declares the LOF defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the NE declaring the LOF defect.
			In the case of Bit 2 (Transmit AIS-P Downstream – Upon LOF), several SONET frame periods are required (after the Receive STS-3 TOH Processor block has declared the LOS defect), before the corresponding Transmit SONET POH Processor block will begin the process of transmitting the AIS-P indicator.
			2. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AlS-P via Downstream STS-1s Enable) within this register, in order enable this feature.
3	Transmit AIS-P (via Downstream STS-1s)	R/W	Transmit AIS-P (via Downstream STS-1s) upon SD (Signal Degrade):
	upon SD	duct	This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (in the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signals (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares the SD defect.
	7,90	and.	0 - Does not configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares the SD defect.
			1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares the SD defect.
			Note:
			1. In the "long-run" the function of this bit-field is exactly the same as that of Bit 4 (Transmit AIS-P Down-stream – Upon SD), within the Receive STS-1 Transport – Auto AIS Control Register (Address Location= 0xN163). The only difference is that this register bit will cause the corresponding "downstream" Transmit SONET POH Processor blocks to IMMEDIATELY begin to transmit the AIS-P condition whenever the Receive STS-1 TOH Processor block declares

			the SD defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the NE declaring the LOS defect.
			In the case of Bit 1 (Transmit AIS-P Downstream – Upon LOF), several SONET frame periods are required (after the Receive STS-1 TOH Processor block has declared the SD defect), before the corresponding Transmit SONET POH Processor block will begin the process of transmitting the AIS-P indicator.
			2. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STS-1s Enable) within this register, in order enable this feature.
2	Transmit AIS-P (via	R/W	Transmit AIS-P (via Downstream STS-1s) upon Signal Failure (SF):
	Downstream STS-1s) upon SF		This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (in the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares an SF condition.
			0 - Does not configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1TOH Processor block declares the SF defect.
			1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 TOH Processor block declares the SF defect.
			Note
	or odu	70 70 70	In the "long-run" the function of this bit-field is exactly the same as that of Bit 5 (Transmit AIS-P Down-stream – Upon SF), within the Receive STS-1 Transport – Auto AIS Control Register (Address Location= 0xN163). The only difference is that this register bit will cause the corresponding "downstream" Transmit SONET POH Processor blocks to IMMEDIATELY begin to transmit the AIS-P condition whenever the Receive STS-1 TOH Processor block declares the SF defect. This will permit the user to easily comply with the Telcordia GR-253-CORE requirements of an NE transmitting the AIS-P indicator downstream within 125us of the NE declaring the SF defect.
	The Pros	Hay	In the case of Bit 5 (Transmit AIS-P Downstream – Upon SF), several SONET frame periods are required (after the Receive STS-1 TOH Processor block has declared the SF defect), before the corresponding Transmit SONET POH Processor blocks will begin the process of transmitting the AIS-P indicator.
			2. In addition to setting this bit-field to "1", the user must also set Bit 0 (Transmit AIS-P via Downstream STS-1s Enable) within this register, in order enable this feature.
1	Unused	R/O	
0	Transmit AIS-P (via Downstream STS-1s) Enable	R/W	Automatic Transmission of AIS-P (via the downstream STS-1s) Enable:
	Ellable		This READ/WRITE bit-field permits the user to configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P indicator, via its "outbound" STS-1 signal (within the outbound STS-3 signal), upon detection of an SF, SD, LOS and LOF condition via the Receive STS-1 TOH Processor block.
			 0 – Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P indicator, whenever the Receive STS-1 TOH Processor block declares either the LOS, LOF,

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

	SD or the SF defects.
	1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P indicator, whenever the Receive STS-1 TOH Processor block declares either the LOS, LOF, SD or the SF defects.

The product are no longered (OBS)

The product are no longered (OBS)

The product are no longered (OBS)

Table 532: Receive STS-1 Path - Control Register - Byte 2 (Address Location= 0xN183)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unu	sed		Check	RDI-P	REI-P	B3 Error Type
					Type	Error Type	
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3	Check Stuff	R/W	Check (Pointer Adjustment) Stuff Select:
			This READ/WRITE bit-field permits the user to enable/disable the SONET standard recommendation that a pointer increment or decrement operation, detected within 3 SONET frames of a previous pointer adjustment operation (e.g., negative stuff, positive stuff) is ignored.
			0 – Disables this SONET standard implementation. In this mode, all pointer-adjustment operations that are detected will be accepted.
			1 – Enables this "SONET standard" implementation. In this mode, all pointer-adjustment operations that are detected within 3 SONET frame periods of a previous pointer-adjustment operation, will be ignored.
2	RDI-P Type	R/W	Path - Remote Defect Indicator Type Select:
			This READ/WRITE bit-field permits the user to configure the Receive STS-1 POH Processor block to support either the "Single-Bit" or the "Enhanced" RDI-P, as described below.
		, in	0 - Configures the Receive STS-1 POH Processor block to support the Single-Bit RDI-P. In this mode, the Receive STS-1 POH Processor block will only monitor Bit 5, within the G1 byte (of the incoming SPE data), in order to declare and clear the RDI-P indicator.
	ď	oduci	1 Configures the Receive STS-1 POH Processor block to support the Enhanced RDI-P (ERDI-P). In this mode, the Receive STS-1 POH Processor block will monitor bits 5, 6 and 7, within the G1 byte, in order to declare and clear the RDI-P indicator.
1	REI-P Error	R/W	REI-P Error Type:
	Туре	9	This READ/WRITE bit-field permits the user to specify how the "Receive Path REI-P Error Count" register is incremented.
		9 1.	0 – Configures the Receive STS-1 POH Processor block to count REI-P Bit Errors.
			In this case, the "Receive Path REI-P Error Count" register will be incremented by the value of the lower nibble within the G1 byte.
			1 – Configures the Receive STS-1 POH Processor block to count REI-P Frame Errors.
			In this case, the "Receive Path REI-P Error Count" register will be incremented by a single count each time the Receive STS-1 POH Processor block receives a G1 byte, in which bits 1 through 4 are set to a "non-zero" value.
0	B3 Error Type	R/W	B3 Error Type:
			This READ/WRITE bit-field permits the user to specify how the "Receive Path B3 Error Count" register is incremented.

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

0 - Configures the Receive STS-1 POH Processor block to count B3 bit errors. In this case, the "Receive Path B3 Error Count" register will be incremented by the number of bits, within the B3 value, that is in error.
1 – Configures the Receive STS-1 POH Processor block to count B3 frame errors. In this case, the "Receive Path B3 Error Count" register will be incremented by the number of erred STS-1 frames.

The product of products mentioned in this deline of the product are no ordered (OBS)

Table 533: Receive STS-1 Path - Control Register - Byte 1 (Address Location= 0xN186)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused							J1 Unstable Indicator
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 1	Unused	R/O	
7-1	J1 Unstable Indicator	R/O	J1 – Path Trace Unstable Indicator: This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the Path Trace Unstable condition. The Receive STS-1 POH Processor block will declare a J1 (Path Trace) Unstable condition, whenever the "J1 Unstable counter reaches the value "8". The "J0 Unstable" counter will be incremented for each time that it receives a J1 message that differs from the previously received message. The "J1 Unstable" counter is cleared to "0" whenever the Receive STS-1 POH Processor block has received a given J1 Message 3 (or 5) consecutive times. Note: Receiving a given J1 Message 3 (or 5) consecutive times also sets this bit-field to "0". 0 – Path Trace Instability condition is NOT declared. 1 – Path Trace Instability condition is currently declared.

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 534: Receive STS-1 Path – SONET Receive POH Status – Byte 0 (Address Location= 0xN187)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TIM-P Defect Declared	C2 Byte Unstable Condition	UNEQ-P Defect Declared	PLM-P Defect Declared	RDI-P Defect Declared	RDI-P Unstable Condition	LOP-P Defect Declared	AIS-P Defect Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	TIM-P	R/O	Trace Identification Mismatch (TIM-P) Defect Indicator:
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the "Trace Identification Mismatch" condition.
			The Receive STS-1 POH Processor block will declare the "TIM-P" condition, when none of the received 64 byte string (received via the J1 byte) matches the expected 64 byte message.
			The Receive STS-1 POH Processor block will clear the "TIM-P" condition, when 80% of the received 64 byte string (received via the J1 byte) matches the expected 64 byte message.
			0 - Indicates that the Receive STS-1 POH Processor block is NOT currently declaring the TIM-P condition.
			1 – Indicates that the Receive STS-1 POH Processor block is currently declaring the TIM-P condition.
6	C2 Byte	R/O	C2 Byte (Path Signal Label Byte) Unstable Indicator:
	Unstable Condition		This READ ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the "Path Signal Label Byte" Unstable condition.
		we o	The Receive STS-1 POH Processor block will declare a C2 (Path Signal Label Byte) Unstable condition, whenever the "C2 Unstable" counter reaches the value "5". The "C2 Unstable" counter will be incremented for each time that it receives an SPE with a C2 byte value that differs from the previously received C2 byte value. The "C2 Unstable" counter is cleared to "0" whenever the Receive STS-1 POH Processor block has received 3 (or 5) consecutive SPEs of the same C2 byte value.
		1,93	Note: Receiving a given C2 byte value in 3 (or 5) consecutive SPEs also sets this bit-field to "0".
			0 – C2 (Path Signal Label Byte) Unstable condition is NOT declared.
			1 – C2 (Path Signal Label Byte) Unstable condition is currently declared.
5	UNEQ-P	R/O	Path – Unequipped Indicator (UNEQ-P):
			This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the UNEQ-P condition.
			The Receive STS-1 POH Processor block will declare a UNEQ-P condition, if it receives at least five (5) consecutive STS-1 frames, in which the C2 byte was set to 0x00 (which indicates that the SPE is "Unequipped").
			The Receive STS-1 POH Processor block will clear the UNEQ-P condition, if it receives at least five (5) consecutive STS-1 frames, in which the C2 byte was set to a value other than 0x00.
			0 - Indicates that the Receive STS-1 POH Processor block is NOT declaring the

		I	UNEQ-P condition.
			1 – Indicates that the Receive STS-1 POH Processor block is currently declaring the UNEQ-P condition.
			Note: The Receive STS-1 POH Processor block will not declare the UNEQ-P condition if it configured to expect to receive STS-1 frames with C2 bytes being set to "0x00" (e.g., if the "Receive STS-1 Path – Expected Path Label Value" Register –Address Location= 0xN197) is set to "0x00".
4	PLM-P	R/O	Path Payload Mismatch Indicator (PLM-P):
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the PLM-P condition.
			The Receive STS-1 POH Processor block will declare an PLM-P condition, if it receives at least five (5) consecutive STS-1 frames, in which the C2 byte was set to a value other than that which it is expecting to receive.
			Whenever the Receive STS-1 POH Processor block is determine whether or not it should declare the PLM-P defect, it checks the contents of the following two registers.
			The "Receive STS-1 Path - Received Path Label Value" Register (Address Location= 0xN196).
			The "Receive STS-1 Path - Expected Path Label Value" Register (Address Location= 0xN197).
			The "Receive STS-1 Path C Expected Path Label Value" Register contains the value of the C2 bytes, that the Receive STS-1 POH Processor blocks expects to receive.
			The "Receive STS-1 Path Received Path Label Value" Register contains the value of the C2 byte, that the Receive STS-1 POH Processor block has most received "validated" (by receiving this same C2 byte in five consecutive STS-1 frames).
			The Receive STS-1 POH Processor block will declare a PLM-P condition, if the contents of these two register do not match. The Receive STS-1 POH Processor block will clear the PLM-P condition if whenever the contents of these two registers do match.
		6	0 -PLM-P defect is currently not being declared.
		No.	1 - PLM-P defect is currently being declared.
	4 %	0 10	Note: The Receive STS-1 POH Processor block will clear the PLM-P defect, upon detecting the UNEQ-P condition.
3	RDI-P	R/O	Path Remote Defect Indicator (RDI-P):
		'0'	This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the RDI-P condition.
			If the Receive STS-1 POH Processor block is configured to support the "Single-bit RDI-P" function, then it will declare an RDI-P condition if Bit 5 (within the G1 byte of the incoming STS-1 frame) is set to "1" for "RDI-P_THRD" number of consecutive STS-1 frames.
			If the Receive STS-1 POH Processor block is configured to support the Enhanced RDI-P" (ERDI-P) function, then it will declare an RDI-P condition if Bits 5, 6 and 7 (within the G1 byte of the incoming STS-1 frame) are set to [0, 1, 0], [1, 0, 1] or [1, 1, 0] for "RDI-P_THRD" number of consecutive STS-1 frames.
			$\rm 0-Indicates$ that the Receive STS-1 POH Processor block is NOT declaring an RDI-P condition.
			1 – Indicates that the Receive STS-1 POH Processor block is currently declaring an RDI-P condition.

			Note: The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-1 Path – SONET Receive RDI-P Register (Address Location= 0xN193).
2	RDI-P	R/O	RDI-P (Path – Remote Defect Indicator) Unstable:
	Unstable		This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the "RDI-P Unstable" condition. The Receive STS-1 POH Processor block will declare a "RDI-P I Unstable" condition whenever the "RDI-P Unstable Counter" reaches the value "RDI-P THRD". The "RDI-P Unstable" counter is incremented for each time that the Receive STS-1 POH Processor block receives an RDI-P value that differs from that of the previous STS-1 frame. The "RDI-P Unstable" counter is cleared to "0" whenever the same RDI-P value is received in "RDI-P_THRD" consecutive STS-1 frames.
			Note: Receiving a given RDI-P value, in "RDI-P_THRD" consecutive STS-1 frames also clears this bit-field to "0"
			0 – RDI-P Unstable condition is NOT declared.
			1 – RDI-P Unstable condition is currently declared.
			Note: The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-1 Path – SONET Receive RDI-P Register (Address Location= 0xN193).
1	LOP-P	R/O	Loss of Pointer Indicator (LOP-P):
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring the LOP (Loss of Pointer) condition.
			The Receive STS-1 POH Processor block will declare the LOP-P condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the TOH) within 8 to 10 consecutive SONET frames. Further, the Receive STS-1 POH Processor block will declare the LOP-P condition, if it detects 8 to 10 consecutive NDF events.
			The Receive STS-1 POH Processor block will clear the LOP-P condition, whenever the Receive STS-1 POH Processor detects valid pointer bytes (e.g., the H1 and H2 bytes, within the TOH) and normal NDF value for three consecutive STS-1 frames.
			0 Indicates that the Receive STS-1 POH Processor block is NOT declaring the LOP-P condition.
		we o	1 - Indicates that the Receive STS-1 POH Processor block is currently declaring the LOP P condition.
0	AIS-P	R/O	Path AIS (AIS-P) Indicator:
			This READ-ONLY bit-field indicates whether or not the Receive STS-1 POH Processor block is currently declaring an AIS-P condition. The Receive STS-1 POH Processor block will declare an AIS-P if it detects all of the following conditions for three consecutive STS-1 frames.
			The H1, H2 and H3 bytes are set to an "All Ones" pattern.
			The entire SPE is set to an "All Ones" pattern.
			The Receive STS-1 POH Processor block will clear the AIS-P indicator when it detects a valid STS-1 pointer (H1 and H2 bytes) and a "set" or "normal" NDF for three consecutive STS-1 frames.
			0 - Indicates that the Receive STS-1 POH Processor block is NOT currently declaring the AIS-P condition.
			1 – Indicates that the Receive STS-1 POH Processor block is currently declaring the AIS-P condition.
			Note: The Receive STS-1 POH Processor block will NOT declare the LOP-P

	condition if it detects an "All Ones" pattern in the H1, H2 and H3 bytes.
	It will, instead, declare the AIS-P condition.

The product are no ordered (OBS)

The product are no be ordered (OBS)



Table 535: Receive STS-1 Path – SONET Receive Path Interrupt Status – Byte 2 (Address Location= 0xN189)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		Detection of AIS Pointer Interrupt Status	Detection of Pointer Change Interrupt Status	Unused	Change in TIM-P Condition Interrupt Status	Change in J1 Unstable Condition Interrupt Status
R/O	R/O	R/O	RUR	RUR	R/O	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 5	Unused	R/O	"his red
4	Detection of AIS Pointer Interrupt Status	RUR	Detection of AIS Pointer Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Detection of AIS Pointer" interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate this interrupt anytime it detects an "AIS Pointer" in the incoming STS-1 data stream. Note: An "AIS Pointer" is defined as a condition in which both the H1 and H2 bytes (within the TOH) are each set to an "AII Ones" pattern.
		orpro	0 - Indicates that the "Detection of AIS Pointer" interrupt has NOT occurred since the last read of this register. 1 - Indicates that the "Detection of AIS Pointer" interrupt has occurred since the last read of this register.
3	Detection of Pointer Change Interrupt Status	RUR	This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Change" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it accepts a new pointer value (e.g., H1 and H2 bytes, in the TOH bytes). 0 – Indicates that the "Detection of Pointer Change" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of Pointer Change" Interrupt has
2	Unused	R/O	occurred since the last read of this register.
_		. , ,	
1	Change in TIM-P Condition Interrupt Status	RUR	Change in TIM-P (Trace Identification Mismatch) Condition Interrupt. This RESET-upon-READ bit-field indicates whether or not the "Change in TIM-P" Condition interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events.

not occurred since the last read of this register. 1 – Indicates that the "Change in TIM-P Condition" Interrupt had occurred since the last read of this register. O Change in J1 Unstable Condition Interrupt Status: RUR Change in "J1 (Trace Identification Message) Unstabe Condition" Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change in J1 Unstable Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 PC Processor block will generate an interrupt in response to either the following events. • When the Receive STS-1 POH Processor block declare the "J1 Unstable" Condition. • When the Receive STS-1 POH Processor block clears the "Unstable" condition. • When the Receive STS-1 POH Processor block clears the "Unstable" condition.				
0 — Indicates that the "Change in TIM-P Condition" Interrupt had not occurred since the last read of this register. 1 — Indicates that the "Change in TIM-P Condition" Interrupt had occurred since the last read of this register. RUR Change in "J1 (Trace Identification Message) Unstabe Condition" Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change in J1 Unstable Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 PC Processor block will generate an interrupt in response to either the following events. • When the Receive STS-1 POH Processor block declare the "J1 Unstable" Condition. • When the Receive STS-1 POH Processor block clears the "Unstable" condition. 0 — Indicates that the "Change in J1 Unstable Condition Interrupt has NOT occurred since the last read of this register.				If the TIM-P condition is declared.
not occurred since the last read of this register. 1 - Indicates that the "Change in TIM-P Condition" Interrupt had occurred since the last read of this register. Change in "J1 (Trace Identification Message) Unstable Condition Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change in J1 Unstable Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 PC Processor block will generate an interrupt in response to either the following events. When the Receive STS-1 POH Processor block declare the "J1 Unstable" Condition. When the Receive STS-1 POH Processor block clears the "Unstable" condition O - Indicates that the "Change in J1 Unstable Condition Interrupt has NOT occurred since the last read of this register.				If the TIM-P condition is cleared.
Occurred since the last read of this register. RUR Change in "J1 (Trace Identification Message) Unstable Condition Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change in J1 Unstable Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-1 PC Processor block will generate an interrupt in response to either the following events. When the Receive STS-1 POH Processor block declare the "J1 Unstable" Condition. When the Receive STS-1 POH Processor block clears the "Unstable" condition. Interrupt has NOT occurred since the last read of this register.				0 – Indicates that the "Change in TIM-P Condition" Interrupt has not occurred since the last read of this register.
Condition Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change in J1 Unstable Condition" Interrupt has occurred sind the last read of this register. If this interrupt is enabled, then the Receive STS-1 PC Processor block will generate an interrupt in response to either the following events. • When the Receive STS-1 POH Processor block declare the "J1 Unstable" Condition. • When the Receive STS-1 POH Processor block clears the "Unstable" condition. • This RESET-upon-READ bit-field indicates whether or not the "Change in J1 Unstable Condition on the "Change in J1 Unstable Change in J1 Unstable Cha				1 – Indicates that the "Change in TIM-P Condition" Interrupt has occurred since the last read of this register.
"Change in J1 Unstable Condition" Interrupt has occurred sind the last read of this register. If this interrupt is enabled, then the Receive STS-1 PC Processor block will generate an interrupt in response to either the following events. • When the Receive STS-1 POH Processor block declare the "J1 Unstable" Condition. • When the Receive STS-1 POH Processor block clears the "Unstable" condition. • Unstable "condition. 0 — Indicates that the "Change in J1 Unstable Condition Interrupt has NOT occurred since the last read of this register.	0		RUR	Change in "J1 (Trace Identification Message) Unstable Condition" Interrupt Status:
Processor block will generate an interrupt in response to either the following events. • When the Receive STS-1 POH Processor block declare the "J1 Unstable" Condition. • When the Receive STS-1 POH Processor block clears the "Unstable" condition. 0 — Indicates that the "Change in J1 Unstable Condition Interrupt has NOT occurred since the last read of this register.				This RESET-upon-READ bit-field indicates whether or not the "Change in J1 Unstable Condition" Interrupt has occurred since the last read of this register.
"J1 Unstable" Condition. • When the Receive STS-1 POH Processor block clears the " Unstable" condition. 0 — Indicates that the "Change in J1 Unstable Condition Interrupt has NOT occurred since the last read of this register.				If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events.
Unstable" condition 0 — Indicates that the "Change in J1 Unstable Condition Interrupt has NOT occurred since the last read of this register.				When the Receive STS-1 POH Processor block declare the "J1 Unstable" Condition.
Interrupt has NOT occurred since the last read of this register.				When the Receive STS-1 POH Processor block clears the "J1 Unstable" condition.
1 - Indicates that the "Change in J1 Unstable Condition Interrupt has occurred since the last read of this register.				0 - Indicates that the "Change in J1 Unstable Condition" Interrupt has NOT occurred since the last read of this register.
The product are no ordered of the product are not be ordered of the product are not be ordered.				1 — Indicates that the "Change in J1 Unstable Condition" Interrupt has occurred since the last read of this register.
		The product of and may	production of the production o	ordered Ob



Table 536: Receive STS-1 Path – SONET Receive Path Interrupt Status – Byte 1 (Address Location= 0xN18A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
New J1 Message Interrupt Status	Detection of REI-P Event Interrupt Status	Change in UNEQ-P Condition Interrupt Status	Change in PLM-P Condition Interrupt Status	New C2 Byte Interrupt Status	Change in C2 Byte Unstable Condition Interrupt Status	Change in RDI-P Unstable Condition Interrupt Status	New RDI-P Value Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	New J1	RUR	New J1 (Trace Identification) Message Interrupt Status:
	Message Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "New J1 Message" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it has accepted (or validated) and new J1 (Trace Identification) Message.
			0 – Indicates that the "New J1 Message" Interrupt has NOT occurred since the last read of this register.
			1 - Indicates that the "New J1-Message" Interrupt has occurred since the last read of this register.
6	Detection of	RUR	Detection of REI-P Event Interrupt Status:
	REI-P Event Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of REI-P Event" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects an REI-P condition in the coming STS-1 data-stream.
		odu	0 Indicates that the "Detection of REI-P Event" Interrupt has NOT occurred since the last read of this register.
		6, 8	1 – Indicates that the "Detection of REI-P Event" Interrupt has occurred since the last read of this register.
5	Change in	RUR	Change in UNEQ-P (Path – Unequipped) Condition Interrupt Status:
	UNEQ-P Condition Interrupt Status	o all	This RESET-upon-READ bit-field indicates whether or not the "Change in UNEQ-P Condition" interrupt has occurred since the last read of this register.
			If this interrupt is enabled , then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following conditions.
			When the Receive STS-1 POH Processor block declares the UNEQ-P Condition.
			When the Receive STS-1 POH Processor block clears the UNEQ-P Condition.
			0 - Indicates that the "Change in UNEQ-P Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in UNEQ-P Condition" Interrupt has occurred since the last read of this register.
			Note: The user can determine the current state of UNEQ-P by reading

			out the state of Pit 5 / INFO P Defeat Declared) within the
			out the state of Bit 5 (UNEQ-P Defect Declared) within the "Receive STS-1 Path – SONET Receive POH Status – Byte 0" Register (Address Location= 0xN187).
4	Change in PLM-P Condition	RUR	Change in PLM-P (Path – Payload Mismatch) Condition Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit indicates whether or not the "Change in PLM-P Condition" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following conditions.
			When the Receive STS-1 POH Processor block declares the "PLM-P" Condition.
			When the Receive STS-1 POH Processor block clears the "PLM-P" Condition.
			0 - Indicates that the "Change in PLMP Condition" Interrupt has NOT occurred since the last read of this register.
			1 - Indicates that the "Change in PLM-P Condition" Interrupt has occurred since the last read of this register.
3	New C2 Byte	RUR	New C2 Byte Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "New C2 Byte" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it has accepted a new C2 byte.
			0 - Indicates that the "New C2 Byte" Interrupt has NOT occurred since the last read of this register.
			1 - Indicates that the "New C2 Byte" Interrupt has occurred since the last read of this register.
2	Change in C2	RUR	Change in C2 Byte Unstable Condition Interrupt Status:
	Byte Unstable Condition Interrupt Status	, uct	This RESET-upon-READ bit-field indicates whether or not the "Change in C2 Byte Unstable Condition" Interrupt has occurred since the last read of this register.
	or or	O KO	If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events.
	The b.	9 11/8	When the Receive STS-1 POH Processor block declares the "C2 Byte Unstable" condition.
	, 80	ano	• When the Receive STS-1 POH Processor block clears the "C2 Byte Unstable" condition.
			0- Indicates that the "Change in C2 Byte Unstable Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in C2 Byte Unstable Condition" Interrupt has occurred since the last read of this register.
			Note: The user can determine the current state of "C2 Byte Unstable Condition" by reading out the state of Bit 6 (C2 Byte Unstable Condition) within the "Receive STS-1 Path – SONET Receive POH Status – Byte 0" Register (Address Location= 0xN187).
1	Change in RDI-	RUR	Change in RDI-P Unstable Condition Interrupt Status:
	P Unstable Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in RDI-P Unstable Condition" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			generate an interrupt in response to either of the following conditions.
			When the Receive STS-1 POH Processor block declares an "RDI-P Unstable" condition.
			When the Receive STS-1 POH Processor block clears the "RDI-P Unstable" condition.
			0 – Indicates that the "Change in RDI-P Unstable Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in RDI-P Unstable Condition" Interrupt has occurred since the last read of this register.
			Note: The user can determine the current state of "RDI-P Unstable" by reading out the state of Bit 2 (RDI-P Unstable Condition) within the "Receive STS-1 Path – SONET Receive POH Status – Byte 0" Register (Address Location= 0xN187).
0	New RDI-P Value Interrupt Status	RUR	New RDI-P Value Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "New RDI-P Value" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate this interrupt anytime it receives and "validates" a new RDI-P value. 0 – Indicates that the "New RDI-P Value" Interrupt has NOT occurred since
			the last read of this register.
			1 – Indicates that the "New RDI-P Value" Interrupt has occurred since the last read of this register.
			Note: The user can obtain the "New RDI-P Value" by reading out the contents of the "RDI-P ACCEPT[2:0]" bit-fields. These bit-fields are located in Bits 6 through 4, within the "Receive STS-1 Path — SONET Receive RDI-P Register" (Address Location= 0xN193).
101 00 1de			
adil at 30 at 0			
proghes in			
The da mo			
, gallo			

Table 537: Receive STS-1 Path – SONET Receive Path Interrupt Status – Byte 0 (Address Location= 0xN18B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Detection of B3 Byte Error Interrupt Status	Detection of New Pointer Interrupt Status	Detection of Unknown Pointer Interrupt Status	Detection of Pointer Decrement Interrupt Status	Detection of Pointer Increment Interrupt Status	Detection of NDF Pointer Interrupt Status	Change of LOP-P Condition Interrupt Status	Change of AIS-P Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION			
7	Detection of B3 Byte	RUR	Detection of B3 Byte Error Interrupt Status:			
	Error Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of B3 Byte Error" Interrupt has occurred since the last read of this register.			
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a B3 byte error in the incoming STS-1 data stream.			
			0 - Indicates that the "Detection of B3 Byte Error" Interrupt has NOT occurred since the last read of this interrupt.			
			1 - Indicates that the "Detection of B3 Byte Error" Interrupt has occurred since the last read of this interrupt.			
6	Detection of New	RUR	Detection of New Pointer Interrupt Status:			
	Pointer Interrupt Status	, 0	This RESET-upon-READ indicates whether the "Detection of New Pointer" interrupt has occurred since the last read of this register.			
	Detection of Unknown Pointer Interrupt Status	i or	If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a new pointer value in the incoming STS-1 frame.			
	290	0	Note: Pointer Adjustments with NDF will not generate this interrupt.			
	opio sy	160	0 – Indicates that the "Detection of New Pointer" Interrupt has NOT occurred since the last read of this register.			
	Theatad	Mo	1 – Indicates that the "Detection of New Pointer" Interrupt has occurred since the last read of this register.			
5	Detection of Unknown	RUR	Detection of Unknown Pointer Interrupt Status:			
	Pointer Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of Unknown Pointer" interrupt has occurred since the last read of this register.			
			If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime that it detects a "pointer" that does not fit into any of the following categories.			
			An Increment Pointer			
			A Decrement Pointer			
			An NDF Pointer			
			An AIS (e.g., All Ones) Pointer			
			New Pointer			
			0 - Indicates that the "Detection of Unknown Pointer" interrupt has NOT			

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			occurred since the last read of this register.
			1 – Indicates that the "Detection of Unknown Pointer" interrupt has occurred since the last read of this register.
4	Detection of Pointer	RUR	Detection of Pointer Decrement Interrupt Status:
	Decrement Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Decrement" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a "Pointer Decrement" event.
			0 - Indicates that the "Detection of Pointer Decrement" interrupt has NOT occurred since the last read of this register.
			1 - Indicates that the "Detection of Pointer Decrement" interrupt has occurred since the last read of this register.
3	Detection of Pointer	RUR	Detection of Pointer Increment Interrupt Status:
	Increment Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Increment" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a "Pointer Increment" event.
			0 – Indicates that the "Detection of Pointer Increment" interrupt has NOT occurred since the last read of this register.
			1 - Indicates that the 'Detection of Pointer Increment" interrupt has occurred since the last read of this register.
2	Detection of NDF	RUR	Detection of NDF Pointer Interrupt Status:
	Pointer Interrupt Status	duct	This RESET-upon-READ bit-field indicates whether or not the "Detection of NDF Pointer" interrupt has occurred since the last read of this register. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects an NDF Pointer event.
	A CONTRACTOR OF THE CONTRACTOR		Or Indicates that the "Detection of NDF Pointer" interrupt has NOT occurred since the last read of this register.
	Theor	SIME	1 – Indicates that the "Detection of NDF Pointer" interrupt has occurred since the last read of this register.
1	Change of LOP-P	RUR	Change of LOP-P Condition Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in LOP-P Condition" interrupt has occurred since the last read of this register.
			If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events.
			When the Receive STS-1 POH Processor block declares an "Loss of Pointer" condition.
			When the Receive "STS-1 POH Processor" block clears the "Loss of Pointer" condition.
			0 – Indicates that the "Change in LOP-P Condition" interrupt has NOT occurred since the last read of this register.
			1 - Indicates that the "Change in LOP-P Condition" interrupt has

			occurred since the last read of this register.
			Note: The user can determine the current state of LOP-P by reading out the state of Bit 1 (LOP-P Defect Declared) within the "Receive STS-1 Path – SONET Receive POH Status – Byte 0" Register (Address Location=0xN187).
0	Change of AIS-P	RUR	Change of AIS-P Condition Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of AIS-P Condition" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events.
			When the Receive STS-1 POH Processor block declares an AIS-P condition.
			When the Receive STS-1 POH Processor block clears the AIS-P condition.
			0 – Indicates that the "Change of AIS-P Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change of AIS-P Condition" Interrupt has occurred since the last read of this register.
			Note: The user can determine the current state of AIS-P by reading out the state of Bit 0 (AIS-P Defect Declared) within the "Receive STS-1 Path – SONET Receive POH Status – Byte 0" Register (Address Location= 0xN187).
	orodu.	ct of a	out the state of Bit 0 (AIS-P Defect Declared) within the "Receive STS-1 Path – SONET Receive POH Status – Byte 0" Register (Address Location= 0xN187).
	The President	may	

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 538: Receive STS-1 Path – SONET Receive Path Interrupt Enable – Byte 2 (Address Location = 0xN18D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused		Detection of AIS Pointer Interrupt Enable	Detection of Pointer Change Interrupt Enable	Unused	Change in TIM-P Condition Interrupt Enable	Change in J1 Unstable Condition Interrupt Enable	
R/O	R/O	R/O	R/W	R/W	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7-5	Unused	R/O	inis red
4	Detection of AIS Pointer	R/W	Detection of AIS Pointer Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of AIS Pointer" interrupt.
			If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects an "AIS Pointer", in the incoming STS-1 data stream.
			Note: An "AIS Pointer" is defined as a condition in which both the H1 and H2 bytes (within the TOH) are each set to an "All Ones" Pattern
			0 - Disables the "Detection of AIS Pointer" Interrupt.
			1 – Enables the "Detection of AIS Pointer" Interrupt.
3	Detection of Pointer	R/W	Detection of Pointer Change Interrupt Enable:
	Change Interrupt Enable	روا	This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Pointer Change" Interrupt.
		ici s	If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it has accepted a new pointer value.
	of	16 7	0 – Disables the "Detection of Pointer Change" Interrupt.
	We to	Ma.	1 - Enables the "Detection of Pointer Change" Interrupt.
2	Unused	R/O	
1	Change in TIM-P Condition Interrupt	R/W	Change in TIM-P (Trace Identification Mismatch) Condition Interrupt:
	Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in TIM-P Condition" interrupt.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events.
			If the TIM-P condition is declared.
			If the TIM-P condition is cleared.
			0 – Disables the "Change in TIM-P Condition" Interrupt.
			1 – Enables the "Change in TIM-P Condition" Interrupt.
0	Change in J1 Unstable Condition Interrupt	R/W	Change in "J1 (Trace Identification Message) Unstable Condition" Interrupt Status:

S

Rev 2.0.0 3-0	HANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER – ATM REGISTERS
---------------	---

Enable	Condition" Interrupt Status:
	This READ/WRITE bit-field permits the user to either enable or disable the "Change in J1 (Trace Identification) Message Unstable Condition" Interrupt.
	If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events.
	When the Receive STS-1 POH Processor block declares the "J1 Unstable" Condition.
	When the Receive STS-1 POH Processor block clears the "J1 Unstable" Condition.
	0 – Disables the "Change in J1 Message Unstable Condition" interrupt.
	1 – Enables the "Change in John Message Unstable Condition" interrupt.
The product	1 - Enables the "Change in Ja Message Unstable Condition" interrupt. 1 - Enables the "Change in Ja Message Unstable Condition" interrupt.

operience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 539: Receive STS-1 Path – SONET Receive Path Interrupt Enable – Byte 1 (Address Location= 0xN18E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
New J1 Message Interrupt Enable	Detection of REI-P Event Interrupt Enable	Change in UNEQ-P Condition Interrupt Enable	Change in PLM-P Condition Interrupt Enable	New C2 Byte Interrupt Enable	Change in C2 Byte Unstable Condition Interrupt Enable	Change in RDI-P Unstable Condition Interrupt Enable	New RDI-P Value Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION				
7	New J1 Message	R/W	New J1 (Trace Identification) Message Interrupt Enable:				
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "New J1 Message" Interrupt.				
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it has accepted (or validated) and new J1 (Trace Identification) Message.				
			0 – Disables the "New J1 Message" Interrupt.				
			1 – Enables the "New J1 Message" Interrupt.				
6	Detection of REI-P	R/W	Detection of REI-P Event Interrupt Enable:				
	Event Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of REI-P Event" Interrupt.				
		(If this interrupt is enabled, then he Receive STS-1 POH Process block will generate an interrupt anytime it detects an REI-P condition the coming STS-1 data-stream.				
			0.4 Disables the "Detection of REI-P Event" Interrupt.				
		X VIX	Enables the "Detection of REI-P Event" Interrupt.				
5	Change in UNEQ-P	R/W	Change in UNEQ-P (Path – Unequipped) Condition Interrupt Enable:				
	Enable	o M	This READ/WRITE bit-field permits the user to either enable or disable the "Change in UNEQ-P Condition" interrupt.				
		and	If this interrupt is enabled , then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following conditions.				
			When the Receive STS-1 POH Processor block declares the UNEQ-P Condition.				
			When the Receive STS-1 POH Processor block clears the UNEQ-P Condition.				
			0 - Disables the "Change in UNEQ-P Condition" Interrupt.				
			1 – Enables the "Change in UNEQ-P Condition" Interrupt.				
4	Change in PLM-P Condition Interrupt	R/W	Change in PLM-P (Path – Payload Mismatch) Condition Interrupt Enable:				
	Enable		This READ/WRITE bit permits the user to either enable or disable the "Change in PLM-P Condition" interrupt.				
			If this interrupt is enabled, then the Receive STS-1 POH Processor				

-			
			block will generate an interrupt in response to either of the following conditions.
			When the Receive STS-1 POH Processor block declares the "PLM-P" Condition.
			When the Receive STS-1 POH Processor block clears the "PLM-P" Condition.
			0 – Disables the "Change in PLM-P Condition" Interrupt.
			1 – Enables the "Change in PLM-P Condition" Interrupt.
3	New C2 Byte	R/W	New C2 Byte Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "New C2 Byte" Interrupt.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt anytime it has accepted a new C2 byte.
			0 – Disables the "New C2 Byte" Interrupt.
			1 – Enables the "New C2 Byte" (nterrupt.
			Note: The user can obtain the value of this "New C2" byte by reading the contents of the "Receive STS-1 Path – Received Path Label Value" Register (Address Location= 0xN196).
2	Change in C2 Byte	R/W	Change in C2 Byte Unstable Condition Interrupt Enable:
	Unstable Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in C2 Byte Unstable Condition" Interrupt.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events.
		, 9	 When the Receive STS-1 POH Processor block declares the "C2 Byte Unstable" condition.
		10,	When the Receive STS-1 POH Processor block clears the "C2 Byte Unstable" condition.
	N N	× 0.	O Disables the "Change in C2 Byte Unstable Condition" Interrupt.
	400	8	– Enables the "Change in C2 Byte Unstable Condition" Interrupt.
1	Change in RDI-P	R/W	Change in RDI-P Unstable Condition Interrupt Enable:
	Unstable Condition Interrupt Enable	Mo	This READ/WRITE bit-field permits the user to either enable or disable the "Change in RDI-P Unstable Condition" interrupt.
	o and		If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following conditions.
			When the Receive STS-1 POH Processor block declares an "RDI-P Unstable" condition.
			When the Receive STS-1 POH Processor block clears the "RDI-P Unstable" condition.
			0 – Disables the "Change in RDI-P Unstable Condition" Interrupt.
			1 – Enables the "Change in RDI-P Unstable Condition" Interrupt.
0	New RDI-P Value Interrupt Enable	R/W	New RDI-P Value Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "New RDI-P Value" interrupt.
			If this interrupt is enabled, then the Receive STS-1 POH Processor block will generate this interrupt anytime it receives and "validates" a

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

D	3	n	n

new RDI-P value.
0 – Disables the "New RDI-P Value" Interrupt.
1 – Enable the "New RDI-P Value" Interrupt.

The product of products in the product of products in the product of products in the product of the product of

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 540: Receive STS-1 Path – SONET Receive Path Interrupt Enable – Byte 0 (Address Location= 0xN18F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Detection of B3 Byte Error Interrupt Enable	Detection of New Pointer Interrupt Enable	Detection of Unknown Pointer Interrupt Enable	Detection of Pointer Decrement Interrupt Enable	Detection of Pointer Increment Interrupt Enable	Detection of NDF Pointer Interrupt Enable	Change of LOP-P Condition Interrupt Enable	Change of AIS-P Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION			
7	Detection of B3 Byte Error Interrupt Enable	R/W	Detection of B3 Byte Error Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B3 Byte Error" Interrupt. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a B3-byte error in the incoming STS-1 data-stream. 0 – Disables the "Detection of B3 Byte Error" interrupt. 1 – Enables the "Detection of B3 Byte Error" interrupt.			
6	Detection of New Pointer Interrupt Enable	R/W	Detection of New Pointer Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable "Detection of New Pointer" interrupt. If the user enables this interrupt, ther Receive STS-1 POH Processor block will generate an interrupt anytime it de a new pointer value in the incoming STS-1 frame. Note: Pointer Adjustments with NDF will not generate this interrupt. 0 – Disables the "Detection of New Pointer" Interrupt. 1 + Enables the "Detection of New Pointer" Interrupt.			
5	Detection of Unknown Pointer Interrupt Enable	R/W	Detection of Unknown Pointer Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Unknown Pointer" interrupt. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a "Pointer Adjustment" that does not fit into any of the following categories. • An Increment Pointer. • A Decrement Pointer • An NDF Pointer • New Pointer. • Disables the "Detection of Unknown Pointer" Interrupt. 1 – Enables the "Detection of Unknown Pointer" Interrupt.			
4	Detection of Pointer Decrement Interrupt Enable	R/W	Detection of Pointer Decrement Interrupt Enable: This READ/WRITE bit-field permits the user to enable or disable the "Detection of Pointer Decrement" Interrupt. If the user enables this interrupt, then the Receive STS-1 TOH Processor block will generate an interrupt anytime it detects a "Pointer-Decrement" event. 0 – Disables the "Detection of Pointer Decrement" Interrupt.			

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			1 – Enables the "Detection of Pointer Decrement" Interrupt.
3	Detection of Pointer Increment Interrupt Enable	R/W	Detection of Pointer Increment Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Pointer Increment" Interrupt. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects a "Pointer Increment" event. 0 – Disables the "Detection of Pointer Increment" Interrupt.
			1 – Enables the "Detection of Pointer Increment" Interrupt.
2	Detection of NDF Pointer Interrupt Enable	R/W	Detection of NDF Pointer Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Detection of NDF Pointer" Interrupt. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt anytime it detects an NDF Pointer event. 0 – Disables the "Detection of NDF Pointer" interrupt. 1 – Enables the "Detection of NDF Pointer" interrupt.
1	Change of LOP-P Condition Interrupt Enable	R/W	Change of LOP-P Condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change in LOP (Loss of Pointer)" Condition interrupt. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events. • When the Receive STS-1 POH Processor block declares a "Loss of Pointer" condition. • When the Receive STS-1 POH Processor block clears the "Loss of Pointer" condition. 0 – Disable the "Change of LOP" Interrupt. 1 – Enables the "Change of LOP" Interrupt. Note: The user can determine the current state of "LOP" by reading out the contents of Bit 1 (LOP) within the "Receive STS-1 Path – SONET Receive POH Status – Byte 0" (Address Location= 0xN187).
0	Change of AIS-P Interrupt Enable	R/W	Change of AlS-P Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change of AlS-P (Path AlS)" interrupt. If the user enables this interrupt, then the Receive STS-1 POH Processor block will generate an interrupt in response to either of the following events. When the Receive STS-1 POH Processor block declares an "AlS-P" condition. When the Receive STS-1 POH Processor block clears the "AlS-P" condition. Disables the "Change of AlS-P" Interrupt. The user can determine the current state of "AlS-P" by reading out the contents of Bit 0 (AlS-P Defect Declared) within the "Receive STS-1 Path — SONET Receive POH Status — Byte 0" (Address Location= 0xN187).

Table 541: Receive STS-1 Path – SONET Receive RDI-P Register (Address Location= 0xN193)

BIT 7 BIT 6 BIT 5 BIT 4 BIT 3 BIT 2	Віт 1 Віт 0
---	-------------



Unused	Unused RDI-P_ACCEPT[2:0]			Unused RDI-P_ACCEPT[2:0] RDI-P THRESHOLD[3:0]				
R/O	R/O	R/O	R/O	R/W R/W R/W R/W			R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7	Unused	R/O	
6 - 4	RDI-P_ACCEPT[2:0]	R/O	Accepted RDI-P Value:
			These READ-ONLY bit-fields contain the value of the most recently "accepted" RDI-P (e.g., bits 5, 6 and 7 within the G1 byte) value.
			Note: A given RDI-P value will be "accepted" by the Receive STS-1 POH Processor block, if this RDI-P value has been consistently received in "RDI-P THRESHOLD[3:0]" number of STS-1 frames.
3 - 0	RDI-P THRESHOLD[3:0]	R/W	RDI-P Threshold:
			These READ/WRITE bit-fields permit the user to defined the "RDI-P Acceptance Threshold" for the Receive STS-1 POH Processor Block.
			The "RDI-P Acceptance Threshold" is the number of consecutive STS-1 frames, in which the Receive STS-1 POH Processor block must receive a given RDI-P value, before it "accepts" or "validates" it.
			The most recently "accepted" RDI-P value is written into the "RDI-P ACCEPT[2:0]" bit-fields, within this register.
	The product of and many	or process	ordered Condered

EXAR Experience Our Connectivi

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 542: Receive STS-1 Path – Received Path Label Value (Address Location= 0xN196)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	Received_C2_Byte_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
1	1	1	1	1	1	1	1		

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Received C2 Byte Value[7:0]	R/O	Received "Filtered" C2 Byte Value:
			These READ-ONLY bit-fields contain the value of the most recently "accepted" C2 byte, via the Receive STS-1 POH Processor block. The Receive STS-1 POH Processor block will "accept" a C2 byte value (and load it into these bit-fields) if it has received a consistent C2 byte, in five (5) consecutive STS-1 frames. Note: The Receive STS-1 POH Processor block uses this register, along the "Receive STS-1 Path – Expected Path Label Value" Register (Address Location = 0xN197), when declaring or clearing the UNEQ-P and PLM-P alarm conditions.

Table 543: Receive STS-1 Path - Expected Path Label Value (Address Location= 0xN197)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 2	Віт 1	Віт 0			
Expected_C2_Byte_Value[7:0]									
R/W	R/W	R/W	R/W R/W	R/W	R/W	R/W			
1	1	1	100 1	1	1	1			

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Expected C2 Byte Value[7:0]	R/W	Expected C2 Byte Value:
	the preshed in	4	These READ/WRITE bit-fields permits the user to specify the C2 (Path Label Byte) value, that the Receive STS-1 POH Processor block should expect when declaring or clearing the UNEQ-P and PLM-P alarm conditions.
	dane		If the contents of the "Received C2 Byte Value[7:0]" (see "Receive STS-1 Path – Received Path Label Value" register) matches the contents in these register, then the Receive STS-1 POH will not declare any alarm conditions.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 544: Receive STS-1 Path - B3 Error Count Register - Byte 3 (Address Location= 0xN198)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	B3_Error_Count[31:24]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	B3_Error_Count[31:24]	RUR	B3 Error Count – MSB:
			This RESET-upon-READ register, along with "Receive STS-1 Path – B3 Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a B3 byte error. *Note:* 1. If the B3 Error Type is configured to be "bit errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the number of bits, within the B3 value that are in error. 2. If the B3 Error Type is configured to be "frame errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the number of frames that contain erred B3 bytes.

Table 545: Receive STS-1 Path - B3 Error Count Register - Byte 2 (Address Location= 0xN199)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0		
B3_Error_Count[23:16]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0 (0	0 0	0	0	0	0		

BIT NUMBER	NAME	O TYPE	DESCRIPTION			
7 - 0	B3_Error_Count[23:16]	RUR	B3 Error Count (Bits 23 through 16):			
	The bata	(18)	This RESET-upon-READ register, along with "Receive STS-1 Path – B3 Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a B3 byte error.			
	'		Note:			
			1. If the B3 Error Type is configured to be "bit errors", then the Receiv STS-1 POH Processor block will increment this 32 bit counter by th number of bits, within the B3 value that are in error.			
			2. If the B3 Error Type is configured to be "frame errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the number of frames that contain erred B3 bytes.			

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 546: Receive STS-1 Path - B3 Error Count Register - Byte 1 (Address Location= 0xN19A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
B3_Error_Count[15:8]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	B3_Error_Count[15:8]	RUR	B3 Error Count – (Bits 15 through 8):
			This RESET-upon-READ register, along with "Receive STS-1 Path – B3 Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a B3 byte error. *Note:* 1. If the B3 Error Type is configured to be "bit errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the number of bits, within the B3 value that are in error. 2. If the B3 Error Type is configured to be "frame errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the number of frames that contain erred B3 bytes.

Table 547: Receive STS-1 Path - B3 Error Count Register - Byte 0 (Address Location= 0xN19B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 2	Віт 1	Віт 0		
B3_Error_Count[7:0]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0 0	0	0	0		

BIT NUMBER	Name	TYPE	DESCRIPTION
7 - 0	B3_Error_Count[7:0]	RUR	B3 Error Count - LSB:
	They	andm	This RESET-upon-READ register, along with "Receive STS-1 Path – B3 Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a B3 byte error.
		0	Note:
			1. If the B3 Error Type is configured to be "bit errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the number of bits, within the B3 value that are in error.
			2. If the B3 Error Type is configured to be "frame errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the number of frames that contain erred B3 bytes.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 548: Receive STS-1 Path – REI-P Error Count Register – Byte 3 (Address Location= 0xN19C)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
	REI_P_Error_Count[31:24]										
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR				
0	0	0	0	0	0	0	0				

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	REI_P_Error_Count[31:24]	RUR	REI-P Error Count – MSB:
			This RESET-upon-READ register, along with "Receive STS-1 Path – REI-P Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a Path – Remote Error Indicator. *Note:* 1. If the REI-P Error Type is configured to be "bit errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the hibble-value within the REI-P field of the incoming G1 byte. 2. If the REI-P Error Type is configured to be "frame errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the number of frames that contain non-zero REI-P values.

Table 549: Receive STS-1 Path – REI_P Error Count Register – Byte 2 (Address Location= 0xN19D)

Віт 7	Віт 6	Віт 5	Вп 4	Віт 3	Віт 2	Віт 1	Віт 0		
RELP_Error_Count[23:16]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	QC		0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	REI_P_Error_Count[23:16]	RUR	REI-P Error Count (Bits 23 through 16):
	The date of the		This RESET-upon-READ register, along with "Receive STS-1 Path – REI-P Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a Path – Remote Error Indicator.
			Note:
			1. If the REI-P Error Type is configured to be "bit errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the nibble-value within the REI-P field of the incoming G1 byte.
			2. If the REI-P Error Type is configured to be "frame errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the number of frames that contain non-zero REI-P values.



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 550: Receive STS-1 Path – REI_P Error Count Register – Byte 1 (Address Location= 0xN19E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
REI_P_Error_Count[15:8]										
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR			
0	0	0	0	0	0	0	0			

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	REI_P_Error_Count[15:8]	RUR	REI-P Error Count – (Bits 15 through 8)
			This RESET-upon-READ register, along with "Receive STS-1 Path – REI-P Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a Path – Remote Error Indicator. *Note:* 1. If the REI-P Error Type is configured to be "bit errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the nibble-value within the REI-P field of the incoming G1 byte. 2. If the REI-P Error Type is configured to be "frame errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the number of frames that contain non-zero REI-P values.

Table 551: Receive STS-1 Path – REI_P Error Count Register – Byte 0 (Address Location= 0xN19F)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0	
	REI_P Error Count[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0 (200	0	0	0	0	

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	NAME REI_P_Error_Count[7:0]	TYPE RUR	REI-P Error Count – LSB: This RESET-upon-READ register, along with "Receive STS-1 Path – REI-P Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STS-1 POH Processor block detects a Path – Remote Error Indicator. Note: 1. If the REI-P Error Type is configured to be "bit errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter by the nibble-value within the REI-P field of the incoming G1 byte. 2. If the REI-P Error Type is configured to be "frame errors", then the Receive STS-1 POH Processor block will increment this 32 bit counter

Table 552: Receive STS-1 Path - Receive J1 Control Register (Address Location= 0xN1A3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		Receive J1 Message Buffer Read Select	Accept Threshold	Message Type	Message Le	ength[1:0]
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION					
7 – 5	Unused	R/O						
4	Received J1 Message	R/W	J1 Buffer Read Se	lection:				
	Buffer Read Select		This READ/WRITE following buffer seg	bit-field permits a user to specify which of the ments to read.				
			c. Valid Message Buffer					
			d. Expected	Message Buffer				
			0 - Executing a READ to the Receive J1 Trace Buffer, will recontents within the "Valid Message" buffer.					
				EAD to the Receive J1 Trace Buffer, will return "Expected Message Buffer".				
			"Receive	of the Receive STS-1 POH Processor block, the In Trace Buffer" is located at Address Location brough 0xN53F.				
3	Accept Threshold	R/W	Message Accept T	hreshold:				
		or pr	This READ/WRITE bit-field permits a user to select the number consecutive times that the Receive STS-1 POH Processor because receive a given J1 Trace Message, before it is accepted described below.					
	Nici	* SIO	The Receive STS-1 POH Processor block accepts the J Message after it has received it the third time in succession.					
	oroche	5,40		SONET POH Processor block accepts the J1 s received in the fifth time in succession.				
2	Message Type	R/O	Message Alignme	nt Type:				
	Ti datid			E bit-field permits a user to specify have the H Processor block will locate the boundary of the as indicated below.				
			0 - Message bound	lary is indicated by "Line Feed".				
				dary is indicated by the presence of a "1" in the yte (within the J1 Trace Message).				
1 – 0	Message Length[1:0]	R/W	J1 Message Lengt	h[1:0]:				
			These READ/WRITE bit-fields permit the user to specify the length of the J1 Trace Message, that the Receive STS-1 POH Processor block will receive. The relationship between the content of these bit-fields and the corresponding J1 Trace Message Length is presented below.					
			MSG LENGTH	Resulting J1 Trace Message Length				
		l						

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev	ъ	n	n
Rev	4.	U.	v.

	01	16 Bytes	
	10/11	64 Bytes	

The product or products mentioned in this deline of the product of products of being manufactured. The product are no ordered (OBS)

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 553: Receive STS-1 Path - Pointer Value - Byte 1 (Address Location= 0xN1A6)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Current_Po MSB					
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 2	Unused	R/O	
1 – 0	Current_Pointer_Value_MSB[7:0]	R/O	Current Pointer Value – MSB:
			These READ-ONLY bit-fields, along with that from the "Receive STS-1 Path —Pointer Value — Byte 0" Register combine to reflect the current value of the pointer that the "Receive STS-1 POH Processor" block is using to locate the SPE within the incoming STS-1 data stream. Note: These register bits comprise the Upper Byte value of the Pointer Value.

Table 554: Receive STS-1 Path – Pointer Value – Byte 0 (Address Location= 0xN1A7)

Віт 7	Віт 6	Віт 5	Віт 4 9 Віт 3	Віт 2	Віт 1	Віт 0		
	Current_Pointer_Value_LSB[7:0]							
R/O	R/O	R/O	R/O R/O	R/O	R/O	R/O		
0	0	0	0 0	0	0	0		

BIT NUMBER	Name Name	TYPE	DESCRIPTION
7 – 0	Current_Pointer_Value_LSB[7:0]	R/O	Current Pointer Value – LSB:
	The progreet not		These READ-ONLY bit-fields, along with that from the "Receive STS-1 Path – Pointer Value – Byte 1" Register combine to reflect the current value of the pointer that the "Receive STS-1 POH Processor" block is using to locate the SPE within the incoming STS-1 data stream.
	o's and		Note: These register bits comprise the Lower Byte value of the Pointer Value.

rience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 555: Receive STS-1 Path – AUTO AIS Control Register (Address Location= 0xN1BB)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Transmit AIS-P (Down- stream) Upon C2 Byte Unstable	Transmit AIS-P (Down- stream) Upon UNEQ-P	Transmit AIS-P (Down- stream) Upon PLM- P	Transmit AIS-P (Down- stream) Upon J1 Message Unstable	Transmit AIS-P (Down- stream) upon TIM-P	Transmit AIS-P (Down- stream) upon LOP-P	Transmit AIS-P (Down- stream) Enable
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	Description
7	Unused	R/O	thille
6	Transmit AIS-P	R/W	Transmit Path AIS upon Detection of Unstable C2 Byte:
	(Downstream) upon C2 Byte Unstable		This READ/WRITE bit-field permits the user to configure the Receive STS-1 POH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Transmit SONET POH Processor blocks), anytime it detects an Unstable C2 Byte condition in the "incoming" STS-1 data-stream. 0 – Does not configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream"
			traffic) whenever it detects an "Unstable C2 Byte" condition.
			1 – Configures the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects an "Unstable C2 Byte" condition.
		ct of	Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
5	Transmit AIS-P (Downstream) upon UNEQ-P	R/W	Transmit Path AIS upon Detection of Path-Unequipped Defect (UNEQ-P):
	UNEQ-P ON A TANK	dnay	This READ/WRITE bit-field permits the user to configure the Receive STS-1 POH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Transmit SONET POH Processor blocks), anytime it declares an UNEQ-P condition.
	*		0 – Does not configure the Receive STS-1 POH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the UNEQ-P defect.
			1 – Configures the Receive STS-1 POH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the UNEQ-P defect.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
4	Transmit AIS-P (Downstream) upon	R/W	Transmit Path AIS upon Detection of Path-Payload Label Mismatch Defect (PLM-P):
	PLM-P		This READ/WRITE bit-field permits the user to configure the Receive STS-1 POH Processor block to automatically transmit a Path AIS

			(AIS-P) Indicator via the "downstream" traffic (e.g., towards the
			Transmit SONET POH Processor blocks), anytime it declares an PLM-P condition.
			0-Does not configure the Receive STS-1 POH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the PLM-P defect.
			1 – Configures the Receive STS-1 POH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the PLM-P defect.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
3	Transmit AIS-P	R/W	Transmit Path AIS upon Detection of Unstable 1 Message:
	(Downstream) upon J1 Message Unstable		This READ/WRITE bit-field permits the user to configure the Receive STS-1 POH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Transmit SONET POH Processor blocks), anytime it detects an Unstable J1 Message condition in the "incoming" STS-1 data-stream.
			0 – Does not configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects an "Unstable J1 Message" condition.
			1 – Configures the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects an "Unstable J1 Message" condition.
		or	Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
2	Transmit AIS-P (Downstream) upon TIM-P	R/W	Transmit Path AIS upon Detection of Path-Trace Identification Message Mismatch Defect (TIM-P):
	oroduc	etano	This READ/WRITE bit-field permits the user to configure the Receive STS-1 POH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Transmit SONET POH Processor blocks), anytime it declares a TIM-P condition.
	Theatand		0-Does not configure the Receive STS-1 POH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the TIM-P defect.
	♂		1 – Configures the Receive STS-1 POH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the TIM-P defect.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
1	Transmit AIS-P	R/W	Transmit Path AIS upon Detection of Loss of Pointer (LOP-P):
	(Downstream) upon LOP-P		This READ/WRITE bit-field permits the user to configure the Receive STS-1 POH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Transmit SONET POH Processor blocks), anytime it declares an LOP-P condition.
			0 - Does not configure the Receive STS-1 POH Processor block to

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the LOP-P defect.
			1 – Configures the Receive STS-1 POH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the LOP-P defect.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
0	Transmit AIS-P (Downstream) Enable	R/W	Automatic Transmission of AIS-P Enable:
	(Downstream) Linable		This READ/WRITE bit-field serves two purposes.
			It permits the user to configure the Receive STS-1 POH Processor block to automatically transmit the Path AIS indicator, via the downstream traffic (e.g., towards the Transmit SONET POH Processor blocks), upon detection of an UNEQ P, PLM-P, LOP-P or LOS conditions.
			It also permits the user to configure the Receive STS-1 POH Processor block to automatically transmit a Path (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Transmit SONET POH Processor blocks) anytime it detects an AIS-P condition in the "incoming " STS-1 data-stream.
			0 - Configures the Receive STS-1 POH Processor block to NOT automatically transmit the AIS-P indicator (via the "downstream" traffic) upon detection of any of the "above-mentioned" conditions.
			1 – Configures the Receive STS-1 POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) upon detection of any of the "above-mentioned" condition.
		्राठ	Note: The user must also set the corresponding bit-fields (within this register) to "1" in order to configure the Receive STS-1 ROH Processor block to automatically transmit the AIS-P indicator upon detection of a given a
	Thedata	id may	not be

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 556: Receive STS-1 Path – SONET Receive Auto Alarm Register – Byte 0 (Address Location= 0xN1C3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Transmit AIS-P (via Downstream STS-1s) upon LOP-P	Transmit AIS-P (via Downstream STS-1s) upon PLM-P	Transmit AIS-P (via Downstream STS-1s) upon LCD-P	Transmit AIS-P (via Downstream STS-1s) upon UNEQ-P	Transmit AIS-P (via Downstream STS-1s) upon TIM-P	Transmit AIS-P (via Downstream STS-1s) upon AIS-P	Transmit DS3 AIS (via Downstream DS3) upon PDI-P
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Unused	R/O	"th' ure
6	Transmit AIS-P (via	R/W	Transmit AIS-P (via Downstream STS-1s) upon LOP-P
	Downstream STS-1s) upon LOP-P		This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the LOP-P defect. 0 — Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the LOP-P defect.
	, yc	OIP	1 Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the LOP-P defect.
5	Transmit AIS-P (via	ZR/W	Transmit AIS-P (via Downstream STS-1s) upon PLM-P:
	Transmit AIS-P (via Downstream STS-1s) upon PLM-P	lay	This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal, anytime the Receive STS-1 POH Processor block declares the PLM-P defect.
	♂		0 – Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the PLM-P defect.
			1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the PLM-P defect.
4	Transmit AIS-P (via	R/W	Transmit AIS-P (via Downstream STS-1s) upon LCD-P:
	Downstream STS-1s) upon LCD-P		This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal, anytime the Receive SONET POH

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			Processor block declares the LCD-P defect.
			0 - Does not configure the corresponding Transmit STS-1 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive SONET POH Processor block declares the LCD-P defect.
			1 – Configures the corresponding Transmit STS-1 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive SONET POH Processor block declares the LCD-P defect.
3	Transmit AIS-P (via	R/W	Transmit AIS-P (via Downstream STS-1s) upon UNEQ-P:
	Downstream STS-1s) upon UNEQ-P		This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal, (within the outbound STS-3 signal) anytime the Receive STS-1 POH Processor block declares the UNEQ-P defect.
			0 - Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the UNEQ-P defect.
			1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the UNEQ-P defect.
2	Transmit AIS-P (via Downstream STS-1s) upon TIM-P	R/W	Transmit AlS-P (via Downstream STS-1s) upon TIM-P: This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the TIM-P defect.
	a produce t		O - Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the TIM-P defect.
	The date	da	1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the TIM-P defect.
1	Transmit AIS-P (via	R/W	Transmit AIS-P (via Downstream STS-1s) upon AIS-P:
	Downstream STS-1s) upon AIS-P		This READ/WRITE bit-field permits the user to configure the Transmit SONET POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the AIS-P defect.
			0 - Does not configure the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal (within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the AIS-P defect.





3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			1 – Configures the corresponding Transmit SONET POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal A(within the outbound STS-3 signal), anytime the Receive STS-1 POH Processor block declares the AIS-P defect.
0	Unused	R/O	

The product are no products mentioned in this tred

EXAR Experience Our Connectivit

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 557: Receive STS-1 Path – Receive J1 Byte Capture Register (Address Location= 0xN1D3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
J1_Byte_Captured_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	J1_Byte_Captured_Value[7:0]	R/O	J1 Byte Captured Value[7:0]
			These READ-ONLY bit-fields contain the value of the J1 byte, within the most recently received STS-1 frame.
			This particular value is stored in this register for one STS-1 frame period. During the next STS-1 frame period, this value will be overridden with a new J1 byte value.

Table 558: Receive STS-1 Path – Receive B3 Byte Capture Register (Address Location= 0xN1D7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт	Віт 2	Віт 1	Віт 0	
B3_Byte_Captured_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	0	0	0	5 60 00	0	0	0	

BIT NUMBER	Name	TYPE	DESCRIPTION
7 – 0	B3_Byte_Captured_Value[7:0]	R/O	B3 Byte Captured Value[7:0]
	oduce	STORY OF THE PROPERTY OF THE P	These READ-ONLY bit-fields contain the value of the B3 byte, within the most recently received STS-1 frame. This particular value is stored in this register for one STS-1 frame period. During the next STS-1 frame period, this value will be overridden with a new B3 byte value.
	The Plash and ma	4	

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 559: Receive STS-1 Path - Receive C2 Byte Capture Register (Address Location= 0xN1DB)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
C2_Byte_Captured_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	C2_Byte_Captured_Value[7:0]	R/O	C2 Byte Captured Value[7:0]
			These READ-ONLY bit-fields contain the value of the C2 byte, within the most recently received STS-1 frame. This particular value is stored in this register for one STS-1 frame period. During the next STS-1 frame period, this value will be overridden with a new C2 byte value.

Table 560: Receive STS-1 Path – Receive G1 Byte Capture Register (Address Location= 0xN1DF)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
	G1_Byte_Captured_Value[7:0]										
R/O	R/O	R/O	R/O	Ø RØ	R/O	R/O	R/O				
0	0	0	0	0 0	0	0	0				

BIT NUMBER	Name	Туре	DESCRIPTION
7 – 0	G1_Byte_Captured_Value[7:0]	R/O	G1 Byte Captured Value[7:0]
	ote	0	These READ-ONLY bit-fields contain the value of the G1 byte, within the most recently received STS-1 frame.
	ducter	the	This particular value is stored in this register for one STS-1 frame period. During the next STS-1 frame period, this value will be overridden with a new G1 byte value.
	The proshed in		

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 561: Receive STS-1 Path – Receive F2 Byte Capture Register (Address Location=0xN1E3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
F2_Byte_Captured_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O			
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	TYPE	DESCRIPTION
7 – 0	F2_Byte_Captured_Value[7:0]	R/O	F2 Byte Captured Value[7:0]
			These READ-ONLY bit-fields contain the value of the F2 byte, within the most recently received STS-1 frame.
			This particular value is stored in this register for one STS-1 frame period. During the next STS-1 frame period, this value will be overridden with a new F2 byte value.

Table 562: Receive STS-1 Path – Receive H4 Byte Capture Register (Address Location= 0xN1E7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
H4_Byte_Captured_Value[7:0]									
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
0	0	0	0	6,00	0	0	0		

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	H4_Byte_Captured_Value[7:0]	R/O	H4 Byte Captured Value[7:0]
	. (6	N VIC	These READ-ONLY bit-fields contain the value of the H4 byte, within the most recently received STS-1 frame.
	Auct.	ste "	This particular value is stored in this register for one STS-1 frame period. During the next STS-1 frame period, this value
	,00 00	70,	will be overridden with a new H4 byte value.
	e plashe	4	
	The Stady		
	all		

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 563: Receive STS-1 Path – Receive Z3 Byte Capture Register (Address Location= 0xN1EB)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Z3_Byte_Captured_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O		
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Z3_Byte_Captured_Value[7:0]	R/O	Z3 Byte Captured Value[7:0]
			These READ-ONLY bit-fields contain the value of the Z3 byte, within the most recently received STS-1 frame.
			This particular value is stored in this register for one STS-1 frame period. During the next STS-1 frame period, this value will be overridden with a new Z3 byte value.

Table 564: Receive STS-1 Path – Receive Z4 (K3) Byte Capture Register (Address Location= 0xN1EF)

					/		
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Z	4(K3)_Byte_Cap	ptured_Value[7:	0]		
R/O	R/O	R/O	R/O 《	R/O	R/O	R/O	R/O
0	0	0	0	0,000	0	0	0

BIT NUMBER	Name	TYPE	0	DESCRIPTION
7 – 0	Z4(K3)_Byte_Captured_Value[70]	R/O	Z4 (ł	(3) Byte Captured Value[7:0]
	Corto	Oto		e READ-ONLY bit-fields contain the value of the Z4 byte, within the most recently received STS-1 frame.
	oducit are b	8	frame	particular value is stored in this register for one STS-1 e period. During the next STS-1 frame period, this will be overridden with a new Z4 (K3) byte value.

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 565: Receive STS-1 Path – Receive Z5 Byte Capture Register (Address Location= 0xN1F3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Z5_Byte_Captured_Value[7:0]								
R/O R/O R/O R/O R/O						R/O	R/O	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Z5_Byte_Captured_Value[7:0]	R/O	Z5 Byte Captured Value[7:0]
			These READ-ONLY bit-fields contain the value of the Z5 byte, within the most recently received STS-1 frame.
			This particular value is stored in this register for one STS-1 frame period. During the next STS-1 frame period, this value will be overridden with a new Z5 byte value.
	The product	or protest	frame period. During the next \$78-1 frame period, this value will be overridden with a new Z5 byte value.

1.12 DS3/E3 FRAMER BLOCK

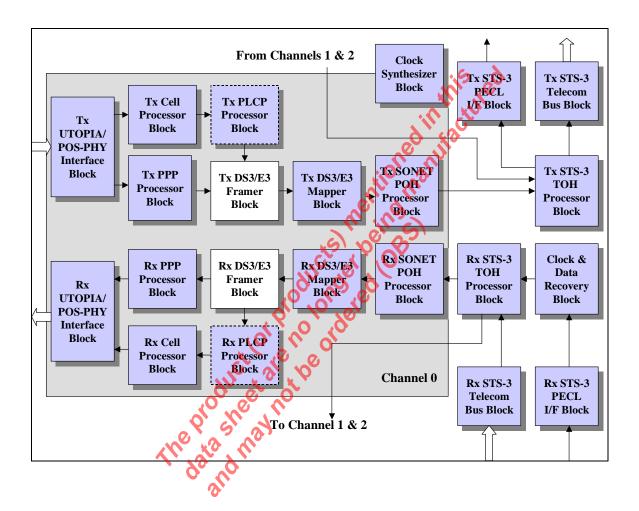
3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

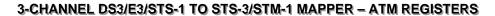
The register map for the DS3/E3 Framer Block is presented in the Table below. Additionally, a detailed description of each of the "DS3/E3 Framer" block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33, with the "DS3/E3 Framer Block "highlighted" is presented below in

Figure 13.

Figure 13: Illustration of the Functional Block Diagram of the XRT94L33, with the DS3/E3 Framer Block "High-lighted







1.12.1 DS3/E3 FRAMER BLOCK REGISTER

Table 566: DS3/E3 Framer Block Control Register Map

Individual Register Address	Address Location	REGISTER NAME	DEFAULT VALUES
0x00	0xN300	Operating Mode Register	0x23
0x01	0xN301	I/O Control Register	0xA0
0x02 - 0x03	0xN302, 0xN303	Reserved	0x00
0x04	0xN304	Block Interrupt Enable Register	0x00
0x05	0xN305	Block Interrupt Status Register	0x00
0x06 - 0x0B	0xN306 – 0xN30B	Reserved	0x00
0x0C	0xN30C	Test Register	0x00
0x0D - 0x0F	0xN30D - 0xN30F	Reserved	0x00
0x10	0xN310	RxDS3 Configuration and Status Register	0x02
		RxE3 Configuration and Status Register #1 + G.832	
		RxE3 Configuration and Status Register # 1 – G.751	
0x11	0xN311	RxDS3 Status Register	0x67
		RxE3 Configuration and Status Register # 2 – G.832	
		RxE3 Configuration and Status Register # 2 – G.751	
0x12	0xN312	RxDS3 Interrupt Enable Register	0x00
		RxE3 Interrupt Enable Register # 1 – G.832	
		RxE3 interrupt Enable Register # 1 – G.751	
0x13	0xN313	RxDS3 Interrupt Status Register	0x00
		RxE3 Interrupt Enable Register # 2 – G.832	
		RxE3 Interrupt Enable Register # 2 – G.751	
0x14	0xN314	RxDS3 Sync Detect Enable Register	0x00
		RxE3 Interrupt Status Register # 1 – G.832	
		RxE3 Interrupt Status Register # 1 – G.751	
0x15	0xN315	RxE3 Interrupt Status Register # 2 – G.832	0x00
		RxE3 Interrupt Status Register # 2 – G.751	
0x16	0xN316	RxDS3 FEAC Register	0x7E
0x17	0xN317	RxDS3 FEAC Interrupt Enable/Status Register	0x00
0x18	0xN318	RxDS3 LAPD Control Register	0x00
		RxE3 LAPD Control Register	
0x19	0xN319	RxDS3 LAPD Status Register	0x00

INDIVIDUAL REGISTER ADDRESS	Address Location	REGISTER NAME	DEFAULT VALUES
		RxE3 LAPD Status Register	
0x1A	0xN31A	RxE3 NR Byte Register – G.832	0x00
		RxE3 Service Bit Register – G.751	
0x1B	0xN31B	RxE3 GC Byte Register – G.832	0x00
0x1C	0xN31C	RxE3 TTB-0 Register – G.832	0x00
0x1D	0xN31D	RxE3 TTB-1 Register – G.832	0x00
0x1E	0xN31E	RxE3 TTB-2 Register – G.832	0x00
0x1F	0xN31F	RxE3 TTB-3 Register – G.832	0x00
0x20	0xN320	RxE3 TTB-4 Register – G.832	0x00
0x21	0xN321	RxE3 TTB-5 Register – G.832	0x00
0x22	0xN322	RxE3 TTB-6 Register – G.832	0x00
0x23	0xN323	RxE3 TTB-7 Register – G.832	0x00
0x24	0xN324	RxE3 TTB-8 Register – G.832	0x00
0x25	0xN325	RxE3 TTB-9 Register – 6,832	0x00
0x26	0xN326	RxE3 TTB-10 Register – G.832	0x00
0x27	0xN327	RxE3 TTB-11 Register - G.832	0x00
0x28	0xN328	RxE3 TTB-12 Register - C.832	0x00
0x29	0xN329	RxE3 TTB 13 Register - G.832	0x00
0x2A	0xN32A	RxE3TTB-14 Register – G.832	0x00
0x2B	0xN32B	RxE3 TTB-15 Register – G.832	0x00
0x2C	0xN32C	RxE3 SSM Register – G.832	0x00
0x2D - 0x2E	0xN32D - 0xN32E	Reserved	0x00
0x2F	0xN32F	RxDS3 Pattern Register	0x0C
0x30	0xN330	TxDS3 Configuration Register	0x00
		TxE3 Configuration Register – G.832	
		TxE3 Configuration Register – G.751	
0x31	0xN331	TxDS3 FEAC Configuration and Status Register	0x00
0x32	0xN332	TxDS3 FEAC Register	0x7E
0x33	0xN333	TxDS3 LAPD Configuration Register	0x08
		TxE3 LAPD Configuration Register	
0x34	0xN334	TxDS3 LAPD Status/Interrupt Register	0x00
		TxE3 LAPD Status/Interrupt Register	

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS



Rev 2.0.0

INDIVIDUAL REGISTER ADDRESS	Address Location	REGISTER NAME	DEFAULT VALUES
0x35	0xN335	TxDS3 M-Bit Mask Register	0x00
		TxE3 GC Byte Register – G.832	
		TxE3 Service Bits Register – G.751	
0x36	0xN336	TxDS3 F-Bit Mask # 1 Register	0x00
		TxE3 MA Byte Register – G.832	
0x37	0xN337	TxDS3 F-Bit Mask # 2 Register	0x00
		TxE3 NR Byte Register – G.832	
0x38	0xN338	TxDS3 F-Bit Mask # 3 Register	0x00
		TxE3 TTB-0 Register – G.832	
0x39	0xN339	TxDS3 F-Bit Mask # 4 Register	0x00
		TxE3 TTB-1 Register – G.832	
0x3A	0xN33A	TxDS3 F-Bit Mask # 3 Register TxE3 TTB-0 Register – G.832 TxDS3 F-Bit Mask # 4 Register TxE3 TTB-1 Register – G.832 TxE3 TTB-2 Register – G.832	0x00
0x3B	0xN33B	TxE3 TTB-3 Register – G.832	0x00
0x3C	0xN33C	TxE3 TTB-4 Register – G.832	0x00
0x3D	0xN33D	TxE3 TTB-5 Register – G.832	0x00
0x3E	0xN33E	TxE3 TTB-6 Register 6.832	0x00
0x3F	0xN33F	TxE3 TTB-7 Register - G.832	0x00
0x40	0xN340	TxE3 TTB-8 Register G.832	0x00
0x41	0xN341	TxE3 TTB-9 Register – G.832	0x00
0x42	0xN342	TxE3 TTB-10 Register - G.832	0x00
0x43	0xN343	TxE3TTB-11 Register – G.832	0x00
0x44	0xN344	TXE3 TTB-12 Register – G.832	0x00
0x45	0xN345	Tx E3 TTB-13 Register – G.832	0x00
0x46	0xN346	TxE3 TTB-14 Register – G.832	0x00
0x47	0xN347	TxE3 TTB-15 Register – G.832	0x00
0x48	0xN348	TxE3 FA1 Error Mask Register – G.832	0x00
		TxE3 FAS Error Mask Upper Register – G.751	
0x49	0xN349	TxE3 FA2 Error Mask Register – G.832	0x00
		TxE3 FAS Error Mask Lower Register – G.751	
0x4A	0xN34A	TxE3 BIP-8 Mask Register – G.832	0x00
		TxE3 BIP-4 Mask Register – G.751	
0x4B	0xN34B	Tx SSM Register – G.832	0x00
0x4C	0xN34C	TxDS3 Pattern Register	0x0C

INDIVIDUAL REGISTER ADDRESS	Address Location	REGISTER NAME	DEFAULT VALUES
0x4D	0xN34D	Receive DS3/E3 AIS/PDI-P Alarm Enable Register	0x00
0x4E	0xN34E	PMON Excessive Zero Count Register - MSB	0x00
0x4F	0xN34F	PMON Excessive Zero Count Register - LSB	0x00
0x50	0xN350	PMON LCV Event Count Register - MSB	0x00
0x51	0xN351	PMON LCV Event Count Register - LSB	0x00
0x52	0xN352	PMON Framing Bit/Byte Error Count Register - MSB	0x00
0x53	0xN353	PMON Framing Bit/Byte Error Count Register - LSB	0x00
0x54	0xN354	PMON Parity Error Event Count Register - MSB	0x00
0x55	0xN355	PMON Parity Error Event Count Register (LSB)	0x00
0x56	0xN356	PMON FEBE Event Count Register - MSB	0x00
0x57	0xN357	PMON FEBE Event Count Register LSB	0x00
0x58	0xN358	PMON CP-Bit Error Count Register - MSB	0x00
0x59	0xN359	PMON CP-Bit Error Count Register LSB	0x00
0x5A	0xN35A	PMON PLCP BIP-8 Error Count Register – MSB	0x00
0x5B	0xN35B	PMON PLCP BIP-8 Error Count Register – LSB	0x00
0x5C	0xN35C	PMON PLCP Framing Byte Error Count Register – MSB	0x00
0x5D	0xN35D	PMON PLCP Framing Byte Error Count Register – LSB	0x00
0x5E	0xN35E	PMON PLCP FEBE Error Count Register – MSB	0x00
0x5F	0xN35F	PMON PLCP FEBE Error Count Register – LSB	0x00
0x60 - 0x67	0xN360 – 0xN367	Reserved	0x00
0x68	0xN3680	PMON PRBS Bit Error Count Register - MSB	0x00
0x69	0xN369	PMON PRBS Bit Error Count Register - LSB	0x00
0x6A - 0x6B	0xN36A – 0xN36B	Reserved	0x00
0x6C	0xN36C	PMON Holding Register	0x00
0x6D	0xN36D	One Second Error Status Register	0x00
0x6E	0xN36E	One Second – LCV Count Accumulator Register - MSB	0x00
0x6F	0xN36F	One Second – LCV Count Accumulator Register - LSB	0x00
0x70	0xN370	One Second – Parity Error Accumulator Register - MSB	0x00
0x71	0xN371	One Second – Parity Error Accumulator Register - LSB	0x00
0x72	0xN372	One Second – CP Bit Error Accumulator Register - MSB	0x00
0x73	0xN373	One Second – CP Bit Error Accumulator Register – LSB	0x00

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS



Rev 2.0.0

INDIVIDUAL REGISTER ADDRESS	Address Location	REGISTER NAME	DEFAULT VALUES
0x74 – 0x7F	0xN374 – 0xN37F	Reserved	0x00
0x80	0xN380	Line Interface Drive Register	0x00
0x81	0xN381	Reserved	0x00
0x82	0xN382	Reserved	0x00
0x83	0xN383	TxLAPD Byte Count Register	0x00
0x84	0xN384	RxLAPD Byte Count Register	0x00
0x85 – 0x8F	0xN385 – 0xN38F	Reserved	0x00
0x90	0xN390	Receive PLCP Configuration and Status Register	0x06
0x91	0xN391	Receive PLCP Interrupt Enable Register	0x00
0x92	0xN392	Receive PLCP Interrupt Status Register	0x00
0x93 – 0x97	0xN393 – 0xN397	Reserved	0x00
0x98	0xN398	Transmit PLCP A1 Byte Error Mask Register	0x00
0x99	0xN399	Transmit PLCP A2 Byte Error Mask Register	0x00
0x9A	0xN39A	Transmit PLCP BIP-8 Error Mask Register	0x00
0x9B	0xN39B	Transmit PLCP G1 Byte Register	0x00
0x9C - 0xAF	0xN39C - 0xN3AF	Reserved	0x00
0xB0	0xN3B0	Transmit LAPD Memory Indirect Address Register	0x00
0xB1	0xN3B1	Transmit LAPD Memory Indirect Data Register	0x00
0xB2	0xN3B2	Receive LAPD Memory Indirect Address Register	0x00
0xB3	0xN3B3	Receive LAPD Memory Indirect Data Register	0x00
0xB4 – 0xEF	0xN3B4 - 0xN3EF	Reserved	0x00
0xF0	0xN3F0	Receive DS3/E3 Configuration Register – Secondary Frame Synchronizer Block – Byte 1	0x10
0xF1	0xN3F1	Receive DS3/E3 Configuration Register – Secondary Frame Synchronizer Block – Byte 0	0x10
0xF2	0xN3F2	Receive DS3/E3 AlS/PDI-P Alarm Enable Register – Secondary Frame Synchronizer Block	0x00
0xF3 - 0xF7	0xN3F3 – 0xN3F7	Reserved	0x00
0xF8	0xN3F8	Receive DS3/E3 Interrupt Enable Register – Secondary Frame Synchronizer Block	0x00
0xF9	0xN3F9	Receive DS3/E3 Interrupt Status Register – Secondary Frame Synchronizer Block	0x00



1.12.2 **DS3/E3 FRAMER BLOCK REGISTER DESCRIPTION**

Table 567: Operating Mode Register (Address Location= 0xN300)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Local Loop Back	IsDS3	Internal LOS Enable	RESET	Direct Map	Frame Format	TimRef	Sel[1:0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	1	0	1	1

BIT NUMBER	NAME	Түре	DESCRIPTION				
7	Local Loop	R/W	Framer Block Local Loop-back Mode:	>			
	Back		This READ/WRITE bit field configures the Frame Generator/Frame Synchronizer blocks to operate in the Local Loop-back Mode. If the Frame Generator/Frame Synchronizer blocks are configured to operate in the Local Loop-back Mode, then the TxPOS n, TxNEG n and TxLineClk signal is internally looped back into the RxPOS n, RxNEG n and RxLineClk signals. 0 – Normal Operating Mode 1 – Local Loop-back Mode				
6	IsDS3	R/W	Is DS3 Mode:				
			This READ/WRITE bit-field, along with Bit 2 (to configure the Frame Generator/Frame Syrappropriate framing format. The relationship Bit 2 and the resulting framing format is present.	nchronizer block to operate in the between the state of this bit-field,			
			Bit 6 (IsDS3) Bit 2 (Frame Format)	Framing Format			
			0 0 0	E3, ITU-T G.751			
			9/100 1	E3, ITU-T G.832			
		di	0	DS3, C-bit Parity			
		il she	1	DS3, M13			
5	Internal LOS Enable	R/W	Internal LOS Enable:				
	Enable	SINO	This READ/WRITE bit-field permits the user LOS Detector", within the Frame Synchronize				
			0 – Internal LOS Detector is disabled.				
			1 – Internal LOS Detector is enabled.				
4	RESET	R/W	Software RESET Input:				
			A "0" to "1" transition in this bit-field comm Channel. Once the user executes a Softwa internal state machines will be reset; and the execute a "Reframe" operation.	are reset to the frame, all of the			
			Note: For a Software Reset, the content not be reset to their default values.	s of the Command Register will			
3	Direct Map	R/W	Direct Map:				
			The READ/WRITE bit-field permits the user	to configure the DS3/E3 framer			

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			block to bypass the PLCP processor block.					
			0 – PLCP processor block is bypassed					
			1 – PLCP processor block is used in the design					
2	Frame Format	R/W	Frame Format:					
			This READ/WRITE bit-field, along with Bit 6 (IsDS3), permits the user to configure the Frame Generator/Frame Synchronizer block to operate in the appropriate framing format. The relationship between the state of this bit-field, Bit 2 and the resulting framing format is presented below.					
			Bit 6 (IsDS3)	Bit 2 (Frame Format)	Framing Format			
			0	0	E3, ITU-T G.751			
			0	1	E3, ITU-T G.832			
			1	0	DS3, C-bit Parity			
			1	1 11 6	DS3, M13			
1 - 0	TimRefSel[1:0]	R/W	Time Reference	e Select:				
			These two READ source and the fra presented below.	/WRITE bit-fields permit the aming-alignment source for	e user to define both the timing the Frame Generator block, as			
			TimRefSel[1:0] Timing Reference	Framing Reference			
			oo duc	Loop-Timing (Timing is taken from the Frame Synchronizer block)	Asynchronous			
			01 pt 10	Transmit Clock Source for the Frame Generator block				
		, co	de ale le	Transmit Clock Source for the Frame Generator block	1 1			
	N.	is of a	May	Transmit Clock Source for the Frame Generator block				

Table 568: I/O Control Register (Address Location= 0xN301)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Disable TxLOC	LOC	Disable RxLOC	AMI/Zero- Suppression	Single Rail/Dual Rail Select	DS3/E3 CLK_OUT Invert:	DS3/E3 CLK_IN Invert:	Reframe
R/W	R/O	R/W	R/W	R/O	R/O	R/O	R/W
1	0	1	0	1	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION			
7	Disable	R/W	Disable Transmit Loss of Clock Feature:			
	TxLOC		This READ/WRITE bit-field permits the user to either enable or disable the "Transmit Loss of Clock" feature.			
			If this feature is enabled, then the DS3/E3 Framer block will enable some circuitry that will terminate the current READ or WRITE access (to the Microprocessor Interface), if a "Loss of Transmit (or Frame Generator) Clock Event were to occur.			
			The intent behind this feature is to prevent any READ/WRITE accesses (to the DS3/E3 Framer block) from "handing" in the event of a "Loss of Clock" event.			
			0 – Enables the "Transmit Loss of Clock" feature.			
			1 - Disables the "Transmit Loss of Clock" feature.			
6	LOC	R/O	Loss of Clock Indicator:			
			This READ-ONLY bit-field indicates that the Channel has experiences a Loss of Clock event.			
5	Disable	R/W	Disable Receive Loss of Clock Feature			
	RxLOC		This READ/WRITE bit-field permits the user to either enable or disable the "Receive Loss of Clock" feature.			
		٨	If this feature is enabled, then the DS3/E3 Framer block will enable some circuitry that will terminate the current READ or WRITE access (to the Microprocessor Interface), if a Loss of Receiver (or Frame Synchronizer) Clock Event were to occur.			
		oto	The intent behind this feature is to prevent any READ/WRITE accesses (to the DS3/E3 Framer block) from "hanging" in the event of a "Loss of Clock" event.			
	N	0,0	0 - Enables the "Receive Loss of Clock" feature.			
		19	Disables the "Receive Loss of Clock" feature.			
4	AMI/Zero-	0	AMI/Zero-Suppression Line Code Select :			
	Suppressi on		This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer Block (associated with channel N) to operate in either the AMI or B3ZS/HDB3 Line Code; as described below.			
			0 - Configures the DS3/E3 Framer Channel to operate in the B3ZS/HDB3 Line Code.			
			1- Configures the DS3/E3 Framer Channel to operate in the AMI Line Code.			
3	Single		Single-Rail/Dual-Rail Select:			
	Rail/Dual Rail Select		This READ/WRITE bit-field permits the user to configure the Primary Frame Synchronizer/Frame Generator blocks (within the XRT94L33) to operate in either the "Single-Rail" or "Dual-Rail" Mode. If the user configures the Primary Frame Synchronizer and Frame Generator blocks to operate in the Single-Rail mode, then the following will happen.			
			• The Primary Frame Synchronizer block will accept data (from the LIU IC) in a			

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Single-Rail Manner.	
The Frame Generator block will output data (to the LIU IC) in a Single-Rail Mail	ner.
If the user configures the Primary Frame Synchronizer and Frame Generator by to operate in the Dual-Rail mode, then the following will happen.	ocks
The Primary Frame Synchronizer block will accept data (from the LIU IC) in a I Rail Manner.	ual-
• The Frame Generator block will output data (to the LIU IC) in a Dual-Rail Manr	er.
0 – Configures the Primary Frame Synchronizer/Frame Generator to operate in Dual-Rail Mode.	the
1 – Configures the Primary Frame Synchronizer/Frame Generator to operate in Single-Rail Mode.	the
Note: This bit-field is only valid if the Primary Frame Synchronizer block has configured to operate in the Ingress Direction, and if the Frame Gene block has been configured to operate in the Egress Direction.	
2 DS3/E3_ DS3/E3_CLK_OUT Invert:	
CLK_OUT Invert: This READ/WRITE bit-field permits the user to configure the DS3/E3 F Generator block (of Channel n), within the XRT94L33, to update the "TxDS3PO output pins (pin B18, G24, AG9) upon either the rising or falling edg "TxDS3LineClk_n" (pin C17, E25, AF10)	3_n"
0 - "TxDS3POS_n" is updated upon the rising edge of "TxDS3LineClk_n". The should insure that the LIU IC will sample "TxDS3POS_n" upon the falling edge "TxDS3LineClk_n".	
1 – "TxDS3POS_n" is updated upon the falling edge of "TxDS3LineClk_n". The should insure that the LIU IC will sample "TxDS3POS_n" upon the rising edge of "TxDS3LineClk_n".	e of
Note: This bit-field is only active if the Frame Generator block has configured to operate in the Egress Path.	oeen
1 DS3/E3_ R/O DS3/E3/STS1_CLK_IN Invert:	
CLK_IN Invert: This READ/WRITE pit-field permits the user to configure Channel n, withir XRT94L33 to sample and latch the "RxDS3POS_n" input pins (pin B14. AG15)" upon either the rising or falling edge of "RxDS3LineClk_n" (pin D14, AF14)	C21.
0 – "RxDS3POS_n" is sampled upon the falling edge of "RxDS3LineClk_n"	
"RxDS3POS_n" is sampled upon the rising edge of "RxDS3LineClk_n"	
0 Reframe R/W DS3/E3 Frame Synchronizer Block – Reframe Command:	
A "0" to "1" transition, within this bit-field commands the DS3/E3 F Synchronizer block (within Channel n) to exit the Frame Maintenance Mode, ar back and enter the Frame Acquisition Mode.	
Note: The user should go back and set this bit-field to "0" following execution the "Reframe" Command.	on of

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 569: Block Interrupt Enable Register (Address Location= 0xN304)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
DS3/E3 Frame Synch Block Interrupt Enable			Unused			DS3/E3 Frame Generator Block Interrupt Enable	One Second Interrupt
R/W	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	DS3/E3 Frame	R/W	DS3/E3 Frame Synchronizer Block Interrupt Enable:
	Synch Block Interrupt Enable		This READ/WRITE bit-field permits the user to enable or disable the Frame Synchronizer block for Interrupt Generation. If the user enables the Frame Synchronizer block (for Interrupt Generation) at the block level, the user still needs to enable the interrupts at the "Source" level, as well; in order for these interrupts to be enabled.
			However, if the user disables the Frame Synchronizer block (for Interrupt Generation) at the Block Level, then ALL Frame Synchronizer-related blocks are disabled. 0 – Frame Synchronizer block is Disabled for Interrupt Generation.
			1 - Frame Synchronizer block is enabled (at the Block level) for Interrupt Generation.
6 – 2	Unused	R/O	or lot are
1	DS3/E3 Frame Generator Block Interrupt Enable	R/W ON CONTROL OF CONT	DS3/E3 Frame Generator Block Interrupt Enable: This READ/WRITE bit-field permits the user to enable or disable the Frame Generator block for Interrupt Generation. If the user enables the Frame Generator block (for Interrupt Generation) at the block level, the user still needs to enable the interrupts at the "Source" level, as well; in order for these interrupts to be enabled. However, if the user disables the Frame Generator block (for Interrupt Generation) at the Block Level, then ALL Frame Generator-related blocks are disabled. 0 – Frame Generator block is Disabled for Interrupt Generation. 1 – Frame Generator block is Enabled (at the Block Level) for Interrupt Generation.
0	One Second Interrupt	R/W	One Second Interrupt Enable: This READ/WRITE bit-field permits the user to enable or disable the One-Second Interrupt, within Channel n. If the user enables this interrupt, then Channel n will generate an interrupt at one second intervals. 0 – One Second Interrupt is disabled. 1 – One Second Interrupt is enabled.

EXAR Experience Our Connectivi

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 570: Block Interrupt Status Register (Address Location= 0xN305)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
DS3/E3			Unused	DS3/E3	One Second		
Frame Sync Block Interrupt Status				Frame Generator Block Interrupt Status	Interrupt		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	DS3/E3 Frame Synch Block Interrupt Status	R/O	DS3/E3 Frame Synchronizer Block Interrupt Status: This READ-ONLY bit-field indicates whether or not a "DS3/E3 Frame Synchronizer Block"-related interrupt (within Channel n) is requesting interrupt service. 0 – The DS3/E3 Frame Synchronizer block (within Channel n) is NOT requesting any interrupt service. 1 – The DS3/E3 Frame Synchronizer block (within Channel n) is requesting interrupt service.
6 - 2	Unused	R/O	is beids
1	DS3/E3 Frame Generator Block Interrupt Status	R/O	DS3/E3 Frame Generator Block Interrupt Status: This READ-ONLY bit-field indicates whether or not a "DS3/E3 Frame Generator"—related interrupt (within Channel n) is requesting interrupt service. 0 — The DS3/E3 Frame Generator block (within Channel n) is NOT requesting any interrupt service. 1 — The DS3/E3 Frame Synchronizer block (within Channel n) is requesting interrupt service.
0	One Second Interrupt Status	RUR	One Second Interrupt Status This RESET-upon-READ bit-field indicates whether or not a "One Second" Interrupt (from Channel n) has occurred since the last read of this register. O – The One Second Interrupt has NOT occurred since the last read of this register. 1 – The One Second Interrupt has occurred since the last read of this register.

Table 571: Test Register (Address Location= 0xN30C)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
TxOHSrc	Unused		RxPRBS Lock	RxPRBS Enable	TxPRBS Enable	Unu	Jnused	
R/W	R/O	R/O	R/O	R/W	R/W	R/O	R/O	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7	TxOHSrc	R/W	Transmit Overhead Bit Source:
			This READ/WRITE bit-field permits the user to configure the Frame Generator to accept and insert overhead bits/bytes which are input via the "Payload Data Input Interface" block, as indicated below.
			0 – Overhead bits/bytes are internally generated by the Frame Generator block.
			1 – Overhead bits/byte data is accepted from the Payload Data Input Interface block.
			Note: This register bit applies to all framing formats that are supported by the Frame Generator block.
6 - 5	Unused	R/O	riot agit
4	RxPRBS	R/O	PRBS Lock Indicator:
	Lock		This READ-ONLY bit-field indicates whether or not the PRBS Receiver (within the Channel) has acquired "PRBS Lock" with the payload data of the incoming DS3 or E3 data stream.
			0 – PRBS Receiver does not have PRBS Lock with the incoming data stream.
			1 – PRBS Receiver does have PRBS Lock with the incoming data stream.
			Note: This bit field is not valid if the PRBS Receiver is disabled, or if the Frame Synchronizer block is bypassed.
З	RxPRBS Enable	R/W	Receive PRBS Enable: This READ/WRITE bit-field permits the user to either enable or disable the PRBS Receiver within the Frame Synchronizer block. Once the user enables the PRBS Receiver, then it will proceed to attempt to acquire and maintain pattern (or PRBS Lock) within the payload bits, within the incoming DS3 or E3 data stream.
		0	0 – Disables the PRBS Receiver.
		13/	1- Enables the PRBS Receiver.
		0 7	Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.
2	TxPRBS	R/W	Transmit PRBS Enable:
	Enable		This READ/WRITE bit-field permits the user to either enable or disable the PRBS Generator within the Frame Generator block. Once the user enables the PRBS Generator block, then it will proceed to insert a PRBS pattern into the payload bits, within the outbound DS3 or E3 data stream.
			0 – Disables the PRBS Generator.
			1 – Enables the PRBS Generator.
			Note: This bit-field is ignored if the Frame Generator block is by-passed.
1 - 0	Unused	R/O	

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS



Rev 2.0.0

1.12.3 RECEIVE DS3 RELATED REGISTERS

Table 572: RxDS3 Configuration and Status Register (Address Location= 0xN310)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
RxAIS	RxLOS	RxIdle	RxOOF	Unused	Framing with Valid P-Bits	F-Sync Algo	M-Sync Algo
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	1	0	0	1	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	RxAIS	R/O	Receive AIS Defect Indicator:
			This READ-ONLY bit-field indicates whether or not the Frame Synchronizer block is currently detecting the AIS pattern in its incoming path.
			0 – Frame Synchronizer block is NOT currently detecting an AIS pattern in its incoming path.
			1 - Frame Synchronizer block is currently detecting an AIS pattern in its incoming path.
6	RxLOS	R/O	Receive LOS Defect Indicator:
			This READ-ONLY bit-field indicates whether or not the Frame Synchronizer block is currently detecting the LOS condition, in its incoming path.
			0 – Frame Synchronizer block is NOT currently declaring an LOS condition in its incoming path.
			1 - Frame Synchronizer block is currently detecting an LOS condition in its incoming bath.
5	RxIdle	R/O	Receive Idle Signal Indicator:
		A	This READ-ONLY bit-field indicates whether or not the Frame Synchronizer block is currently detecting the DS3 Idle pattern, in its incoming path.
		400	0 — Frame Synchronizer block is NOT currently detecting the DS3 Idle Pattern, in its incoming path.
	×	000	1 – Frame Synchronizer block is currently detecting the DS3 Idle Pattern in its incoming path.
4	RxOOF	8 O	Receive OOF Defect Indicator:
		0	This READ-ONLY bit-field indicates whether or not the Frame Synchronizer block is currently declaring an OOF (Out of Frame) condition.
			0 - Frame Synchronizer block is NOT currently declaring the OOF condition.
			1 – Frame Synchronizer block is currently declaring the OOF condition.
3	Unused	R/O	
2	Framing with	R/W	Framing with Valid P-Bit Select:
	Valid P Bits		This READ/WRITE bit-field permits the user to choose between two different sets of DS3 Frame Acquisition/Maintenance criteria.
			0 - Normal Framing Acquisition/Maintenance Criteria (without P-bit Checking)
			In this mode, the Frame Synchronizer block will declare the "In-frame" state, one it has successfully completed both the "F-Bit Search" and the "M-Bit Search" states.

		1 - Framing Acquisition/Maintenance with P-bit Checking				
		In this mode, the Frame Synchronizer block will (in addition to passing through the "F-Bit Search" and "M-Bit Search" states) also verify valid P-bits, prior to declaring the "In-Frame" state.				
		Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.				
F-Sync Algo	R/W	F-Bit Search State Criteria Select:				
		This READ/WRITE bit-field permits the user to choose between two different sets of DS3 Out of Frame (OOF) Declaration criteria.				
		0 – OOF is declared when 6 out of 15 F-bits are erred.				
		1 – OOF is declared when 3 out of 15 F-bits are erred.				
		Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.				
M-Sync Algo	R/W	M-Bit Search State Criteria Select				
		This READ/WRITE bit-field permits the user to choose between two different sets of DS3 Out of Frame (OOF) Declaration criteria.				
		0 – M-bit Errors do not result in the Frame Synchronizer declaring OOF.				
		1 – OOF is declared when M-bits, within 3 out of 4 DS3 frames are in error.				
0 – M-bit Errors do not result in the Frame Synchronizer declaring OOF. 1 – OOF is declared when M-bits, within 3 out of 4 DS3 frames are in error.						
	M-Sync Algo	M-Sync Algo R/W				

EXAR

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 8: RxDS3 Status Register (Address Location= 0xN311)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused			RxFERF	RxAIC	RxFEBE[2:0]		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 5	Unused	R/O	
4	RxFERF	R/O	Receive FERF (Far-End Receive Failure) Defect Indicator:
			This READ-ONLY bit-field indicates whether or not the Frame Synchronizer block is currently declaring a FERF condition.
			0 - The Frame Synchronizer block is NOT currently declaring the FERF condition.
			1 – The Frame Synchronizer block is currently declaring the FERF condition.
			Note: This bit-field is not valid if the Frame Synchronizer block has been bypassed.
3	RxAIC	R/O	Receive AIC State:
			This READ-ONLY bit-field indicates the current state of the AIC bit-field within the incoming DS3 data-stream.
			0 – Indicates that the Frame Synchronizer block has received at least 2 consecutive M-frames that have the AIC bit-field set to "0".
			1 – Indicates that the Frame Synchronizer block has received at least 63 consecutive M-frames that have the AIC bit-field set to "1".
2 – 0	RxFEBE[2:0]	R/O	Receive FEBE (Far-End Block Error) Value:
			These READ-ONLY bit-fields reflect the FEBE value within the most recently received DS3 frame.
		30,	RxFEBE[2:0] = [1, 1, 1] indicates a normal condition. All other values for RxFEBE[2:0] indicates an erred condition at the remote terminal equipment.
		6,	Note:
	*	10 10	1. This bit-field is not valid if the Frame Synchronizer block has been by- passed.
		0	2. This bit-field is not valid if the Frame Synchronizer block has been configured to operate in the M13 Framing format.

Table 574: RxDS3 Interrupt Enable Register (Address Location= 0xN312)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Detection of CP Bit Error Interrupt Enable	Change of LOS Condition Interrupt Enable	Change of AIS Condition Interrupt Enable	Change of Idle Condition Interrupt Enable	Change of FERF Condition Interrupt Enable	Change of AIC State Interrupt Enable	Change of OOF Condition Interrupt Enable	Detection of P-Bit Error Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Detection of	R/W	Detection of CP-Bit Error Interrupt Enable
	CP Bit Error Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of CP-Bit Error" Interrupt, within the Channel. If the user enables this interrupt, then the Frame Synchronizer block will generate an interrupt anytime it detects CP bit errors.
			0 - Disables the "Detection of CP Bit Error" Interrupt.
			1 - Enables the "Detection of CP-Bit Error" Interrupt.
			Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.
6	Change of	R/W	Change in LOS Condition Interrupt Enable:
	LOS Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in LOS (Loss of Signal) Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Frame Synchronizer block will generate an interrupt in response to either of the following conditions.
			The instant that the channel declares an LOS condition.
			The instant that the channel clears the LOS condition.
		*	0 – Disables the "Change in LOS Condition" Interrupt.
		AUC	1 Enables the "Change in LOS Condition" Interrupt.
5	Change of AIS	R/W	Change in AIS Condition Interrupt Enable:
	Condition Interrupt Enable	ata d	This READ/WRITE bit-field permits the user to either enable or disable the Change in AIS (Alarm Indication Signal) Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Frame Synchronizer block will generate an interrupt in response to either of the following conditions.
		2	The instant that the channel declares an AIS condition.
			The instant that the channel clears the AIS condition.
			0 - Disables the "Change in AIS Condition" Interrupt.
			1 - Enables the "Change in AIS Condition" Interrupt.
			Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.
4	Change of Idle	R/W	Change in Idle Condition Interrupt Enable:
	Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in Idle Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Frame Synchronizer block will generate an interrupt in response to either of the following conditions.
			The instant that the channel detects the Idle condition.
			The instant that the channel ceases to detect the Idle condition.
	i		

EXAR Experience Our Connectivi

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			0 – Disables the "Change in Idle Condition" Interrupt.			
			1 - Enables the "Change in Idle Condition" Interrupt.			
			Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.			
3	Change of	of R/W Change in FERF Condition Interrupt Enable:				
	FERF Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in FERF (Far-End Receive Failure) Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Frame Synchronizer block will generate an interrupt in response to either of the following conditions.			
			The instant that the channel declares an FERF condition.			
			The instant that the channel clears the FERF condition.			
			0 - Disables the "Change in FERF Condition" Interrupt.			
			1 – Enables the "Change in FERF Condition" Interrupt.			
			Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.			
2	Change of AIC	R/W	Change in AIC State Interrupt Enable:			
	State Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in AIC State" Interrupt, within the Channel. If the user enables this interrupt, then the Frame Synchronizer block will generate an interrupt in response to it detecting a change in the AIC bit-field, within the incoming DS3 data stream. Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.			
1	Change of	R/W	Change in OOF Condition Interrupt Enable:			
	OOF Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in OOF (Out of Frame) Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Frame Synchronizer block will generate an interrupt in response to either of the following conditions.			
			The instant that the channel declares an OOF condition.			
			The instant that the channel clears the OOF condition.			
		<u> </u>	0 - Disables the "Change in OOF Condition" Interrupt.			
		400	1 - Enables the "Change in OOF Condition" Interrupt.			
		6,	Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.			
0	Detection of P	R/W	Detection of P-Bit Error Interrupt Enable:			
	Bit Error \\ Interrupt Enable	98	This READ/WRITE bit-field permits the user to either enable or disable the "Detection of CP-Bit Error" Interrupt, within the Channel. If the user enables this interrupt, then the Frame Synchronizer block will generate an interrupt anytime it detects CP bit errors.			
			0 – Disables the "Detection of CP Bit Error" Interrupt.			
			1 – Enables the "Detection of CP-Bit Error" Interrupt.			
			Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.			

Table 575: RxDS3 Interrupt Status Register (Address Location= 0xN313)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Detection of CP Bit Error Interrupt Status	Change of LOS Condition Interrupt Status	Change of AIS Condition Interrupt Status	Change of Idle Condition Interrupt Status	Change of FERF Condition Interrupt Status	Change of AIC State Interrupt Status	Change of OOF Condition Interrupt Status	Detection of P-Bit Error Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7	Detection of CP	RUR	Detection of CP-Bit Error Interrupt Status:
	Bit Error Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of CP-Bit Error" Interrupt has occurred since the last read of this register.
			0 – The "Detection of CR-Bit Error" Interrupt has not occurred since the last read of this register.
			1 – The "Detection of CP-Bit Error" Interrupt has occurred since the last read of this register.
			Note: This bit-field is ignored if the Frame Synchronizer block is bypassed.
6	Change of LOS	RUR	Change in LOS Condition Interrupt Status:
	Condition Interrupt Status		This RESET upon-READ register indicates whether or not the "Change in LOS Condition" Interrupt has occurred since the last read of this register.
			0 The "Change in LOS Condition" Interrupt has not occurred since the last read of this register.
		loi	1 The "Change in LOS Condition" Interrupt has occurred since the last read of this register.
		glicita	Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.
5	Change of AIS	RUR	Change in AIS Condition Interrupt Status
	Condition Interrupt Status	SIMAY	This RESET-upon-READ register indicates whether or not the "Change in LOS Condition" Interrupt has occurred since the last read of this register.
	1.98	nd.	0 – The "Change in LOS Condition" Interrupt has not occurred since the last read of this register.
			1 – The "Change in LOS Condition" Interrupt has occurred since the last read of this register.
			Note: This bit-field is ignored if the Frame Synchronizer block is bypassed.
4	Change of Idle	RUR	Change in Idle Condition Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ register indicates whether or not the "Change in Idle Condition" interrupt has occurred since the last read of this register.
			0 – The "Change in Idle Condition" Interrupt has not occurred since the last read of this register.
			1 – The "Change in Idle Condition" Interrupt has occurred since the last read of this register.
			Note: This bit-field is ignored if the Frame Synchronizer block is by-

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			passed.
3	Change of FERF	RUR	Change in FERF Condition Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ register indicates whether or not the "Change in FERF Condition" Interrupt has occurred since the last read of this register.
			$0-\mbox{\sc The}$ "Change in FERF Condition" Interrupt has not occurred since the last read of this register.
			$1-\mbox{The}$ "Change in FERF Condition" Interrupt has occurred since the last read of this register.
			Note: This bit-field is ignored if the Frame Synchronizer block is bypassed.
2	Change of AIC	RUR	Change in AIC State Interrupt Status:
	State Interrupt Status		This RESET-upon-READ register bit indicates whether or not the "Change in AIC State" interrupt has occurred since the last read of this register.
			0 – The "Change in AIC State" Interrupt has not occurred since the last read of this register.
			1 – The "Change in AIC State" Interrupt has occurred since the last read of this register.
			Note: This bit-field is ignored if the Frame Synchronizer block is bypassed.
1	Change of OOF	RUR	Change in OOF condition Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ register indicates whether or not the "Change in OOF Condition" Interrupt has occurred since the last read of this register.
			0 – The "Change in OOF Condition" Interrupt has not occurred since the last read of this register.
			1 - The "Change in OOF Condition" Interrupt has occurred since the last read of this register.
		المجار	Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.
0	Detection of P-Bit	RUR	Detection of P-Bit Error Interrupt Status:
	Error Interrupt Status	ologie	This RESET-upon-READ bit-field indicates whether or not the "Detection of CP-Bit Error" Interrupt has occurred since the last read of this register.
	The	20 11	O – The "Detection of CP-Bit Error" Interrupt has not occurred since the last read of this register.
		and	1 – The "Detection of CP-Bit Error" Interrupt has occurred since the last read of this register.
			Note: This bit-field is ignored if the Frame Synchronizer block is bypassed.

Table 576: RxDS3 Sync Detect Register (Address Location= 0xN314)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused					F Algorithm	One and Only
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
2	P-Bit Correct	R/W	P-Bit Correct:
			This READ/WRITE bit-field permits the user to enable or disable the "P-Bit Correct" feature within the DS3 Frame Synchronizer block. If the user enables this feature, then the DS3 Frame Synchronizer will automatically invert the state of any P-bits, whenever it detects "P-bit errors".
			0 – Disables the "P-Bit Correct" feature
			1 – Enables the "P-Bit Correct" feature
1	F Algorithm	R/W	F-Bit Search Algorithm Select.
			This READ/WRITE bit-field permits the user to select the "F-bit acquisition" criteria, when the Frame Synchronizer block is operating in the "F-Bit Search" state.
			0 - Frame Synchronizer will move on to the "M-Bit Search" state, when it has properly located 10 consecutive F-bits.
			1 – Frame Synchronizer will move on to the "M-Bit Search" state, when it has properly located 16 consecutive F-bits.
0	One and Only	R/W	F-Bit Search/Mimic-Handling Algorithm Select:
		. (6	This READ/WRITE bit-field permits the user to select the "F-bit acquisition" criteria, when the Frame Synchronizer block is operating in the "F-Bit Search" state.
		oduct.	0 – Frame Synchronizer will move on to the "M-Bit Search" state, when it has properly located 10 (or 16) consecutive F-bits (as configured in Bit 1 of this register).
	, he	ra ma	1 – Frame Synchronizer will move on to the "M-Bit Search" state, when (1) it has properly located 10 (or 16) consecutive F-bits; and (2) when it has located and identified only one viable "F-Bit Alignment" candidate.
	7.8	and.	Note: If this bit is set to "1", then the Frame Synchronizer block will NOT transition into the "M-Bit Search" state, as long as at least two viable candidate set of bits appear to function as the F-bits.

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 577: RxDS3 FEAC Register (Address Location= 0xN316)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused			RxFEACCode[5:0]				Unused
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	1	1	1	1	1	1	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Unused	R/O	
6 - 1	RxFEAC_Code[5:0]	R/O	Receive FEAC Code Word:
			These READ-ONLY bit-fields contain the value of the most recently "validated" FEAC Code word.
0	Unused	R/O	All Jie
	thed	ata and a	Lor products mentioned in the products mentioned in the products mentioned in the products of

Table 578: RxDS3 FEAC Interrupt Enable/Status Register (Address Location= 0xN317)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		FEAC Valid	RxFEAC Remove Interrupt Enable	RxFEAC Remove Interrupt Status	RxFEAC Valid Interrupt Enable	RxFEAC Valid Interrupt Status
R/O	R/O	R/O	R/O	R/W	RUR	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 5	Unused	R/O	Please set to "0" (the default value) for normal operation.
4	FEAC Valid	R/O	FEAC Message Validation Indicator
			This READ-ONLY bit-field indicates that the FEAC Code (which resides within the "RxDS3 FEAC" Register) has been validated by the Receive FEAC Controller. The Receive FEAC Controller will validate a FEAC codeword if it has received this codeword in 8 out of the last 10 FEAC Messages. Polled systems can monitor this bit-field, when checking for a newly validated FEAC codeword.
			0 – FEAC Message is not (or no longer) validated.
			1 – FEAC Message has been validated.
3	RxFEAC	R/W	FEAC Message Remove Interrupt Enable:
	Remove Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Receive FEAC Remove Interrupt". If the user enables this interrupt, then the Framer Synchronizer will generate an interrupt anytime the most recently validated FEAC Message has been removed. The Receive FEAC Controller will remove a validated FEAC codeword, if it has received a different codeword in 3 out of the last 10 FEAC Messages.
			0 Receive FEAC Remove Interrupt is disabled.
			1 – Receive FEAC Remove Interrupt is enabled.
		400	Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.
2	RxFEAC	RUR	FEAC Message Remove Interrupt Status:
	Remove Interrupt Status	300	This RESET-upon-READ bit-field indicates whether or not the "FEAC Message Remove Interrupt" has occurred since the last read of this register.
		o silic	$\rm 0-FEAC$ Message Remove Interrupt has NOT occurred since the last read of this register.
			1 - FEAC Message Remove Interrupt has occurred since the last read of this register.
1	RxFEAC	R/W	FEAC Message Validation Interrupt Enable:
	Valid Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the FEAC Message Validation Interrupt. If the user enables this interrupt, then the Frame Synchronizer block will generate an interrupt anytime a new FEAC Codeword has been validated by the Receive FEAC Controller.
			0 – FEAC Message Validation Interrupt is NOT enabled.
			1 – FEAC Message Validation Interrupt is enabled.
0	RxFEAC	RUR	FEAC Message Validation Interrupt Status:
	Valid Interrupt		This RESET-upon-READ bit-field indicates whether or not the "FEAC Message

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Status	Validation" Interrupt has occurred since the last read of this register.
	0 – FEAC Message Validation Interrupt has not occurred since the last read of this register.
	1 – FEAC Message Validation Interrupt has occurred since the last read of this register.

The product are no longered (OBS)

The product are no longered (OBS)

The product are no longered (OBS)

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 579: RxDS3 LAPD Control Register (Address Location= 0xN318)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
RxLAPD Any		Unu	ısed		RxLAPD Enable	RxLAPD Interrupt Enable	RxLAPD Interrupt Status
R/W	R/O	R/O	R/O	R/O	R/W	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	RxLAPD Any	R/W	Receive LAPD – Any kind:
			This READ/WRITE bit-field permits the user to configure the LAPD Receiver to receive any kind of LAPD Message (or HDLC Message) with a size of 82 bytes or less. If the user implements this option, then the LAPD Receiver will be capable of receiving any kind of HDLC Message (with any value of header bytes). The only restriction is that the size of the HDLC Message must not exceed 82 bytes. 0 – Does not invoke this "Any Kind of HDLC Message" feature. In this case, the LAPD Receiver will only receive HDLC Messages that contains the Bellcore GR-499-CORE values for SAPI and TEI.
			Invokes this "Any Kind of HDLC Message" feature. In this case, the LAPD Receiver will be able to receive HDLC Messages that contain any header byte values. Note:
			This bit-field is ignored if the Frame Synchronizer block is by-passed.
			The user can determine the size (or byte-count) of the most recently received LAPD/PMDL Message, by reading the contents of the "RxLAPD Byte Count" Register (Address Location= 0xN284)
6 – 3	Unused	R/O	10,00
2	RxLAPD	R/W	LAPD Receiver Enable:
	Enable	*S	This READ/WRITE bit-field permits the user to either enable or disable the LAPD Receiver within the channel. If the user enables the LAPD Receiver, then it will immediately begin extracting out and monitoring the data (being carried via the "DL" bits) within the incoming DS3 data stream.
	7.8	9, 9	0 – Enables the LAPD Receiver.
		0	1 – Disables the LAPD Receiver.
			Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.
1	RxLAPD	R/W	Receive LAPD Message Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Receive LAPD Message" Interrupt. If the user enables this interrupt, then the channel will generate an interrupt, anytime the LAPD Receiver receives a new PMDL Message.
			0 - Disables the "Receive LAPD Message" Interrupt.
			1 – Enables the "Receive LAPD Message" Interrupt.
			Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.
0	RxLAPD	RUR	Receive LAPD Message Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Receive LAPD

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Status	Message" Interrupt has occurred since the last read of this register.
	$\rm 0-$ "Receive LAPD Message" Interrupt has NOT occurred since the last read of this register.
	1 – "Receive LAPD Message" Interrupt has occurred since the last read of this register.
	Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.

The product are no longered (OBS)

The product are no longered (OBS)

The product are no longered (OBS)

Table 580: RxDS3 LAPD Status Register (Address Location= 0xN319)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	RxABORT	RxLAPDType[1:0]		RxCR Type	RxFCS Error	End of Message	Flag Present
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре			DESCRIPTION
7	Unused	R/O			
6	RxABORT	R/O	Receive A	BORT Seq	uence Indicator:
					oit-field indicates that the LAPD Receiver has bequence (e.g., a string of seven consecutive "0s").
			0 – LAPD	Receiver ha	as NOT received an ABORT sequence.
			1 - LAPD	Receiver ha	as received an ABORT sequence.
			;		PD Receiver receives an ABORT sequence, it will it-field "high", until it receives another LAPD
5 – 4	RxLAPDType[1:0]	R/O	Receive L	APD Mess	age Type Indicator:
			residing w between t	ithin the R the content	bits indicate the type of LAPD Message that is eceive LAPD Message buffer. The relationship of these two bit-fields and the corresponding ented below.
			RXLAPD	Type[1:0]	Message Type
			0	0	CL Path Identification
	N		90	1	Idle Signal Identification
	300	S C	1	0	Test Signal Identification
	66,8	107	1	1	ITU-T Path Identification
3	RxCR Type	R/O	Received	C/R Value:	
	o alli				field indicates the value of the C/R bit (within one of the most recently received LAPD Message.
2	RxFCS Error	R/O	Receive F	rame Chec	k Sequence (FCS) Error Indicator:
					t-field indicates whether or not the most recently age frame contained an FCS error.
			0 – The m an FCS er	-	received LAPD Message frame does not contain
			1 – The m FCS error.		y received LAPD Message frame does contain an
1	End of Message	R/O	End of Me	essage Indi	cator
			_		-field indicates whether or not the LAPD Receiver ete LAPD Message.
			0 – LAPD	Receiver is	currently receiving a LAPD Message, but has not

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			received the complete message.
			1 – LAPD Receiver has received a completed LAPD Message.
			Note: Once the LAPD Receiver sets this bit-field "high", this bit-field will remain high, until the LAPD Receiver begins to receive a new LAPD Message.
0	Flag Present	R/O	Receive Flag Sequence Indicator:
			This READ-ONLY bit-field indicates whether or not the LAPD Receiver is currently receiving the Flag Sequence (e.g., a continuous stream of 0x7E octets within the Data Link channel).
			0 – LAPD Receiver is NOT currently receiving the Flag Sequence octet.

receive sceiving the a sceiving the

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 581: RxDS3 Pattern Register (Address Location= 0xN32F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
DS3 AIS Unframed All Ones	DS3 AIS Non Stuck Stuff	Unused	Receive LOS Pattern		Receive DS3 l	dle Pattern[3:0]	
R/W	R/W	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	1	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	DS3 AIS	R/W	DS3 AIS - Unframed All Ones – AIS Pattern
	Unframed All Ones		This READ/WRITE bit-field, (along with the "Non-Stuck-Stuff" bit) permits the user specify the "AIS Declaration" criteria for the DS3 Frame Synchronizer block, as described below:
			0 - Configures the DS3 Frame Synchronizer block to declare an AIS condition, when receiving a DS3 signal carrying a "framed 1010" pattern.
			1 — Configures the DS3 Frame Synchronizer block to declare an AIS condition, when receiving either an unframed, All Ones pattern or a "framed 1010" pattern.
6	DS3 AIS	R/W	DS3 AIS - Non-Stuck-Stuff Option – AIS Pattern
	Non-Stuck Stuff		This READ/WRITE bit-field (along with the "Unframed All Ones – AIS Pattern bit-field) permits the user to define the "AIS Declaration" criteria for the DS3 Frame Synchronizer block, as described below.
			0 – Configures the DS3 Frame Synchronizer block to require that all "C" bits are set to "0" before it will declare an AIS condition.
			1 Configures the DS3 Frame Synchronizer block to NOT require that all "C" bits are set to "0" before it will declare an AIS condition. In this mode, no attention will be paid to the state of the "C" bits within the incoming DS3 data-stream.
5	Unused	R/O	
4	Receive LOS Pattern	R/W	Receive LOS Pattern:
	Pattern	Silis	this READ/WRITE bit-field permits the user to define the "LOS Declaration" criteria for the DS3 Frame Synchronizer block, as described below.
	7,99	My Tro	0- Configures the DS3 Frame Synchronizer to declare an LOS condition if it receives a string of a specific length of consecutive zeros.
		6	1 – Configures the DS3 Frame Synchronizer to declare an LOS condition if it receives a string (of a specific length) of consecutive ones.
3 – 0	Receive DS3	R/W	Receive DS3 Idle Pattern:
	Idle Pattern[3:0]		These READ/WRITE bit-fields permit the user to specify the pattern in which the DS3 Frame Synchronizer will recognize as the "DS3 Idle Pattern".
			Note: The Bellcore GR-499-CORE specified value for the Idle Pattern is a framed repeating "1, 1, 0, 0" pattern. Therefore, if the user wishes to configure the "DS3 Frame Synchronizer" to declare an "Idle Pattern" when it receives this pattern, then he/she write the value [1100] into these bit-fields.

1.12.4 RECEIVE E3, ITU-T G.751 RELATED REGISTERS

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 582: RxE3 Configuration and Status Register # 1 - G.751 (Address Location= 0xN310)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		RxFERF		Unused		RxBIP-4
			Algo				Enable
R/O	R/O	R/O	R/W	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 5	Unused	R/O	
4	RxFERF Algo	R/W	Receive FERF Algorithm Select:
			This READ/WRITE bit-field permits the user to select the "Receive FERF Declaration" and "Clearance" criteria.
			0 - Receive FERF is declared if the "A" bit-field (within the incoming E3 data-stream) is set to "1" for 3 consecutive frames. Receive FERF is cleared if the "A" bit-field is set to "0" for 3 consecutive frames.
			1 - Receive FERF is declared if the "A" bit-field is set to "1" for 5 consecutive frames. Receive FERF is cleared if the "A" bit-field is set to "0" for 5 consecutive frames.
3 – 1	Unused	R/O	me ing
0	RxBIP4 Enable	R/W	Enable BIP-4 Verification: This READ/WRITE bit-field permits the user to configure the Frame Synchronizer block to verify the BIP-4 value, within the incoming E3 data-stream. 0 – BIP-4 Verification is NOT performed.
			1 – BIP-4 Verification is performed.
	~	he data	0 – BIP-4 Verification is performed. 1 – BIP-4 Verification is performed.

Table 583: RxE3 Configuration and Status Register # 2 - G.751 (Address Location= 0xN311)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
RxLOF Algo	RxLOF	RxOOF	RxLOS	RxAIS	Unu	ısed	RxFERF
R/W	R/O						
0	1	1	0	0	0	0	1

BIT NUMBER	NAME	Түре	DESCRIPTION
7	RxLOF Algo	R/W	Receive Loss of Frame Declaration/Clearance Criteria Select:
			This READ/WRITE bit-field permits the user to select the Loss of Frame (LOF) Declaration and Clearance Criteria.
			0 – LOF will be declared if the Frame Synchronizer block resides within the OOF (Out-of-Frame) state for 24 E3 frame periods. LOF will also be cleared once the Frame Synchronizer resides within the "In-Frame" state for 24 E3 frame period.
			1 – LOF will be declared if the Frame Synchronizer block resides within the OOF state for 8 E3 frame periods. LOF will also be cleared once the Frame Synchronizer block resides within the "In-Frame" state for 8 E3 frame periods.
6	RxLOF	R/O	Receive Loss of Frame Defect Indicator
			This READ-ONLY bit-field indicates whether or not the Frame Synchronizer block is currently declaring the LOF condition.
			0 – Frame Synchronizer is NOT declaring an LOF condition with the incoming data stream.
			1 - Frame Synchronizer is currently declaring an LOF condition with the incoming data stream.
		×	Note: This bit-field is not valid if the Frame Synchronizer block is bypassed.
5	RxOOF	R/O	Receive Out of Frame Defect Indicator
		dogue	This READ-ONLY bit-field indicates whether or not the Frame Synchronizer block is currently declaring the OOF condition.
	The	40	Frame Synchronizer is NOT declaring an OOF condition with the incoming data stream.
		you do	1 – Frame Synchronizer is currently declaring an OOF condition with the incoming data stream.
			Note: This bit-field is not valid if the Frame Synchronizer block is bypassed.
4	RxLOS	R/O	Receive Loss of Signal Defect Indicator
			This READ-ONLY bit-field indicates whether or not the Frame Synchronizer block is currently declaring the LOS condition.
			0 - Frame Synchronizer/Channel is NOT declaring an LOS condition in the incoming data stream.
			1 – Frame Synchronizer/Channel is currently declaring an LOS condition in the incoming data stream.
3	RxAIS	R/O	Receive AIS Defect Indicator:
			This READ-ONLY bit-field indicates whether or not the Frame Synchronizer block is currently receiving an AIS signal within the incoming E3 data-stream

EXARExperience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

		1	Ţ ,
			or not.
			0 – Frame Synchronizer block is NOT detecting an AIS pattern in the incoming data stream.
			1 - Frame Synchronizer block is currently detecting an AIS pattern in the incoming data stream.
			Note: This bit-field is not valid if the Frame Synchronizer block is bypassed.
2 – 1	Unused	R/O	
0	RxFERF	R/O	Receive FERF (Far-End-Receive Failure) Defect Indicator:
			This READ-ONLY bit-field indicates whether or not the Frame Synchronizer block is currently declaring a FERF condition or not.
			0 – Frame Synchronizer block is NOT declaring the FERF condition.
			1 – Frame Synchronizer block is declaring the FERF condition.
			Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.
		the production	1 - Frame Synchronizer block is declaring the FPRF condition. Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.

Table 584: RxE3 Interrupt Enable Register # 1 – G.751 (Address Location= 0xN312)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		COFA Interrupt Enable	Change in OOF State Interrupt Enable	Change in LOF State Interrupt Enable	Change in LOS State Interrupt Enable	Change in AIS State Interrupt Enable
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 5	Unused	R/O	
4	COFA Interrupt Enable	R/W	Change of Framing Alignment Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change of Framing Alignment" Interrupt, within the Channel. If the user enables this interrupt, then the Frame Synchronizer block will generate an interrupt anytime it detects a Change in Frame Alignment (e.g., the FAS bits have appeared to move to a different location in the E3 data stream).
3	Change in	R/W	Change in OOF Condition Interrupt Enable
	OOF State Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in OOF (Out of Frame) Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Frame Synchronizer block will generate an interrupt in response to either of the following conditions.
			The instant that the channel declares an OOF condition.
			The instant that the channel clears the OOF condition.
			0 – Disables the "Change in OOF Condition" Interrupt.
			1 Enables the Change in OOF Condition" Interrupt.
		X	Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.
2	Change in LOF State Interrupt Enable	RAND progression	Change in LOF Condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change in LOF (Loss of Frame) Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Frame Synchronizer block will generate an interrupt in response to either of the following conditions. The instant that the channel declares an LOF condition. The instant that the channel clears the LOF condition.
			0 – Disables the "Change in LOF Condition" Interrupt.
			1 – Enables the "Change in LOF Condition" Interrupt.Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.
1	Change in	D/M/	
1	Change in LOS State	R/W	Change in LOS Condition Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in LOS (Loss of Signal) Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Frame Synchronizer block will generate an interrupt in response to either of the following conditions.
			The instant that the channel declares an LOS condition.
			The instant that the channel clears the LOS condition.
			0 – Disables the "Change in LOS Condition" Interrupt.

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			1 – Enables the "Change in LOS Condition" Interrupt.
0	Change in AIS State Interrupt Enable	R/W	Change in AIS Condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change in AIS (Alarm Indication Signal) Condition" Interrupt, within the Channel. If the user enables this interrupt, then the Frame Synchronizer block will generate an interrupt in response to either of the following conditions. • The instant that the channel declares an AIS condition. • The instant that the channel clears the AIS condition. 1 — Disables the "Change in AIS Condition" Interrupt. 1 — Enables the "Change in AIS Condition" Interrupt. Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.

The drattice and having the arthur and having the arthur and the a

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 585: RxE3 Interrupt Enable Register # 2 - G.751 (Address Location= 0xN313)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused				Detection of BIP-4 Error Interrupt Enable	Detection of FAS Bit Error Interrupt Enable	Reserved
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 4	Unused	R/O	Please set to "0" (the default value) for normal operation
3	Change in FERF State Interrupt Enable	R/W	Change in FERF Condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change in FERF Condition" Interrupt of the user enables this interrupt, then the Frame Synchronizer block will generate an interrupt anytime the state of the FERF condition changes: 0 – Disables the "Change in FERF Condition" Interrupt. 1 – Enables the "Change in FERF Condition" Interrupt. Note: This bit-field is ignored anytime the Frame Synchronizer block is bypassed.
2	Detection of BIP-4 Error Interrupt Enable	R/W	Detection of BIP-4 Error Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Detection of BIP-4 Error" Interrupt. If the user enables this interrupt, then the Frame Synchronizer block will generate an interrupt anytime it detects a BIP-4 error within the incoming E3 data stream. O- Disables the "Detection of BIP-4 Error" Interrupt. 1 - Enables the "Detection of BIP-4 Error" Interrupt. Note: This bit-field is ignored anytime the Frame Synchronizer block is bypassed.
1	Detection of FAS Bit Error Interrupt Enable	OR/WI	This READ/WRITE bit-field permits the user to either enable or disable the "FAS Bit Error" Interrupt. If the user enables this interrupt, then the Frame Synchronizer block will generate an interrupt anytime it detects an FAS error within the incoming E3 data stream. 0 – Disables the "Detection of FAS Bit Error" Interrupt. 1 – Enables the "Detection of FAS Bit Error" Interrupt. Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.
0	Unused	R/O	Please set to "0" (the default value) for normal operation.



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 586: RxE3 Interrupt Status Register # 1 – G.751 (Address Location= 0xN314)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused			COFA Interrupt Status	Change in OOF State Interrupt Status	Change in LOF State Interrupt Status	Change in LOS State Interrupt Status	Change in AIS State Interrupt Status
R/O	R/O	R/O	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 5	Unused	R/O	
4	COFA	RUR	Change of Framing Alignment (COFA) Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of Framing Alignment (COFA) interrupt has occurred since the last read of this register.
			0 - The "COFA" Interrupt has NOT occurred since the last read of this register.
			1 – The "COFA" Interrupt has occurred since the last read of this register.
3	Change in	RUR	Change of OOF (Out of Frame) Condition Interrupt Status:
	OOF State Interrupt Status		This RESET-upon-READ bit field indicates whether or not the "Change of OOF Condition" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the DS3/E3 Framer block will generate an interrupt in response to either of the following condition.
			Whenever the Frame Synchronizer block declares the OOF Condition.
			Whenever the Frame Synchronizer block clears the OOF Condition.
		8	0 - The "Change in OOF Condition" Interrupt has NOT occurred since the last read of this register.
			1 – The "Change in OOF Condition" Interrupt has occurred since the last read of this register.
		he is	Note: The user can obtain the current OOF state of the DS3/E3 Framer block by reading out the state of Bit 5 (RxOOF) within the "RxE3 Configuration and Status # 2 – G.751" (Address Location= 0xN311).
2	Change in	RUR	Change of LOF (Loss of Frame) Condition Interrupt Status:
	LOF State Interrupt Status	0	This RESET-upon-READ bit-field indicates whether or not the "Change of LOF Condition" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the DS3/E3 Framer block will generate an interrupt in response to either of the following condition.
			Whenever the Frame Synchronizer block declares the LOF Condition.
			Whenever the Frame Synchronizer block clears the LOF Condition.
			$\rm 0-The$ "Change in LOF Condition" Interrupt has NOT occurred since the last read of this register.
			1 – The "Change in LOF Condition" Interrupt has occurred since the last read of this register.
			Note: The user can obtain the current LOF state of the DS3/E3 Framer block by reading out the state of Bit 6 (RxLOF) within the "RxE3 Configuration and Status # 2 – G.751" (Address Location= 0xN311).

1	Change in	RUR	Change of LOS (Loss of Signal) Condition Interrupt Status:
	LOS State Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of LOS Condition" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the DS3/E3 Framer block will generate an interrupt in response to either of the following condition.
			Whenever the Frame Synchronizer block declares the LOS Condition.
			Whenever the Frame Synchronizer block clears the LOS Condition.
			0 – The "Change of LOS Condition" Interrupt has NOT occurred since the last read of this register.
			1 – The "Change of LOS Condition" Interrupt has occurred since the last read of this register.
			Note: The user can obtain the current LOS state of the DS3/E3 Framer block by reading out the state of Bit 4 (RxLOS) within the "RxE3 Configuration and Status #2 – G.751" (Address Location= 0xN311).
0	Change in	RUR	Change of AIS Condition Interrupt Status:
	AIS State Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of AIS Condition" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the DS3/E3 Framer block will generate an interrupt in response to either of the following condition.
			Whenever the Frame Synchronizer block declares the AIS Condition.
			Whenever the Frame Synchronizer block clears the AIS Condition.
			0 - The "Change of AIS Condition" Interrupt has NOT occurred since the last read of this register.
			1 – The "Change of AIS Condition" Interrupt has occurred since the last read of this register.
		Ä	Note: The user can obtain the current AIS state of the DS3/E3 Framer block by reading out the state of Bit 3 (RxAIS) within the "RxE3 Configuration and Status # 2 – G.751" (Address Location= 0xN311).
	The	production of the state of the	Note: The user can obtain the current AIS state of the DS3/E3 Framer block by reading out the state of Bit 3 (RxAIS) within the "RxE3 Configuration and Status # 2 – G.751" (Address Location= 0xN311).
		o affic	

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 587: RxE3 Interrupt Status Register # 2 - G.751 (Address Location= 0xN315)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused				Change of FERF Condition Interrupt Status	Detection of BIP-4 Error Interrupt Status	Detection of FAS Bit Error Interrupt Status	Reserved
R/O	R/O	R/O	R/O	RUR	RUR	RUR	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION			
7 – 4	Unused	R/O	is ad			
3	Change of FERF	RUR	Change of FERF Condition Interrupt			
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in FERF Condition" interrupt has occurred since the last read of this register.			
			0 – The "Change in FERF Condition" interrupt has NOT occurred since the last read of this register.			
			1 – The "Change in FERF Condition" interrupt has occurred since the last read of this register.			
2	Detection of	RUR	Detection of BIP-4 Error Interrupt:			
	BIP-4 Error Interrupt Status		This "RESET-upon-READ" bit-field indicates whether or not the "Detection of BIP-4 Error" interrupt has occurred since the last read of this register.			
			0 – The "Detection of BIP-4 Error" Interrupt has NOT occurred since the last read of this register.			
			1 - The "Detection of BIP-4 Error" Interrupt has occurred since the last read of this register.			
1	Detection of	RUR	Detection of FAS Bit Error Interrupt:			
	FAS Bit Error Interrupt Status	,odl	This "RESET-upon-READ" bit-field indicates whether or not the "Detection of FAS Bit Error" interrupt has occurred since the last read of this register.			
		6, 6	0 – The "Detection of FAS Bit Error" Interrupt has NOT occurred since the last read of this register.			
	Ku	dation	The "Detection of FAS Bit Error" Interrupt has occurred since the last read of this register.			
0	Unused	R/O				

Table 588: RxE3 LAPD Control Register – G.751 (Address Location= 0xN318)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
RxLAPD Any	Message Check Disable		Unused			RxLAPD Interrupt Enable	RxLAPD Interrupt Status
R/W	R/W	R/O	R/O	R/O	R/W	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	RxLAPD Any	R/W	Receive LAPD – Any kind:
			This READ/WRITE bit-field permits the user to configure the LAPD Receiver to receive any kind of LAPD Message (or HDLC Message) with a size of 82 bytes or less. If the user implements this option, then the LAPD Receiver will be capable of receiving any kind of HDLC Message (with any value of header bytes). The only restriction is that the size of the HDLC Message must not exceed 82 bytes.
			0 – Does not invoke this "Any Kind of HDLC Message" feature. In this case, the LAPD Receiver will only receive HDLC Messages that contains the Bellcore GR-499-CORE values for SAPI and TEI.
			1 - Invokes this "Any Kind of HDLC Message" feature. In this case, the LAPD Receiver will be able to receive HDLC Messages that contain any header byte values. Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.
			The user can determine the size (or byte count) of the most recently received LAPD/PMDL Message, by reading the contents of the "RxLAPD Byte Count" Register (Address Location= 0xN384).
6	Message	R/W	Message Check Disable:
	Check Disable	AUC	This READ/WRITE bit-field permits the user to either enable or disable the new message comparison logic. If the user disables the new message comparison logic, then every message received would generate an interrupt.
		40,00	0 – Enables the new message comparison logic
	0	6, 21,	Disables the new message comparison logic
5 – 3	Unused	R/O	
2	RxLAPD	R/W	LAPD Receiver Enable:
	Enable	%	This READ/WRITE bit-field permits the user to either enable or disable the LAPD Receiver within the channel. If the user enables the LAPD Receiver, then it will immediately begin extracting out and monitoring the data (being carried via the "DL" bits) within the incoming DS3 data stream.
			0 – Enables the LAPD Receiver.
			1 – Disables the LAPD Receiver.
			Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.
1	RxLAPD	R/W	Receive LAPD Message Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Receive LAPD Message" Interrupt. If the user enables this interrupt, then the channel will generate an interrupt, anytime the LAPD Receiver receives a new PMDL Message.

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			0 – Disables the "Receive LAPD Message" Interrupt. 1 – Enables the "Receive LAPD Message" Interrupt. Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.		
0	RxLAPD	RUR	Receive LAPD Message Interrupt Status:		
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Receive LAPD Message" Interrupt has occurred since the last read of this register.		
			0 – "Receive LAPD Message" Interrupt has NOT occurred since the last read of this register.		
			1 – "Receive LAPD Message" Interrupt has occurred since the last read of this register.		
			Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.		

rame Synchi

-rame Synchi

-rame Synchi

Inthis trad

Int

Table 589: RxE3 LAPD Status Register – G.751 (Address Location= 0xN319)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	RxABORT	RxLAPDType[1:0]		RxCR Type	RxFCS Error	End of Message	Flag Present
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре			DESCRIPTION		
7	Unused	R/O					
6	RxABORT	R/O	Receive ABORT Sequence Indicator:				
					oit-field indicates that the LAPD Receiver has bequence (e.g., a string of seven consecutive "0s").		
			0 – LAPD	Receiver ha	as NOT received an ABORT sequence.		
			1 – LAPD	Receiver ha	as received an ABORT sequence.		
			;		PD Receiver receives an ABORT sequence, it will it-field "high", until it receives another LAPD		
5 – 4	RxLAPDType[1:0]	R/O	Receive L	APD Mess	age Type Indicator:		
			residing w between t	ithin the R the content	bits indicate the type of LAPD Message that is eceive LAPD Message buffer. The relationship tof these two bit-fields and the corresponding ented below.		
			RXLAPD	Type[1:0]	Message Type		
			0	0	CL Path Identification		
	N	0	90	1	Idle Signal Identification		
	300	S C	1 0 Test Signal Identification				
	e Pig	107	1	1	ITU-T Path Identification		
3	RxCR Type	R/O	Received	C/R Value:			
	o alli				field indicates the value of the C/R bit (within one of the most recently received LAPD Message.		
2	RxFCS Error	R/O	Receive F	rame Chec	k Sequence (FCS) Error Indicator:		
					t-field indicates whether or not the most recently age frame contained an FCS error.		
			0 – The most recently received LAPD Message frame does not contain an FCS error.				
			1 – The most recently received LAPD Message frame does contain an FCS error.				
1	End of Message	R/O	End of Message Indicator				
			_		-field indicates whether or not the LAPD Receiver ete LAPD Message.		
			0 – LAPD	Receiver is	currently receiving a LAPD Message, but has not		

EXARExperience *Qur* Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			received the complete message. 1 – LAPD Receiver has received a completed LAPD Message. Note: Once the LAPD Receiver sets this bit-field "high", this bit-field will remain high, until the LAPD Receiver begins to receive a new LAPD Message.		
0	Flag Present	R/O	Receive Flag Sequence Indicator:		
			This READ-ONLY bit-field indicates whether or not the LAPD Receiver is currently receiving the Flag Sequence (e.g., a continuous stream of 0x7E octets within the Data Link channel).		
			0 – LAPD Receiver is NOT currently receiving the Flag Sequence octet.		
			1 – LAPD Receiver is currently receiving the Flag Sequence octet.		

Table 590: RxE3 Service Bits Register - G.751 (Address Location= 0xN31A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Unu	00	P RxA	RxN		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0,0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 2	Unused	R/O	100 N
1	RxA	R/O	Received A Bit Value: This READ-ONLY bit-field reflects the value of the "A" bit, within the most recently received E3 frame.
0	RxN	R/O	Received N Bit Value: This READ-ONLY bit-field reflects the value of the "N" bit, within the most recently received E3 frames.
		The	ata sha y no

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

1.12.5 RECEIVE E3, ITU-T G.832 RELATED REGISTERS

Table 591: RxE3 Configuration and Status Register # 1 – G.832 (Address Location= 0xN310)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
RxPLDType[2:0]			RxFERF Algo.	RxTMark Algo	RxPLDTypeExp[2:0]		
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	1	0	0	0	0	1	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 5	RxPLDType[2:0]	R/O	Received PLD (Payload) Type[2:0]:
			These three READ-ONLY bit-fields reflect the value of the Payload Type bits, within the MA byte of the most recently received E3 frame.
4	RxFERF Algo	R/W	Receive FERF Declaration/Clearance Algorithm:
			This READ/WRITE bit-field permits the user to select a "Receive FERF Declaration and Clearance" Algorithm, as indicated below.
			0 – The Frame Synchronizer block will declare a FERF condition if it receives the FERF indicator in 3 consecutive E3 frames. Additionally, the Frame Synchronizer block will also clear the FERF condition if it no longer receives the FERF indicator for 3 consecutive E3 frames.
			1 – The Frame Synchronizer block will declare a FERF condition if it receives the PERF indicator in 5 consecutive E3 frames. Additionally, the Frame Synchronizer block will also clear the FERF condition if it no longer receives the FERF indicator for 5 consecutive E3 frames.
3	RxTMark Algo	R/W	Receive Timing Marker Validation Algorithm:
		, cit	This READ/WRITE bit-field permits the user to select the "Receive Timing Marker Validation" algorithm, as indicated below.
	30,	oe'	The Timing Marker will be validated if it is of the same state for three consecutive E3 frames.
	we ha	showy	1 – The Timing Marker will be validated if it is of the same state for five (5) consecutive E3 frames.
2 - 0	RxPLDTypExp[2:0]	R/W	Receive PLD (Payload) Type – Expected:
			This READ/WRITE bit-field permits the user to specify the "expected value" for the Payload Type, within the MA bytes of each incoming E3 frame. If the Frame Synchronizer block receives a Payload Type that differs then what has been written into these register bits, then it will generate the "Payload Type Mismatch" Interrupt.

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 592: RxE3 Configuration and Status Register # 2 – G.832 (Address Location= 0xN311)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
RxLOF	RxLOF	RxOOF	RxLOS	RxAIS	RxPLD	RxTMark	RxFERF
Algo					Unstab		
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	1	1	0	0	1	1	1

BIT NUMBER	NAME	Түре	DESCRIPTION
7	RxLOF Algo	R/W	Receive LOF (Loss of Frame) Declaration Algorithm:
			This READ/WRITE bit-field permits the user to select a "Receive LOF Declaration" Algorithm, as indicated below.
			0 – The Frame Synchronizer will declare a Loss of Frame condition after it has resided within the "OOF" (Out of Frame) condition for 24 E3 frame periods.
			1 – The Frame Synchronizer will declare a Loss of Frame condition after it has resided within the "OOF" condition for 8 £3 frame periods.
6	RxLOF	R/O	Receive Loss of Frame Indicator:
			This READ-ONLY bit-field indicates whether or not the Frame Synchronizer is currently declaring a Loss of Frame condition, as indicated below.
			0 – The Frame Synchronizer block is NOT currently declaring a Loss of Frame condition.
			1 – The Frame Synchronizer block is currently declaring a Loss of Frame condition.
5	RxOOF	R/O	Receive Out of Frame Indicator:
			This READ-ONLY bit-field indicates whether or not the Frame Synchronizer is currently declaring an Out of Frame (OOF) condition, as indicated below.
			0 The Frame Synchronizer block is NOT currently declaring an Out of Frame condition.
		,0	1 – The Frame Synchronizer block is currently declaring an Out of Frame condition
	A	he sts	Note: The Frame Synchronizer block will declare an "OOF" condition if it detects FA1 or FA2 byte errors in four (4) consecutive "incoming" E3 frames.
4	RxLOS	R/O	Receive Loss of Signal Indicator:
			This READ-ONLY bit-field indicates whether or not the Frame Synchronizer block is currently declaring an LOS (Loss of Signal) condition, as indicated below.
			0 - The Frame Synchronizer block is NOT currently declaring an LOS condition.
			1 – The Frame Synchronizer block is currently declaring an LOS condition.
3	RxAIS	R/O	Receive AIS Indicator:
			This READ-ONLY bit-field indicates whether or not the Frame Synchronizer block is currently detecting an AIS pattern, in the incoming E3 data stream; as indicated below.
			0 – The Frame Synchronizer block is NOT currently detecting an AIS pattern in the incoming E3 data stream.
			1 - The Frame Synchronizer block is currently detecting an AIS pattern in the

		incoming E3 data stream.						
		Note: The Frame Synchronizer block will declare an "AIS" condition if it detects 7 or less "0s" within two consecutive "incoming" E3 frames.						
RxPLD	R/O	Receive Payload-Type Unstable Indicator:						
Unstab		This READ-ONLY bit-field indicates whether or not the Payload Type (within the MA bytes of each incoming E3 frame) has been consistent in the last 5 frames, as indicated below.						
		0 – The Payload Type value has been consistent for at least 5 consecutive Estrames.						
		1 - The Payload Type value has NOT been consistence for the last 5 E3 frames.						
RxTMark	R/O	Received (Validated) Timing Marker:						
		This READ-ONLY bit-field indicates the value of the most recently validated "Timing Marker".						
RxFERF	R/O	Receive FERF (Far-End-Receive Failure) Indicator:						
		This READ-ONLY bit-field indicates whether or not the Frame Synchronizer is currently declaring a FERF condition, as indicated below.						
		0 - The Frame Synchronizer block is NOT currently declaring a FERF condition.						
		1 – The Frame Synchronizer block is currently declaring a FERF condition.						
	RxTMark RxFERF	RxTMark R/O RxFERF R/O						

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 593: RxE3 Interrupt Enable Register # 1 – G.832 (Address Location= 0xN312)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Change in SSM MSG Interrupt Enable	Change in SSM OOS Interrupt Enable	COFA Interrupt Enable	Change in OOF State Interrupt Enable	Change in LOF State Interrupt Enable	Change in LOS State Interrupt Enable	Change in AIS State Interrupt Enable
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7	Unused	R/O	
6	Change in SSM MSG Interrupt Enable	R/W	Change of Synchronization Status Message (SSM) Condition Interrupt Enable:
			This READ/WRITE bit-field permits the user to either enable or disable the "Change in SSM Message" Interrupt, as indicated below.
			0 – Disables the "Change in SSM Message" Interrupt.
			1 — Enables the "Change of SSM Message" Interrupt. In this configuration, the Frame Synchronizer block will generate an interrupt anytime it receives a new (or different) SSM Message in the incoming E3 data-stream.
5	Change in SSM OOS State Interrupt Enable	R/W	Change of SSM OOS (Out of Sequence) Condition Interrupt Enable:
			This READ/WRITE bit-field permits the user to either enable or disable the "Change of SSM OOS Condition" Interrupt, as indicated below.
		6,	0 – Disables the "Change of SSM OOS Condition" Interrupt.
	COFA Interrupt Enable	et al	1 Enables the "Change of SSM OOS Condition" Interrupt. In this configuration, the Frame Synchronizer block will generate an interrupt under the following conditions.
		27	When the Frame Synchronizer block declares an SSM OOS condition.
	Thedata	4,	When the Frame Synchronizer block clears the SSM OOS condition.
4	COFA Interrupt Enable	R/W	Change of Framing Alignment Interrupt Enable:
			This READ/WRITE bit-field permits the user to either enable or disable the "Change of Framing Alignment" condition interrupt, as indicated below.
			0 – Disables the "Change of Framing Alignment" Interrupt.
			1 – Enables the "Change of Framing Alignment" Interrupt.
3	Change in OOF State	R/W	Change of OOF (Out of Frame) Condition Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of OOF Condition" Interrupt, as indicated below.
			0 – Disables the "Change of OOF Condition" Interrupt.
			1 – Enables the "Change of OOF Condition" Interrupt. In this configuration, the Frame Synchronizer block will generate an

			interrupt under the following conditions.
			When the Frame Synchronizer block declares an OOF condition.
			When the Frame Synchronizer block clears the OOF condition.
2	Change in LOF State	R/W	Change of LOF (Loss of Frame) Condition Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of LOF Condition" Interrupt, as indicated below.
			0 – Disables the "Change of LOF Condition" Interrupt.
			1 – Enables the "Change of LOF Condition" Interrupt. In this configuration, the Frame Synchronizer block will generate an interrupt under the following conditions.
			When the Frame Synchronizer block declares an LOF condition.
			When the Frame Synchronizer block clears the LOF condition.
1	Change in LOS State	R/W	Change of LOS (Loss of Signal) Condition Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the Change of LOS Condition" Interrupt, as indicated below.
			0 - Disables the "Change of LOS Condition" Interrupt.
			1 — Enables the "Change of LOS Condition" Interrupt. In this configuration, the Frame Synchronizer block will generate an interrupt under the following conditions.
		50,	When the Frame Synchronizer block declares an LOS condition.
		16,0	When the Frame Synchronizer block clears the LOS condition.
0	AIS Interrupt Enable	R/W	Change of AIS (Alarm Indication Signal) Condition Interrupt Fnable:
	AIS Interrupt Enable	al of	This READ/WRITE bit-field permits the user to either enable or disable the "Change of AIS Condition" Interrupt, as indicated below.
	6,8,3	3	0 – Disables the "Change of AIS Condition" Interrupt.
	The data and ma		1 – Enables the "Change of AIS Condition" Interrupt. In this configuration, the Frame Synchronizer block will generate an interrupt under the following conditions.
			When the Frame Synchronizer block declares an AIS condition.
			When the Frame Synchronizer block clears the AIS condition.

EXARExperience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 594: RxE3 Interrupt Enable Register # 2 - G.832 (Address Location= 0xN313)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Change in RxTTB Message Interrupt Enable	Reserved	Detection of FEBE Event Interrupt Enable	Change in FERF State Interrupt Enable	Detection of BIP-8 Error Interrupt Enable	Detection of Framing Byte Error Interrupt Enable	RxPLD Mis Interrupt Enable
R/O	R/W	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Unused	R/O	nis ad
6	Change in RxTTB	R/W	Change in Receive Trail-Trace Buffer Message Interrupt Enable:
	Message Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in RxTTB Message" Interrupt, as indicated below.
			0 – Disables the "Change in RXTTB Message" Interrupt.
			1 – Enables the "Change in RXITB Message" Interrupt. In this mode, the Frame Synchronizer block will generate an interrupt anytime it receives a different TTB message, then what it had been receiving.
5	Unused	R/W	'el 'se' 85'
4	Detection of FEBE	R/W	Detection of FEBE Interrupt Enable:
	Event Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of FEBE" Interrupt, as indicated below.
			0 - Disables the "Detection of FEBE" Interrupt.
		. ict	1 – Enables the "Detection of FEBE" Interrupt. In this mode, the Frame Synchronizer block will generate an interrupt anytime it detects a FEBE (Far-End Block Error) indicator in the incoming E3 data-stream.
3	Change in FERF	R/W	Change of FERF Condition Interrupt Enable:
	State Interrupt Enable	She	This READ/WRITE bit-field permits the user to either enable or disable the Change of FERF Condition Interrupt, as indicated below.
	411.21	074	0 – Disables the "Change in FERF Condition" Interrupt.
	, 90	ano	1 – Enables the "Change in FERF Condition" Interrupt. In this mode, the Frame Synchronizer block will generate an interrupt, in response to either of the following conditions.
			When the Frame Synchronizer declares a FERF condition.
			When the Frame Synchronizer clears the FERF condition.
2	Detection of BIP-8	R/W	Detection of BIP-8 Error Interrupt Enable:
	Error Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of BIP-8 Error" Interrupt, as indicated below.
			0 - Disables the "Detection of BIP-8 Error" Interrupt.
			1 – Enables the "Detection of BIP-8 Error" Interrupt. In this mode, the Frame Synchronizer block will generate an interrupt anytime it detects a BIP-8 error in the incoming E3 data-stream.
1	Detection of Framing Byte Error Interrupt	R/W	Detection of Framing Byte Interrupt Enable:

	Enable	This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Framing Byte Error" Interrupt, as indicated below.
		0 – Disables the "Detection of Framing Byte Error" Interrupt.
		1 – Enables the "Detection of Framing Byte Error" Interrupt. In this mode, the Frame Synchronizer block will generate an interrupt anytime it detects a FA1 or FA2 byte error in the incoming E3 data stream.
0	RxPLD Mis Interrupt	Received Payload Type Mismatch Interrupt Enable:
	Enable	This READ/WRITE bit-field permits the user to either enable or disable the "Receive Payload Type Mismatch" interrupt, as indicated below.
		0 – Disables the "Received Payload Type Mismatch" Interrupt.
		1 – Enables the "Received Payload Type Mismatch" Interrupt. In this mode, the Frame Synchronizer block will generate an interrupt anytime it receives a "Payload Type" value (within the MA byte) that differs from that written into the "RxPLDExp[2:0]" bit-fields.

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 595: RxE3 Interrupt Status Register # 1 – G.832 (Address Location= 0xN314)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Change in SSM MSG Interrupt Status	Change in SSM OOS Interrupt Status	COFA Interrupt Status	Change in OOF State Interrupt Status	Change in LOF State Interrupt Status	Change in LOS State Interrupt Status	Change in AIS State Interrupt Status
R/O	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7	Unused	R/O	
6	Change in SSM MSG Interrupt Status	RUR	Change in SSM (Synchronization Status Message) Interrupt Status:
			This RESET-upon-READ bit-field indicates whether or not the "Change in SSM Message" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the DS3/E3 Framer block will generate an interrupt, anytime it detects a change in the "SSM[3:0]" value that it has received via the incoming E3 data-stream.
			0 - Indicates that the "Change in SSM Message" Interrupt has NOT occurred since the last read of this register.
			1 Indicates that the "Change in SSM Message" Interrupt has occurred since the last read of this register.
		or pro	Note: The user can obtain the newly received value for "SSM" by reading out the contents of Bits 3 through 1 (RxSSM[3:0]) within the "RxE3 SSM Register – G.832" (Address Location= 0xN32C).
5	Change in SSM OOS State Interrupt Status	RUR	Change in SSM OOS (Out of Sequence) State Interrupt Status:
	Change in SSM OOS State Interrupt Status	NO	This RESET-upon-READ bit-field indicates whether or not the "Change in SSM OOS State" Interrupt has occurred since the last read of this register.
	Theatendu		If this interrupt is enabled, then the DS3/E3 Framer block will generate the "Change in SSM OOS State" Interrupt will response to the following events.
			When the DS3/E3 Frame Synchronizer block declares the SSM OOS Condition.
			When the DS3/E3 Frame Synchronizer block clears the SSM OOS condition.
			0 – Indicates that the "Change in SSM OOS Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in SSM OOS Condition" Interrupt has occurred since the last read of this register.
4	COFA Interrupt Status	RUR	COFA Interrupt Status:
			This RESET-upon-READ bit-field indicates whether or not the "COFA" (Change of Framing Alignment) Interrupt has occurred since the last read of this register.

			If this interrupt is enabled, then the DS3/E3 Framer block will generate an interrupt anytime it detects a new "Framing Alignment" with the incoming E3 data-stream.
			0 – Indicates that the "COFA Interrupt" has not occurred since the last of this register.
			1 - Indicates that the "COFA Interrupt" has occurred since the last read of this register.
3	Change in OOF State Interrupt	RUR	Change in OOF (Out of Frame) State Interrupt Status:
	Status		This RESET-upon-READ bit-field indicates whether or not the "Change in OOF State" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the DS3/E3 Framer block will generate the "Change in OOF State" Interrupt in response to the following events.
			When the DS3/E3 Frame Synchronizer block declares the "OOF Condition".
			When the D\$3/E3 Frame Synchronizer block clears the "OOF Condition".
			0 – Indicates that the "Change in OOF State Interrupt" has not occurred since the last of this register.
			1 – Indicates that the "Change in OOF State Interrupt" has occurred since the last read of this register.
		du	Note: The user can determine the current state of the "AIS Condition" by reading out the contents of Bit 5 (RxOOF) within the "RxE3 Configuration and Status Register # 2 – G.832" (Address Location= 0xN311).
2	Change in LOF State Interrupt	RUR	Change in LOF (Loss of Frame) State Interrupt Status:
	Change in LOF State Interrupt Status	0	This RESET-upon-READ bit-field indicates whether or not the Change in LOF State" Interrupt has occurred since the last read of this register.
	aroduo ta	oto	If this interrupt is enabled, then the DS3/E3 Framer block will generate the "Change in LOF State" Interrupt will occur in response to the following events.
	the to may		When the DS3/E3 Frame Synchronizer block declares the "LOF Condition".
	J. gand		When the DS3/E3 Frame Synchronizer block clears the "LOF Condition".
			occurred since the last of this register.
			1 – Indicates that the "Change in LOF State Interrupt" has occurred since the last read of this register.
			Note: The user can determine the current state of the "AIS Condition" by reading out the contents of Bit 6 (RxLOF) within the "RxE3 Configuration and Status Register # 2 – G.832" (Address Location= 0xN311).
1	Change in LOS State Interrupt	RUR	Change in LOS (Loss of Signal) State Interrupt Status:
	Status		This RESET-upon-READ bit-field indicates whether or not the "Change in LOS State" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the DS3/E3 Framer block will

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			generate the "Change in LOS State" Interrupt will occur in response to the following events.
			When the DS3/E3 Frame Synchronizer block declares the "LOS Condition".
			When the DS3/E3 Frame Synchronizer block clears the "LOS Condition".
			0 – Indicates that the "Change in LOS State Interrupt" has not occurred since the last of this register.
			1 – Indicates that the "Change in LOS State Interrupt" has occurred since the last read of this register.
			Note: The user can determine the current state of the "AIS Condition" by reading out the contents of Bit 4 (RxLOS) within the "RxE3 Configuration and Status Register # 2 – G.832" (Address Location= 0xN311).
0	Change in AIS State Interrupt	RUR	Change in AIS State Interrupt Status:
	Status		This RESET-upon-READ bit-field indicates whether or not the "Change in AIS State" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the DS3/E3 Framer block will generate the "Change in AIS State" Interrupt will occur in response to the following events.
			When the DS3/E3 Frame Synchronizer block declares the "AIS Condition".
			When the DS3/E3 Frame Synchronizer block clears the "AIS Condition".
		No	0 – Indicates that the "Change in AIS State Interrupt" has not occurred since the last of this register.
		ol so	 Indicates that the "Change in AIS State Interrupt" has occurred since the last read of this register.
	do hee	3100	The user can determine the current state of the "AIS Condition" by reading out the contents of Bit 3 (RxAIS) within the "RxE3 Configuration and Status Register # 2 – G.832" (Address Location= 0xN311).

Table 596: RxE3 Interrupt Status Register # 2 - G.832 (Address Location= 0xN315)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Change in RxTTB Message Interrupt Status	Reserved	Detection of FEBE Event Interrupt Status	Change in FERF State Interrupt Status	Detection of BIP-8 Error Interrupt Status	Detection of Framing Byte Error Interrupt Status	RxPLD Mis Interrupt Status
R/O	RUR	R/O	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7	Unused	R/O	is a
6	Change in RxTTB Message Interrupt Status	RUR	Change in Receive Trail-Trace Buffer Message Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change in RxTTB Message" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the DS3/E3 Framer block will generate an interrupt anytime it receives a Trail-Trace Buffer Message, that is different from that of the previously received message. 0 – Indicates that the "Change in Receive TTB Message" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Change in Receive TTB Message" Interrupt has occurred since the last read of this register. Note: The user can obtain the value of the most recently received TTB Message by reading out the contents of the "RxE3 TTB-0" through "RxE3 TTB-15" registers (Address Location=0xN31C through 0xN32B).
5	Unused	R/O	
4	Detection of FEBE Event Interrupt Status	RUR	Detection of FEBE Event Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Detection of FEBE Event" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the DS3/E3 Framer block will generate an interrupt anytime is detects a FEBE event in the incoming E3 data-stream. 0 – Indicates that the "Detection of FEBE Event" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of FEBE Event" Interrupt has occurred since the last read of this register.
3	Change in FERF State Interrupt Status	RUR	Change in FERF (Far-End Receive Failure) State Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change in FERF State" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the DS3/E3 Framer block will generate an interrupt in response to the following events. • When the Frame Synchronizer block declares the FERF condition. • When the Frame Synchronizer block clears the FERF condition. 0 – Indicates that the "Change in FERF State" Interrupt has NOT

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			occurred since the last read of this register.
			1 – Indicates that the "Change in FERF State" Interrupt has occurred since the last read of the register.
			Note: The user can obtain the state of the FERF condition, by reading out the contents of Bit 0 (RxFERF) within the "RxE3 Configuration and Status Register # 2 – G.832" (Address Location= 0xN311).
2	Detection of BIP-8 Error Interrupt Status	RUR	Detection of BIP-8 Error Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Detection of BIP-8 Error" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the DS3/E3 Framer block will generate an interrupt anytime is detects a BIP-8 Error in the incoming E3 data-stream. 0 – Indicates that the "Detection of BIP-8 Error" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Detection of BIP-8 Error" Interrupt has occurred since the last read of this register.
1	Detection of Framing Byte Error Interrupt Status	RUR	Detection of Framing Byte Error Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Detection of Framing Byte Error" Interrupt has occurred since the last read of this register. If this interrupt is enabled then the DS3/E3 Framer block will generate an interrupt anytime is detects an error in either the FA1 or FA2 byte, within the incoming E3 data-stream. 0 – Indicates that the "Detection of Framing Byte Error" Interrupt has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of Framing Byte Error" Interrupt has occurred since the last read of this register.
0	Detection of PLD Type Mismatch Interrupt Status	RUR	Detection of Payload Type Mismatch Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the Detection of Payload Type Mismatch" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the DS3/E3 Framer block will generate an interrupt anytime it receives an E3 data-stream that contains a "RxPLDType[2:0]" that is different from the "RxPLDTypeExp[2:0]" value. 0 – Indicates that the "Detection of Payload Type Mismatch" Interrupt
		all	has NOT occurred since the last read of this register. 1 – Indicates that the "Detection of Payload Type Mismatch" Interrupt has occurred since the last read of this register.
			Note: The user can obtain the contents of the most recently received Payload Type by reading out the contents of Bits 7 through 5 (RxPLDType[2:0]) within the "RxE3 Configuration and Status Register # 1 – G.832" (Address Location= 0xN310).

Table 597: RxE3 LAPD Control Register – G.832 (Address Location= 0xN318)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
RxLAPD Any	Message Check Disable	Unused		DL from NR Byte	RxLAPD Enable	RxLAPD Interrupt Enable	RxLAPD Interrupt Status
R/W	R/W	R/O	R/O	R/W	R/W	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	RxLAPD Any	R/W	Receive LAPD – Any kind:
			This READ/WRITE bit-field permits the user to configure the LAPD Receiver to receive any kind of LAPD Message (or HDLC Message) with a size of 82 bytes or less. If the user implements this option, then the LAPD Receiver will be capable of receiving any kind of HDLC Message (with any value of header bytes). The only restriction is that the size of the HDLC Message must not exceed 82 bytes. 0 – Does not invoke this "Any Kind of HDLC Message" feature. In this case, the LAPD Receiver will only receive HDLC Messages that contains the Bellcore GR-499-CORE values for SAPI and TEI.
			1-Invokes this "Any Kind of HDLC Message" feature. In this case, the LAPD Receiver will be able to teceive HDLC Messages that contain any header byte values.
			Note: This bit-field is ignored if the Frame Synchronizer block is by-passed. The user can determine the size (or byte count) fo the most recently received LAPD/PMDL Message, by reading the contents of the "RxLAPD Byte Count" Register (Address Location= 0xN384).
0	Message Check Disable	R/W	Message Check Disable: This READ/WRITE bit-field permits the user to either enable or disable the new message comparison logic. If the user disables the new message comparison logic, then every message received would generate an interrupt. 0 – Enables the new message comparison logic
	· · · · · · · · · · · · · · · · · · ·	6, 2,	Disables the new message comparison logic
6 – 4	Unused	R/O	
3	DL from NR	R/W	PMDL in NR Byte Select:
	Byte	'0	This READ/WRITE bit-field permits the user to configure the LAPD Receiver to extract out the PMDL data from the NR or GC byte, within the incoming E3 data stream.
			$\rm 0-The\;LAPD\;Receiver\;will\;extract\;PMDL$ information from the GC byte, within the incoming E3 data stream.
			$1-\mbox{The LAPD}$ Receiver will extract PMDL information from the NR byte, within the incoming E3 data stream.
			Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.
2	RxLAPD	R/W	LAPD Receiver Enable:
	Enable		This READ/WRITE bit-field permits the user to either enable or disable the LAPD Receiver within the channel. If the user enables the LAPD Receiver, then it will immediately begin extracting out and monitoring the data (being carried via the "DL" bits) within the incoming DS3 data stream.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

	ı	1			
			0 – Enables the LAPD Receiver.		
			1 – Disables the LAPD Receiver.		
			Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.		
1	RxLAPD	R/W	Receive LAPD Message Interrupt Enable:		
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Receive LAPD Message" Interrupt. If the user enables this interrupt, then the channel will generate an interrupt, anytime the LAPD Receiver receives a new PMDL Message.		
			0 - Disables the "Receive LAPD Message" Interrupt.		
			1 – Enables the "Receive LAPD Message" Interrupt.		
			Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.		
0	RxLAPD	RUR	Receive LAPD Message Interrupt Status		
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Receive LAPD Message" Interrupt has occurred since the last read of this register.		
			0 – "Receive LAPD Message" Interrupt has NOT occurred since the last read of this register.		
			1 – "Receive LAPD Message" Interrupt has occurred since the last read of this register.		
			Note: This bit-field is ignored if the Frame Synchronizer block is by-passed.		

Table 598: RxE3 LAPD Status Register – G.832 (Address Location= 0xN319)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	RxABORT	RxLAPD [*]	Type[1:0]	RxCR	RxFCS	End of	Flag
				Type	Error	Message	Present
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре			DESCRIPTION	
7	Unused	R/O				
6	RxABORT	R/O	Receive A	BORT Seq	uence Indicator:	
					oit-field indicates that the LAPD Receiver has sequence (e.g., a string of seven consecutive "0s").	
			0 – LAPD	Receiver ha	as NOT received an ABORT sequence.	
			1 - LAPD	Receiver h	as received an ABORT sequence.	
					PD Receiver receives an ABORT sequence, it will it-field "high", until it receives another LAPD	
5 – 4	RxLAPDType[1:0]	R/O	Receive L	APD Mess	age Type Indicator:	
			residing w between t	ithin the R	bits indicate the type of LAPD Message that is eceive LAPD Message buffer. The relationship tof these two bit-fields and the corresponding ented below.	
			RXLAPD	Type[1:0]	Message Type	
		160	0 0	0	CL Path Identification	
	N	0, 0,	90	1	Idle Signal Identification	
	NO.	0 (1	0	Test Signal Identification	
	ac Pig	(3)	1	1	ITU-T Path Identification	
3	RxCR Type	R/O	Received	C/R Value:		
	o and				-field indicates the value of the C/R bit (within one of the most recently received LAPD Message.	
2	RxFCS Error	R/O	Receive F	rame Chec	ck Sequence (FCS) Error Indicator:	
					t-field indicates whether or not the most recently age frame contained an FCS error.	
			0 – The m an FCS er		y received LAPD Message frame does not contain	
			1 – The m FCS error.		y received LAPD Message frame does contain an	
1	End of Message	R/O	End of Message Indicator			
			_		-field indicates whether or not the LAPD Receiver ete LAPD Message.	
			0 – LAPD	Receiver is	currently receiving a LAPD Message, but has not	

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			received the complete message. 1 – LAPD Receiver has received a completed LAPD Message. Note: Once the LAPD Receiver sets this bit-field "high", this bit-field will remain high, until the LAPD Receiver begins to receive a new LAPD Message.
0	Flag Present	R/O	Receive Flag Sequence Indicator:
			This READ-ONLY bit-field indicates whether or not the LAPD Receiver is currently receiving the Flag Sequence (e.g., a continuous stream of 0x7E octets within the Data Link channel).
			0 – LAPD Receiver is NOT currently receiving the Flag Sequence octet.
			1 – LAPD Receiver is currently receiving the Flag Sequence octet.

receive sceiving the a sceiving the

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 599: RxE3 NR Byte Register - G.832 (Address Location= 0xN31A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	RxNR_Byte[7:0]						
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	RxNR_Byte[7:0]	R/O	Receive NR Byte Value:
			These READ-ONLY bit-fields contain the value of the NR byte, within the most recently received E3 frame.

Table 600: RxE3 GC Byte Register - G.832 (Address Location= 0xN31B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	RxGC_Byte[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	RxGC_Byte[7:0]	R/O	Receive GC Byte Value: These READ-ONLY bit-fields contain the value of the GC byte, within the most recently received E3 frame.

Table 601: RxE3 TTB-0 Register - G.832 (Address Location= 0xN31C)

Віт 7	Віт 6	B) 7 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		10,00	RxTTB	5_0[7:0]			
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	3 0000	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_0[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 0:
			These READ-ONLY bit-fields contain the contents of Byte 0 (e.g., the "Marker" Byte), within the most recently received Trail-Trace Buffer" Message.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 602: RxE3 TTB-1 Register - G.832 (Address Location= 0xN31D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	RxTTB_1[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	RxTTB_1[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 1:
			These READ-ONLY bit-fields contain the contents of Byte 1, within the most recently received Trail-Trace Buffer" Message.

Table 603:	RxE3 TTB-2 R	egister – G.8	32 (Address I	Location= 0xl	N31E) HIS	ò	
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			RxTTB	3_2[7:0]	S JIII		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	RxTTB_2[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 2: These READ-ONLY bit-fields contain the contents of Byte 2, within the most recently received Trail-Trace Buffer" Message.

Table 604: RxE3 TTB-3 Register - G.832 (Address Location= 0xN31F)

Віт 7	Віт 6	Віт 5	Віт.4	Віт 3	Віт 2	Віт 1	Віт 0	
	© (RxTTB_3[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	0	0 0	0	0	0	0	0	

BIT NUMBER	NAME	Түрб	DESCRIPTION
7 - 0	RxTTB_3[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 3:
			These READ-ONLY bit-fields contain the contents of Byte 3, within the most recently received Trail-Trace Buffer" Message.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 605: RxE3 TTB-4 Register - G.832 (Address Location= 0xN320)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	RxTTB_4[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_4[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 4:
			These READ-ONLY bit-fields contain the contents of Byte 4, within the most recently received Trail-Trace Buffer" Message.

Table 606: RxE3 TTB-5 Register – G.832 (Address Location= 0xN321)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			RxTTB	_5[7:0]			
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	RxTTB_5[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 5: These READ-ONLY bit-fields contain the contents of Byte 5, within the most recently received Trail-Trace Buffer" Message.

Table 607: RxE3 TTB-6 Register - G.832 (Address Location= 0xN322)

Віт 7	Віт 6	Bit 5	Вгт 4	Віт 3	Віт 2	Віт 1	Віт 0
		0000	RxTTB	5_6[7:0]			
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0 0	0 0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_6[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 6:
			These READ-ONLY bit-fields contain the contents of Byte 6, within the most recently received Trail-Trace Buffer" Message.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 608: RxE3 TTB-7 Register - G.832 (Address Location= 0xN323)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	RxTTB_7[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	RxTTB_7[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 7:
			These READ-ONLY bit-fields contain the contents of Byte 7, within the most recently received Trail-Trace Buffer" Message.

Table 609:	RxE3 TTB-8	3 Register –	G.832 (Add	ress Locatio	on= 0xN324)	histored	
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			F	RxTTB_8[7:0]	0		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_8[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 8: These READ-ONLY bit-fields contain the contents of Byte 8, within the most recently received Trail-Trace Buffer" Message.

Table 610: RxE3 TTB-9 Register – G.832 (Address Location= 0xN325)

Віт 7	Віт 6	Віт 5	Віт.4	Віт 3	Віт 2	Віт 1	Віт 0	
	© (RxTTB_9[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	0	0 0	0	0	0	0	0	

BIT NUMBER	NAME	Түрб	DESCRIPTION
7 - 0	RxTTB_9[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 9:
			These READ-ONLY bit-fields contain the contents of Byte 9, within the most recently received Trail-Trace Buffer" Message.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 611: RxE3 TTB-10 Register – G.832 (Address Location= 0xN326)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
RxTTB_10[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_10[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 10:
			These READ-ONLY bit-fields contain the contents of Byte 10, within the most recently received Trail-Trace Buffer" Message.

Table 612: RxE3 TTB-11 Register - G.832 (Address Location= 0xN327)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			RxTTB_	_11[7:0]			
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	RxTTB_11[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 11: These READ-ONLY bit-fields contain the contents of Byte 11, within the most recently received Trail-Trace Buffer" Message.

Table 613: RxE3 TTB-12 Register - G.832 (Address Location= 0xN328)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		.00	O R	xTTB_12[7:0]			
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0 0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	RxTTB_12[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 12:
			These READ-ONLY bit-fields contain the contents of Byte 12, within the most recently received Trail-Trace Buffer" Message.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 614: RxE3 TTB-13 Register – G.832 (Address Location= 0xN329)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
RxTTB_13[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	RxTTB_13[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 13:
			These READ-ONLY bit-fields contain the contents of Byte 13, within the most recently received Trail-Trace Buffer" Message.

Table 615: RxE3 TTB-14 Register – G.832 (Address Location= 0xN32A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			RxTTB_	_14[7:0]			
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	RxTTB_14[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 14: These READ-ONLY bit-fields contain the contents of Byte 14, within the most recently received Trail-Trace Buffer" Message.

Table 616: RxE3 TTB-15 Register – G.832 (Address Location= 0xN32B)

Віт 7	Віт 6	Віт 5	Віт.4	Віт 3	Віт 2	Віт 1	Віт 0	
	© (RXTTB_15[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	0	Ø 0	0	0	0	0	0	

BIT NUMBER	NAME	Түрб	DESCRIPTION
7 - 0	RxTTB_15[7:0]	R/O	Receive Trail-Trace Buffer Message – Byte 15:
			These READ-ONLY bit-fields contain the contents of Byte 15, within the most recently received Trail-Trace Buffer" Message.

Table 617: RxE3 SSM Register – G.832 (Address Location= 0xN32C)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
RxSSM Enable	MF[1:0]		Reserved	RxSSM[3:0]			
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	RxSSM Enable	R/W	Receive SSM Enable:
			This READ/WRITE bit-field permits the user to configure the Frame Synchronizer block to operate in either the "Old ITU-T G.832 Framing" format or in the "New ITU-T G.832 Framing" format.
			0 – Configures the Frame Synchronizer block to support the "Pre October 1998" version of the E3, ITU-T G.832 Framing format.
			1 - Configures the Frame Synchronizer block to support the "October 1998" version of the E3/1TU-T G.832 framing format.
6 - 5	MF[1:0]	R/O	Multi-Frame Identification
			These READ-ONLY bit-fields reflect the current frame number, within the Received Multi-Frame
			Note: These bit-fields are only active if the DS3/E3 Frame Synchronizer block is active, and if Bit 7 (RxSSM Enable) of this register is set to "1".
4	Unused	R/O	od no ed
3 - 0	RxSSM[3:0]	R/O	Receive Synchronization Status Message[3:0]:
		, (0)	These READ-ONLY bit-fields reflect the content of the "SSM" bits, within the most recently received SSM Multiframe.
	50,	Joseph S	Note: These bit-fields are only active if the DS3/E3 Frame Synchronizer block is active, and if Bit 7 (RxSSM Enable) of this register is set to "1".
	The prod	id may	

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS



1.12.6 Transmit DS3 Related Registers

Table 618: TxDS3 Configuration Register (Address Location= 0xN330)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Tx Yellow Alarm	Tx X-Bits	Txldle	TxAIS	TxLOS	TxFERF upon LOS	TxFERF upon OOF	TxFERF upon AIS
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Tx Yellow	R/W	Transmit Yellow Alarm (FERF) indicator:
	Alarm		This READ/WRITE bit-field permits the user to force the Frame Generator block to transmit the FERF condition by setting both of the X-bits (within each outbound DS3 frame) to "0".
			0- "X" bits are set to the appropriate value, depending upon receive conditions (as detected by the Frame Synchronizer block).
			1 – "X" bits are forced to "0" and the FERF indicator is transmitted to the remote terminal equipment.
6	Tx X-Bits	R/W	Force X bits to "1":
			This READ/WRITE bit-field permits the user to force the Frame Generator block to set the X-bits (within each outbound DS3 frame) to "1".
			0- "X" bits are set to the appropriate value, depending upon receive conditions (as detected by the Frame Synchronizer block).
			1 – "X" bits are forced to "1".
5	Txldle	R/W	Transmit DS3 Idle Signal:
			This READ/WRITE bit-field permits the user to force the Frame Generator block to transmit an Idle signal condition to the remote terminal equipment.
		,(0 - Normal traffic is generated and transmitted by the Frame Generator block.
		6,	1-Frame Generator block transmits the DS3 Idle Pattern.
		No K	Note: This bit-field is ignored if "TxAIS" or "TxLOS" bit-fields are set to "1".
	•	1,99	The exact pattern that the Frame Generator transmits (whenever this bit-field is set to "1") depends upon the contents within Bits 3 through 0 (Tx_Idle_Pattern[3:0]) within the "Transmit DS3 Pattern" Register (Address Location= 0xN34C).
4	TxAIS	R/W	Transmit AIS Pattern:
			This READ/WRITE bit-field permits the user to force the Frame Generator block to transmit an AIS signal condition to the remote terminal equipment.
			0 - Normal traffic is generated and transmitted by the Frame Generator block.
			1 – Frame Generator block transmits the DS3 AIS Pattern.
			Note: This bit-field is ignored if the "TxLOS" bit-field is set to "1".
			When this bit-field is set to "1", it will transmit either a "Framed, repeating 1, 0, 1, 0," pattern, or an "Unframed, All-Ones" pattern, depending upon the state of Bit 7 (TxAIS Unframed All Ones), within the "Transmit DS3 Pattern Register (Address Location= 0xN34C).

	1		
3	TxLOS	R/W	Transmit LOS Pattern:
			This READ/WRITE bit-field permits the user to force the Frame Generator block to transmit an LOS signal condition to the remote terminal equipment.
			0 – Normal traffic is generated and transmitted by the Frame Generator block.
			1 – Frame Generator block transmits the LOS (e.g., All Zeros) Pattern.
			Note: This bit-field is ignored if "TxAIS" or "TxLOS" are set to "1".
			When this bit-field is set to "1", it will transmit either an "All Zeros" pattern, or an "All Ones" pattern; depending upon the state of Bit 4 (TxLOS Pattern) within the "Transmit DS3 Pattern Register (Address Location=0xN34C).
2	TxFERF	R/W	Transmit FERF upon Detection of LOS:
	upon LOS		This READ/WRITE bit-field permits the user to configure the Frame Generator block to automatically transmit the FERF indicator, anytime the Frame Synchronizer block declares an LOS condition.
			0 – Frame Generator block will NOT automatically transmit the FERF indicator, upon the Frame Synchronizer detecting an LOS condition.
			Frame Generator block will automatically transmit the FERF indicator upon the Frame Synchronizer detecting an LOS condition.
1	TxFERF	R/W	Transmit FERF upon Detection of OOF:
	upon OOF		This READ/WRITE bit-field permits the user to configure the Frame Generator block to automatically transmit the FERF indicator, anytime the Frame Synchronizer block declares an OOF condition.
			0 – Frame Generator block will NOT automatically transmit the FERF indicator, upon the Frame Synchronizer detecting an OOF condition.
			1 – Frame Generator block will automatically transmit the FERF indicator upon the Frame Synchronizer detecting an OOF condition.
0	TxFERF	R/W	Transmit FERF upon Detection of AIS:
	upon AIS		This READ/WRITE bit-field permits the user to configure the Frame Generator block to automatically transmit the FERF indicator, anytime the Frame Synchronizer block declares an AIS condition.
		NOON	Frame Generator block will NOT automatically transmit the FERF indicator, upon the Frame Synchronizer detecting an AIS condition.
	1/1/6	10	1. Frame Generator block will automatically transmit the FERF indicator upon the Frame Synchronizer detecting an AIS condition.
		Xa C	

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 619: TxDS3 FEAC Configuration and Status Register (Address Location= 0xN331)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		TxFEAC Interrupt Enable	TxFEAC Interrupt Status	TxFEAC Enable	TxFEAC Go	TxFEAC Busy
R/O	R/O	R/O	R/W	RUR	R/W	R/W	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 5	Unused	R/O	Please set to "0" for normal operation.
4	TxFEAC	R/W	Transmit FEAC Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Transmit FEAC" Interrupt. If the user enables this interrupt, then the Frame Generator will generate an interrupt, once it has completed its 10 th transmission of a given FEAC Message to the remote terminal equipment.
			0 – Transmit FEAC Interrupt is disabled.
			The Frame Generator block will NOT generate an interrupt after it has completed its 10 th transmission of a given FEAC Message.
			1 – Transmit FEAC Interrupt is enabled.
			The Frame Generator block will generate an interrupt after it has completed its 10 th transmission of a given FEAC Message.
3	TxFEAC	RUR	Transmit FEAC Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Transmit FEAC Interrupt" has occurred since the last read of this register.
			0 - The Transmit FEAC Interrupt has NOT occurred since the last read of this register.
			1 The Transmit FEAC Interrupt has occurred since the last read of this register.
2	TxFEAC	R/W	Transmit FEAC Controller Enable:
	Enable	100°	This READ/WRITE bit-field permits the user to either enable or disable the Transmit FEAC Controller, within the Frame Generator block.
	/	10	0 Disables the Transmit FEAC Controller.
		0	Enables the Transmit FEAC Controller.
1	TxFEAC Go	R/W	Transmit FEAC Message Command:
			A "0" to "1" transition, within this bit-field configures the Transmit FEAC Controller to begin its transmission of the FEAC Message (which consists of the FEAC code, as specified within the "TxDS3 FEAC" Register).
			Note: The user is advised to perform a write operation that resets this bit-field back to "0", following execution of the command to transmit a FEAC Message.
0	TxFEAC	R/O	Transmit FEAC Controller BUSY Indicator:
	Busy		This READ-ONLY bit-field indicates whether or not the Transmit FEAC Controller is currently busy transmitting a FEAC Message to the remote terminal.
			0 – Transmit FEAC Controller is NOT busy.
			1 - Transmit FEAC Controller is currently transmitting the FEAC Message to the



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

	remote terminal.

Table 620: TxDS3 FEAC Register (Address Location= 0xN332)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Unused		TxFEACCode[5:0]							
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/O		
0	1	1	1	1	1	1	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7	Unused	R/O	.6 À
6 - 1	TxFEACCode[5:0]	R/W	Transmit FEAC Code Word[5:0]
			These six (6) READ/WRITE bit-fields permit the user to specify the FEAC Code word that the Transmit PEAC Processor (within the Frame Generator block) should transmit to the remote terminal equipment.
			Once the user enables the "Transmit FEAC Controller" and commands it to begin its transmission, the Transmit FEAC Controller will then (1) encapsulate this six bit code word into a 16-bit structure, (2) proceed to transmit this 16-bit structure 10 times, repeatedly, and then halt.
			Note: These bit-fields are ignored if the user does not enable and use the Transmit FEAC Controller.
0	Unused	R/O	
	Thepro	duct (A productive of the contract o

EXARExperience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 621: TxDS3 LAPD Configuration Register (Address Location= 0xN333)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TxLAPD Any	Unused			Auto Retransmit	Reserved	TxLAPD Message Length	TxLAPD Enable
R/W	R/O	R/O	R/O	R/W	R/O	R/W	R/W
0	0	0	0	1	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	TxLAPD Any	R/W	Transmit LAPD – Any kind:
			This READ/WRITE bit-field permits the user to configure the LAPD Transmitter to transmit any kind of LAPD Message (or HDLC Message) with a size of 82 byte or less. If the user implements this option, then the LAPD Transmitter will be capable of transmitting any kind of HDLC frame (with any value of header bytes). The only restriction is that the size of the HDLC frame must not exceed 82 bytes. 0 – Does not invoke this "Any Kind of HDLC Message" feature. In this case,
			the LAPD Transmitter will only transmit HDLC Messages that contains the Bellcore GR-499-CORE values for SAPI and TEI.
			1- Invokes this "Any King of HDLC Message" feature. In this case, the LAPD Transmitter will be able to transmit HDLC Messages that contain any header byte values.
			Note: If the user invokes the "Any Kind of HDLC Message" feature, then he/she must indicate the size of the information payload (in terms of bytes) within the "Transmit LAPD Byte Count" Register (Address Location=0xN383).
6 - 4	Unused	R/O	101 100 110°
3	Auto Retransmit	R/W	Auto-Retransmit of LAPD Message:
	Retaismit	ne ro	This READ/WRITE bit-field permits the user to configure the LAPD Transmitter to transmit PMDL messages, repeatedly at one-second intervals. Once the user enables this feature, and then commands the LAPD Transmitter to transmit a given PMDL Message; the LAPD Transmitter will then proceed to transmit this PMDL Message (based upon the contents within the Transmit LAPD Message Buffer) repeatedly at one second intervals.
		1,90	0 – Disables the Auto-Retransmit Feature.
		0	In this case, the PMDL Message will only be transmitted once, afterwards the LAPD Transmitter will proceed to transmit a continuous stream of Flag Sequence octets (0x7E) via the DL bits, within each output DS3 frame. No more PMDL Messages will be transmitted until the user commands another transmission.
			1 – Enables the Auto-Retransmit Feature.
			In this case, the LAPD Transmitter will transmit PMDL messages (based upon the contents within the Transmit LAPD Buffer) repeatedly at one-second intervals.
			Note: This bit-field is ignored if the LAPD Transmitter is disabled.
2	Reserved	R/O	
1	TxLAPD	R/W	Transmit LAPD Message Length Select:
	Message Length		This READ/WRITE bit-field permits the user to specify the length of the payload

			date within the cuthours of ADD/DMDI Massacrass as indicated below	
			data within the outbound LAPD/PMDL Message, as indicated below.	
			0 – Configures the LAPD Transmitter to transmit a LAPD/PMDL message that has a payload data size of 76 bytes.	
			1 – Configures the LAPD Transmitter to transmit a LAPD/PMDL message that has a payload data size of 82 bytes.	
0	TxLAPD	R/W	LAPD Transmitter Enable:	
	Enable	This READ/WRITE bit-field permits the user to enable the LAPD Transmitter, within the channel. Once the user enables the LAPD Transmitter, it will immediately begin transmitting the Flag Sequence octet (0x7E) to the remote terminal via the outbound "DL" bits, within each DS3 data stream. The LAPD Transmitter will continue to do this until the user commands the LAPD Transmitter to transmit a PMDL Message.		
			0 – Disables the LAPD Transmitter.	
			1 – Enables the LAPD Transmitter.	
Transmitter will continue to do this until the user commands the LAPD Transmitter to transmit a PMDL Message. 0 – Disables the LAPD Transmitter. 1 – Enables the LAPD Transmitter. 1 – Enables the LAPD Transmitter. 1 – Enables the LAPD Transmitter.				

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 622: TxDS3 LAPD Status/Interrupt Register (Address Location= 0xN334)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unu	sed		TxDL	TxDL	TxLAPD	TxLAPD
				Start	Busy	Interrupt Enable	Interrupt Status
R/O	R/O	R/O	R/O	R/W	R/O	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 4	Unused	R/O	
3	TxDL Start	R/W	Transmit LAPD Message Command:
			A "0" to "1" transition, within this bit-field commands the LAPD Transmitter to begin the following activities:
			Reading out the contents of the Transmit LAPD Message Buffer.
			Zero-Stuffing of this data
			FCS Calculation and Insertion
			Fragmentation of this composite PMDL Message, and insertion into the "DL" bit-fields, within each outbound DS3 frame.
2	TxDL Busy	R/O	Transmit LAPD Controller Busy Indicator:
			This "READ-ONLY" bit-field indicates whether or not the Transmit LAPD Controller is currently busy transmitting a PMDL Message to the remote terminal equipment. The user can continuously poll this bit-field in order to check for completion of transmission of the LAPD/PMDL Message.
			0 – LAPD Transmitter is NOT busy transmitting a PMDL Message.
			1 – LAPD Transmitter is currently busy transmitting a PMDL Message.
1	TxLAPD Interrupt Enable	R/W	Transmit LAPD Interrupt Enable: This READ WRITE bit-field permits the user to either enable or disable the "Transmit LAPD Interrupt". If the user enables this interrupt, then the channel will generate an interrupt anytime the LAPD Transmitter has completed its transmission of a given LAPD/PMDL Message to the remote terminal.
	/	11/2	0 Disables Transmit LAPD Interrupt.
		0,	Enables Transmit LAPD Interrupt.
0	TxLAPD	RUR	Transmit LAPD Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Transmit LAPD Interrupt" has occurred since the last read of this register.
			0 - Transmit LAPD Interrupt has NOT occurred since the last read of this register.
			1 – Transmit LAPD Interrupt has occurred since the last read of this register.

Table 623: TxDS3 M-Bit Mask Register (Address Location= 0xN335)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Т	TxFEBEDat[2:0]			Tx P-Bit Error	Т	xM_Bit_Mask[2:	0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DECRIPTION
7 - 5	TxFEBEDat	R/W	Transmit FEBE Value:
	[2:0]		These READ/WRITE bit-fields, along with "FEBE Register Enable" permit the user to configure the Frame Generator block to transmit FEBE values (to the remote terminal) based upon the contents of these bit-fields.
			If the user sets the "FEBE Register Enable" bit-field to "1", then the Frame Generator block will write the contents of these bit-fields into the FEBE bits, within each outbound DS3 frame.
			If the user sets the "FEBE Register Enable" bit-field to "0" then these register bits will be ignored.
4	FEBE	R/W	Transmit FEBE (by Software) Enable:
	Register Enable		This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit FEBE values (to the remote terminal) per register setting via the "TxFEBEDat[2:0]" bit-field. This option provides the user with software control over the "outbound" FEBE values, within the DS3 data stream.
			0 – Configures the Frame Generator block to transmit FEBE values based upon receive conditions, as determined by the companion Frame Synchronizer block.
			1 - Configures the Frame Generator block to write the contents of the "TxFEBEDat[2:0]" bit-fields into the FEBE bits, within each "outbound" DS3 frame.
3	Tx P-Bit	R/W	Transmit P-Bit Error:
	Error	orock	This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with erred P-bits, as indicated below.
	The	The ata	DS3 frames with correct P-bits are generated and transmitted to the remote terminal equipment.
	·		1 – DS3 frames with erred P-bits are generated and transmitted to the remote terminal equipment.
2 – 0	TxM_Bit_	R/W	Transmit M-Bit Error:
	Mask[2:0]		These READ/WRITE bit-fields permit the user to configure the Frame Generator block to transmit DS3 frames with erred M-bits.
			These three (3) bit-fields correspond to the three M-bits, within each outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of these bit-fields and the value of the three M-bits. The results of this calculation will be written back into the M-bit positions within each outbound DS3 frame.
			The user should set these bit-fields to "0, 0, 0" for normal (e.g., un-erred) operation.

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 624: TxDS3 F-Bit Mask # 1 Register (; Address Location= 0xN336)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused			F_Bit Mask[27]/ UDL Bit # 9 (C73)	F_Bit Mask [26]/ UDL Bit # 8 (C72)	F_Bit Mask [25]/ UDL Bit # 7 (C71)	F_Bit Mask [24]/	
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3	F Bit Mask[27]/	R/W	Transmit F-Bit Error – Bit 28/UDL Bit #9 (C73):
	UDL Bit # 9 (C73)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
			If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 28:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
			This F-bit corresponds with the 28 th F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 28 th F-bit. The results of this calculation will be written back into the 28 th F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 – Insert Enable for UDL Bit # 9 or C73 bit:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to externally accept an overhead bit and insert it into the "UDL Bit #9 (or C73)" bit-fields, within the outbound DS3 data-stream.
		N'	 O – Configures the Frame Generator to externally accept and insert data into this overhead bit-field.
		Dior.	1 – Configures the Frame Generator to NOT externally accept and insert data into this overhead bit-field.
2	F Bit Mask	R/W	Transmit F-Bit Error – Bit 27/UDL Bit # 8 (C72):
	[26]/ UDL Bit #8 (C72)	98.00	The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
	(3.2)	.0	If "TxOHSrc" = 0 - Transmit F-Bit Error - Bit 27
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
			This F-bit corresponds with the 27 th F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 27 th F-bit. The results of this calculation will be written back into the 27 th F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 − Insert Enable for UDL Bit # 8 or C72 bit:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to externally accept an overhead bit and insert it into the "UDL Bit #8 (or C72)" bit-fields, within the outbound DS3 data-stream.

			0 – Configures the Frame Generator to externally accept and insert data into this overhead bit-field.
			1 – Configures the Frame Generator to NOT externally accept and insert data into this overhead bit-field.
1	F Bit Mask	R/W	Transmit F-Bit Error – Bit 26/UDL Bit # 7 (C71):
	[25]/ UDL Bit # 7 (C71)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
	(3.1)		If "TxOHSrc" = 0 - Transmit F-Bit Error - Bit 26:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
			This F-bit corresponds with the 26 th F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 26 th F-bit. The results of this calculation will be written back into the 26 th F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 – Insert Enable for UDL Bit # 7 or C71 bit:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to externally accept an overhead bit and insert it into the "UDL Bit #7 (or C71)" bit-fields, within the outbound DS3 data-stream.
			0 – Configures the Frame Generator to externally accept and insert data into this overhead bit field.
			1 – Configures the Frame Generator to NOT externally accept and insert data into this overhead bit-field.
0	F Bit Mask [24]	R/W	Transmit F-Bit Error – Bit 25:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
		roduct to the	This F-bit corresponds with the 25 th F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 25 th F-bit. The results of this calculation will be written back into the 25 th F-bit position, within each outbound DS3 frame.
		" Elle	The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
	The	to m	Note: This bit-field is ignored if Bit 7 (TxOHSrc), within the "Test Register (Address Location= 0xN30C) is set to the "1".



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 625: TxDS3 F-Bit Mask # 2 Register (Address Location= 0xN337)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
F_Bit Mask [23]/ UDL Bit # 6 (C63)	F_Bit Mask [22]/ UDL Bit # 5 (C62)	F_Bit Mask [21]/ UDL Bit # 4 (C61)	F_Bit Mask [20]	F_Bit Mask [19]/ DL Bit # 3 (C53)	F_Bit Mask [18]/ DL Bit # 2 (C52)	F_Bit Mask [17]/ DL Bit # 1 (C51)	F_Bit Mask [16]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	F Bit Mask[23]/	R/W	Transmit F-Bit Error – Bit 24/UDL Bit # 6 (C63):
	UDL Bit # 6 (C63)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Indirect Address = 0xNE, 0x0C; Direct Address Address Location= 0xNFN30C) is set to "1" or "0".
			If "TxOHSrc" = 0 - Transmit F-Bit Error Bit 24:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
			This F-bit corresponds with the 24th F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 24th F-bit. The results of this calculation will be written back into the 24th F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 Insert Enable for UDL Bit # 6 or C63 bit:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to externally accept an overhead bit and insert it into the "UDL Bit # 6 (or C63)" bit-fields, within the outbound DS3 data-stream.
			0 - Configures the Frame Generator to externally accept and insert data into this overhead bit-field.
		arod!	1 Configures the Frame Generator to NOT externally accept and insert data into this overhead bit-field.
6	F Bit Mask	R/W	Transmit F-Bit Error – Bit 23/UDL Bit # 5 (C62):
	[22]/ UDL Bit # 5 (C62)	Agra	The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
	(552)	2	If "TxOHSrc" = 0 - Transmit F-Bit Error - Bit 23:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
			This F-bit corresponds with the 23 rd F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 23 rd F-bit. The results of this calculation will be written back into the 23rd F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 - Insert Enable for UDL Bit # 5 or C62 bit:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to externally accept an overhead bit and insert it into the "UDL Bit # 5 (or C62)" bit-fields, within the outbound DS3 data-stream.
			0 - Configures the Frame Generator to externally accept and insert data into

			this overhead bit-field.
			1- Configures the Frame Generator to NOT externally accept and insert data into this overhead bit-field.
5	F Bit Mask [21]/	R/W	Transmit F-Bit Error – Bit 22/UDL Bit # 4 (C61):
	UDL Bit # 4 (C61)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
	,		If "TxOHSrc" = 0 - Transmit F-Bit Error - Bit 22:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
			This F-bit corresponds with the 22 nd F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 22 nd F-bit. The results of this calculation will be written back into the 22 nd F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 - Insert Enable for UDL Bit # 4 or C61 bit:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to externally accept an overhead bit and insert it into the "UDL Bit # 4 (or C61)" bit-fields, within the outbound DS3 data-stream.
			0 - Configures the Frame Generator to externally accept and insert data into this overhead bit-field.
			1- Configures the Frame Generator to NOT externally accept and insert data into this overhead bit-field.
4	F Bit Mask [20]	R/W	Transmit F-Bit Error - Bit 21:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
		duct	This F-bit corresponds with the 21 st F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 21 st F-bit. The results of this calculation will be written back into the 21 st F-bit position, within each outbound DS3 frame.
		10, 10,	The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
3	F Bit Mask	R/W	Transmit F-Bit Error – Bit 20/DL Bit # 3 (C53):
	[19]/ DL Bit #3 (C53)	grad u	The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
	(===)	3 1.	If "TxOHSrc" = 0 - Transmit F-Bit Error - Bit 20:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
			This F-bit corresponds with the 20 th F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 20 th F-bit. The results of this calculation will be written back into the 20 th F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 - Insert Enable for DL Bit # 3 or C53 bit:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to externally accept an overhead bit and insert it into the "DL Bit # 3 (or C53)" bit-fields, within the outbound DS3 data-stream.
			0 - Configures the Frame Generator to externally accept and insert data into

Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			this overhead bit-field.
			1- Configures the Frame Generator to NOT externally accept and insert data into this overhead bit-field.
2	F Bit Mask	R/W	Transmit F-Bit Error – Bit 19/DL Bit # 2 (C52):
	[18]/ DL Bit # 2 (C52)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
	(002)		If "TxOHSrc" = 0 - Transmit F-Bit Error - Bit 19:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
			This F-bit corresponds with the 19 th F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 19 th F-bit. The results of this calculation will be written back into the 19 th F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 - Insert Enable for DL Bit # 2 or C52 bit:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to externally accept an overhead bit and insert it into the "DL Bit # 2 (or C52)" bit-fields, within the outbound DS3 data-stream.
			0 - Configures the Frame Generator to externally accept and insert data into this overhead bit-field.
			1- Configures the Frame Generator to NOT externally accept and insert data into this overhead bit-field.
1	F Bit Mask	R/W	Transmit F-Bit Error – Bit 18/DL Bit # 1 (C51):
	[17]/ DL Bit # 1 (C51)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
	(,		If "TxOHSrc" = 0 Transmit F-Bit Error – Bit 18:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
	N	ie prodi	This F-bit corresponds with the 18 th F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 18 th F-bit. The results of this calculation will be written back into the 18 th F-bit position, within each outbound DS3 frame.
	^	100	The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
		3	If "TxOHSrc" = 1 - Insert Enable for DL Bit # 1 or C51 bit:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to externally accept an overhead bit and insert it into the "DL Bit # 1 (or C51)" bit-fields, within the outbound DS3 data-stream.
			0 - Configures the Frame Generator to externally accept and insert data into this overhead bit-field.
			1- Configures the Frame Generator to NOT externally accept and insert data into this overhead bit-field.
0	F Bit Mask [16]	R/W	Transmit F-Bit Error – Bit 17:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
			This F-bit corresponds with the 17 th F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 17 th F-bit. The results of this





calculation will be written back into the 17 th F-bit position, within each outbound DS3 frame.
The user should set this bit-field to "0" for normal (e.g., un-erred) operation.

The product are no longered (OBS)

The product are no longered (OBS)

The product are no longered (OBS)



Table 626: TxDS3 F-Bit Mask # 3 Register (Address Location= 0xN338)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
F_Bit Mask [15]/ FEBE Bit 3 (C43)	F_Bit Mask [14]/ FEBE Bit 2 (C42)	F_Bit Mask [13]/ FEBE Bit 1 (C41)	F_Bit Mask [12]	F_Bit Mask [11]/ CP Bit # 3 (C33)	F_Bit Mask [10]/ CP Bit # 2 (C32)	F_Bit Mask [9]/ CP Bit # 1 (C31)	F_Bit Mask [8]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	F Bit Mask[15]/	R/W	Transmit F-Bit Error – Bit 16/FEBE Bit # 3 (C43):
	FEBE Bit # 3 (C43)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
			If "TxOHSrc" = 0 - Transmit F-Bit Error - Bit 16:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
			This F-bit corresponds with the 16 th F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 16 th F-bit. The results of this calculation will be written back into the 16 th F-bit position, within each outbound DS3 frame.
			The user should set this bit field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 Insert Enable for FEBE Bit # 3 or C43 bit:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to externally accept an overhead bit and insert it into the "FEBE Bit # 3 (or C43)" bit-fields, within the outbound DS3 data-stream.
			0 - Configures the Frame Generator to externally accept and insert data into this overhead bit field.
		۵	1- Configures the Frame Generator to NOT externally accept and insert data into this overhead bit-field.
6	F Bit Mask [14]/	R/W	Transmit F-Bit Error – Bit 15/FEBE Bit # 2 (C42):
	FEBE Bit # 2 (C42)	80,0	The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
		10,	If "TxOHSrc" = 0 - Transmit F-Bit Error - Bit 15:
		0	This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
			This F-bit corresponds with the 15 th F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 15 th F-bit. The results of this calculation will be written back into the 15 th F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 - Insert Enable for FEBE Bit # 2 or C42 bit:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to externally accept an overhead bit and insert it into the "FEBE Bit # 2 (or C42)" bit-fields, within the outbound DS3 data-stream.
			0 - Configures the Frame Generator to externally accept and insert data into this overhead bit-field.
			1- Configures the Frame Generator to NOT externally accept and insert data

			into this overhead bit-field.
5	F Bit Mask [13]/	R/W	Transmit F-Bit Error – Bit 14/FEBE Bit # 1 C41):
	FEBE Bit 1 (C41)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
			If "TxOHSrc" = 0 - Transmit F-Bit Error - Bit 14:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
			This F-bit corresponds with the 14 th F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 14 th F-bit. The results of this calculation will be written back into the 14 th F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 - Insert Enable for FEBE Bit # 1 or C41 bit:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to externally accept an overhead bit and insert it into the "FEBE Bit # 1 (or C41)" bit-fields, within the outbound DS3 data-stream.
			0 - Configures the Frame Generator to externally accept and insert data into this overhead bit-field.
			1- Configures the Frame Generator to NOT externally accept and insert data into this overhead bit-field.
4	F Bit Mask [12]	R/W	Transmit F-Bit Error - Bit 13
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
			This F-bit corresponds with the 13 th F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 13 th F-bit. The results of this calculation will be written back into the 13 th F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
3	F Bit Mask [11]/	R/W	Transmit F-Bit Error – Bit 12/CP Bit # 3 (C33):
	CP Bit # 3 (C33)	000	The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
	6,6	6	if "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 12:
	The	096	This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
		affe	This F-bit corresponds with the 12th F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 12th F-bit. The results of this calculation will be written back into the 12th F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 - Insert Enable for CP Bit # 3 or C33 bit:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to externally accept an overhead bit and insert it into the "CP Bit # 3 (or C33)" bit-fields, within the outbound DS3 data-stream.
			0 - Configures the Frame Generator to externally accept and insert data into this overhead bit-field.
			1- Configures the Frame Generator to NOT externally accept and insert data into this overhead bit-field.

2	F Bit Mask [10]/	R/W	Transmit F-Bit Error – Bit 11/CP Bit # 2 (C32):
	CP Bit # 2 (C32)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
			If "TxOHSrc" = 0 - Transmit F-Bit Error - Bit 11:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
			This F-bit corresponds with the 11th F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 11th F-bit. The results of this calculation will be written back into the 11th F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 - Insert Enable for CP Bit # 2 or C32 bit:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to externally accept an overhead bit and insert it into the "CP Bit # 2 (or C32)" bit-fields, within the outbound DS3 data-stream.
			0 - Configures the Frame Generator to externally accept and insert data into this overhead bit-field.
			1- Configures the Frame Generator to NOT externally accept and insert data into this overhead bit-field.
1	F Bit Mask [9]/	R/W	Transmit F-Bit Error – Bit 10/CP Bit # 1 (C31):
	CP Bit # 1 (C31)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
			If "TxOHSrc" = 0 - Transmit F-Bit Error - Bit 10:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
			This F-bit corresponds with the 10th F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 10th F-bit. The results of this calculation will be written back into the 10th F-bit position, within each outbound DS3 frame.
		S	The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
		400	If "TxOHSrc" = 1 - Insert Enable for CP Bit # 1 or C31 bit:
	N/N	0,0	This READ/WRITE bit-field permits the user to configure the Frame Generator block to externally accept an overhead bit and insert it into the "CP Bit # 1 (or C31)" bit-fields, within the outbound DS3 data-stream.
		9,0	o - Configures the Frame Generator to externally accept and insert data into this overhead bit-field.
			1- Configures the Frame Generator to NOT externally accept and insert data into this overhead bit-field.
0	F Bit Mask [8]	R/W	Transmit F-Bit Error – Bit 9:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
			This F-bit corresponds with the 9th F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 9th F-bit. The results of this calculation will be written back into the 9th F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
L	I.		

Table 62: TxDS3 F-Bit Mask # 4 Register (Address Location= 0xN339)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
F_Bit Mask [7]/ UDL Bit # 3 (C23)	F_Bit Mask [6]/ UDL Bit # 2 (C22)	F_Bit Mask [5]/ UDL Bit # 1 (C21)	F_Bit Mask [4]/ X Bit # 2	F_Bit Mask [3]/ FEAC Bit (C13)	F_Bit Mask [2]/ NA Bit (C12)	F_Bit Mask [1]/ AIC Bit (C11)	F_Bit Mask [0]/ X Bit # 1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	F Bit Mask[7]/	R/W	Transmit F-Bit Error – Bit 8/UDL Bit # 3 (C23):
	UDL Bit # 3 (C23)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
			If "TxOHSrc" = 0 - Transmit F-Bit Erroi - Bit 8:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
			This F-bit corresponds with the 8th F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 8th F-bit. The results of this calculation will be written back into the 8th F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 - Insert Enable for UDL Bit # 3 or C23 bit:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to externally accept an overhead bit and insert it into the "UDL Bit # 3 (or C23)" bit-fields, within the outbound DS3 data-stream.
			0 - Configures the Frame Generator to externally accept and insert data into this overhead bit-field.
		HIL	1- Configures the Frame Generator to NOT externally accept and insert data into this overhead bit-field.
6	F Bit Mask [6]/	R/W	Transmit F-Bit Error – Bit 7/UDL Bit # 2 (C22):
	UDL Bit # 2 (C22)	. 'S'	The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
	1	9. 9	If "TxOHSrc" = 0 - Transmit F-Bit Error - Bit 7:
		Silve	This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
			This F-bit corresponds with the 7th F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 7th F-bit. The results of this calculation will be written back into the 7th F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 - Insert Enable for UDL Bit # 2 or C22 bit:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to externally accept an overhead bit and insert it into the "UDL Bit # 2 (or C22)" bit-fields, within the outbound DS3 data-stream.
			0 - Configures the Frame Generator to externally accept and insert data into this overhead bit-field.
			1- Configures the Frame Generator to NOT externally accept and insert data

			into this overhead bit-field.
5	F Bit Mask [5]/	R/W	Transmit F-Bit Error – Bit 6/UDL Bit # 1 (C21):
	UDL Bit # 1 (C21)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
			If "TxOHSrc" = 0 - Transmit F-Bit Error - Bit 6:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
			This F-bit corresponds with the 6th F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 6th F-bit. The results of this calculation will be written back into the 6th F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 - Insert Enable for UDL Bit # 1 or C21 bit:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to externally accept an overhead bit and insert it into the "UDL Bit # 1 (or C21)" bit-field, within the outbound DS3 data-stream.
			0 - Configures the Frame Generator to externally accept and insert data into this overhead bit-field.
			1- Configures the Frame Generator to NOT externally accept and insert data into this overhead bit-field
4	F Bit Mask [4]/	R/W	Transmit F-Bit Error -Bit 5/X Bit # 2:
	X Bit # 2		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
			If "TxOHSrc" = 0 - Transmit F-Bit Error - Bit 5:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
			This F-bit corresponds with the 5th F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 5th F-bit. The results of this calculation will be written back into the 5th F-bit position, within each outbound DS3 frame.
		,C	The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
		6,	If "TxOHSrc" = 1 - Insert Enable for X Bit # 2:
	~~	lo is	This READ/WRITE bit-field permits the user to configure the Frame Generator block to externally accept an overhead bit and insert it into the "X-Bit # 2" bit-field, within the outbound DS3 data-stream.
		7	0 - Configures the Frame Generator to externally accept and insert data into this overhead bit-field.
			1- Configures the Frame Generator to NOT externally accept and insert data into this overhead bit-field.
3	F Bit Mask [3]/	R/W	Transmit F-Bit Error – Bit 4/FEAC Bit (C13):
	FEAC Bit (C13)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
			If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 4:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
			This F-bit corresponds with the 4th F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 4th F-bit. The results of this calculation will be

			written back into the 4th F-bit position, within each outbound DS3 frame.
			• • •
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 - Insert Enable for FEAC or C13 bit:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to externally accept an overhead bit and insert it into the "FEAC (or C13)" bit-field, within the outbound DS3 data-stream.
			0 - Configures the Frame Generator to externally accept and insert data into this overhead bit-field.
			1- Configures the Frame Generator to NOT externally accept and insert data into this overhead bit-field.
2	F Bit Mask [2]/	R/W	Transmit F-Bit Error – Bit 3/NA Bit (C12):
	NA Bit (C12)		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
			If "TxOHSrc" = 0 – Transmit F-Bit Error – Bit 3:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
			This F-bit corresponds with the 3rd F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 3rd F-bit. The results of this calculation will be written back into the 3rd F-bit position, within each outbound DS3 frame.
			The user should set this bit field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 - Insert Enable for NA or C12 bit:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to externally accept an overhead bit and insert it into the "NA (or C12)" bit-field, within the outbound DS3 data-stream.
			0 - Configures the Frame Generator to externally accept and insert data into this overhead bit-field.
			1- Configures the Frame Generator to NOT externally accept and insert data into this overhead bit-field.
1	F Bit Mask [1]/	R/W	Transmit F-Bit Error – Bit 2/AIC Bit (C11):
	AIC Bit (C11)	NO SK	The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".
		xo.	TxOHSrc" = 0 – Transmit F-Bit Error – Bit 2:
	7, 8	and	This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.
		<i>'</i>	This F-bit corresponds with the 2^{nd} F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 2^{nd} F-bit. The results of this calculation will be written back into the 2^{nd} F-bit position, within each outbound DS3 frame.
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.
			If "TxOHSrc" = 1 - Insert Enable for AIC or C11 bit:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to externally accept an overhead bit and insert it into the "AIC (or C11)" bit-field, within the outbound DS3 data-stream.
			0 - Configures the Frame Generator to externally accept and insert data into this overhead bit-field.
			1- Configures the Frame Generator to NOT externally accept and insert data into this overhead bit-field.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

0	F Bit Mask [0]/	R/W	Transmit F-Bit Error – Bit 1/X Bit # 1:		
	X Bit # 1		The exact function of this register bit depends upon whether Bit 7 (TxOHSrc), within the "Test Register" (Address Location= 0xN30C) is set to "1" or "0".		
			If "TxOHSrc" = 0 - Transmit F-Bit Error - Bit 1:		
		This READ/WRITE bit-field permits the user to configure the Frame Generator block to transmit DS3 frames with an erred F bit.			
			This F-bit corresponds with the 1 st F-bit, within a given outbound DS3 frame. The Frame Generator block will perform an XOR operation with the contents of this bit-field and value of the 1 st F-bit. The results of this calculation will be written back into the 1 st F-bit position, within each outbound DS3 frame.		
			The user should set this bit-field to "0" for normal (e.g., un-erred) operation.		
			If "TxOHSrc" = 1 - Insert Enable for X Bit # 1:		
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to externally accept an overhead bit and insert it into the "X-Bit # 1" bit-field, within the outbound DS3 data-stream.		
			0 - Configures the Frame Generator to externally accept and insert data into this overhead bit-field.		
			1- Configures the Frame Generator to NOT externally accept and insert data into this overhead bit-field.		
1- Configures the Frame Generator to NOT externally accept and insert data into this overhead bit-field.					

Table 628: Transmit DS3 Pattern Register (Address Location= 0xN34C)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 0	
TxAIS - Unframed All Ones	Unused		TxLOS Pattern	Transmit_Idle_Pattern[3:0]			
R/W	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	1	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	TxAIS - Unframed All	R/W	Transmit AIS – Unframed All Ones:
	Ones		This READ/WRITE bit-field permits the user to configure the "Frame Generator" block to transmit either of the following pattern, anytime it is configured to transmit an AIS signal.
			 A "Framed, repeating 1, 0, 1, 0 pattern (per Bellcore GR-499-CORE) or An "Unframed All Ones" pattern.
			0 - Configures the Frame Generator to transmit the "Framed, Repeating 1, 0, 1, 0, pattern; whenever it is configured to transmit an AIS pattern
			1- Configures the Frame Generator to transmit an "Unframed, All-Ones" pattern, whenever it is configured to transmit an AIS signal.
6 - 5	Unused	R/W	
4	TxLOS Pattern	R/W	Transmit LOS Pattern:
		orpi	This READ/WRITE bit-field permits the user to configure the "Frame Generator" block to transmit either an "All Zeros" or an "All Ones" pattern, anytime it is configured to transmit an "LOS Pattern".
	أيرا	210	0 Configures the Frame Generator to transmit an "All Zeros" pattern, whenever it is configured to transmit an LOS pattern.
	oroche	5, 40	1 – Configures the Frame Generator to transmit an "All Ones" pattern, whenever it is configured to transmit an LOS pattern.
3 - 0	Tx_ldle Pattern[3:0]	/R/W	Transmit Idle Pattern:
	11, 9stoy l		These READ/WRITE bit-fields permit the user to specify the type of pattern the Frame Generator should send, whenever it is transmitting the "DS3 Idle" pattern.
			Note: Setting these bit-fields to "[1, 1, 0, 0] configure the Frame Generator block to transmit a "Framed, repeating "1, 1, 0, 0," pattern (per Bellcore GR-499-CORE) requirements.



1.12.7 Transmit E3, ITU-T G.751 Related Registers

Table 629: TxE3 Configuration Register – G.751 (Address Location= 0xN330)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TxBIP-4 Enable	TxASrc	Sel[1:0]	TxNSrcSel[1:0]		TxAIS Enable	TxLOS Enable	TxFAS Source Sel
R/W	R/W	R/W	R/W	R/W R/W		R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре		DESCRIPTION					
7	TxBIP-4 Enable	R/W	Transmit BIP-4 Enable: This READ/WRITE bit-field permits the user to configure the Frame Generator block to do the following: Compute the BIP-4 value over a given E3 frame. Insert this BIP-4 value into the last nibble-field within the very next E3 frame. Description of the last nibble field within the very next E3 frame. This read of the property of the property of the last nibble frame. This read of the property of the						
6 - 5	TxASrcSel[1:0]	R/W	These two READ/ type of data that E3 data stream, a	The "TxA" bit-field, within the "TxE3 Service Bit" register (Address Location= 0xN335). Not Valid - Do not use. The "A" bit is sourced via the "Payload Data Input Interface" block. This is discussed in greater detail in Section The Companion Frame Synchronizer					
4 – 3	TxNSrcSel[1:0]	R/W	block. In this case, the A bit will transmit the FEBE indicator to the remote terminal equipment. The A bit will be set to "1" when the companion Frame Synchronizer detects a BIP-4 error, and will be set to "0" when the Frame Synchronizer detects un-erred E3 frames. Transmit N Bit Source Select[1:0]: These two READ/WRITE bit-fields permit the user to specify the source or						

					s being carried via the "N" bits, within each "outbound" s indicated below.			
			TxNSrc	Sel[1:0]	Resulting Source of N Bit			
			0 The "TxN" bit-field, within the "TxE3 Service Bit" register (Address Location= 0xN335).					
			0	1	Not Valid – Do not use.			
			1	0	The LAPD Transmitter			
					In this case, the N bit will function as the LAPD/PMDL channel.			
			1	1	The "N" bit is sourced via the "Payload Data Input Interface" block.			
					This is discussed in greater detail in Section			
2	TxAIS Enable	R/W	Transmit	AIS Indi	cator:			
				e Genera	bit-field permits the user to (by software control) force ator to generate and transmit the AIS indicator to the juipment.			
			0 – Does AIS indica		gure the Frame Generator to generate and transmit the			
			indicator.	In this	Frame Generator to generate and transmit the AIS case, the Frame Generator will force all bits (within the a stream) to an "All Ones" pattern.			
		iol			field is ignored if the Frame Generator has been ed to transmit the LOS pattern.			
1	TxLOS Enable	R/W	Transmit	LOS (Pa	attern) Enable:			
	50,	neer o	the Frame	e Genera	E bit-field permits the user to (by software control) force tor block to transmit the LOS (Loss of Signal) pattern to all equipment.			
	We ha	3/1/84	0 – Does transmit t		nfigure the Frame Generator block to generate and pattern.			
	11 gate	9,	1 – Configures the Frame Generator block to generate and transmit the LOS pattern. In this case, the Frame Generator block will force all bits (within the "outbound" E3 data stream) to an "All Zeros" pattern.					
0	TxFAS Source Sel	R/W	Transmit FAS Source Select:					
			This READ/WRITE bit-field permits the user to specify the source of the FAS (Framing Alignment Signal), to be used in the "outbound" E3 data-stream, as indicated below.					
			0 – FAS b	oits are in	serted internally by the Frame Generator block.			
					sourced by the "Payload Data Input Interface" block. n greater detail in Section			

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 630: TxE3 LAPD Configuration Register – G.751 (Address Location= 0xN333)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unu	ised		Auto Retransmit	Reserved	TxLAPD Message Length	TxLAPD Enable
R/O	R/O	R/O	R/O	R/W	R/O	R/W	R/W
0	0	0	0	1	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3	Auto Retransmit	R/W	Auto-Retransmit of LAPD Message:
	Retiansinit		This READ/WRITE bit-field permits the user to configure the LAPD Transmitter to transmit PMDL messages, repeatedly at one-second intervals. Once the user enables this feature, and then commands the LAPD Transmitter to transmit a given PMDL Message; the LAPD Transmitter will then proceed to transmit this PMDL Message (based upon the contents within the Transmit LAPD Message Buffer) repeatedly at one second intervals.
			0 – Disables the Auto-Retransmit Feature.
			In this case, the PMDL Message will only be transmitted once, afterwards the LAPD Transmitter will proceed to transmit a continuous stream of Flag Sequence octets (0x7E) via the DL bits, within each output DS3 frame. No more PMDL Messages will be transmitted until the user commands another transmission.
			1 – Enables the Auto-Retransmit Feature.
			In this case, the LAPD Transmitter will transmit PMDL messages (based upon the contents within the Transmit LAPD Buffer) repeatedly at one-second intervals.
			Note: This bit-field is ignored if the LAPD Transmitter is disabled.
2	Reserved	R/O	AUC TOLLAND
1	TxLAPD Message	R/W	Transmit LAPD Message Length Select:
	Length	~6,	This READ/WRITE bit-field permits the user to specify the length of the payload data within the outbound LAPD/PMDL Message, as indicated below.
	•	1,99	0 Configures the LAPD Transmitter to transmit a LAPD/PMDL message that has a payload data size of 76 bytes.
			— Configures the LAPD Transmitter to transmit a LAPD/PMDL message that has a payload data size of 82 bytes.
0	TxLAPD	R/W	LAPD Transmitter Enable:
	Enable		This READ/WRITE bit-field permits the user to enable the LAPD Transmitter, within the channel. Once the user enables the LAPD Transmitter, it will immediately begin transmitting the Flag Sequence octet (0x7E) to the remote terminal via the outbound "DL" bits, within each DS3 data stream. The LAPD Transmitter will continue to do this until the user commands the LAPD Transmitter to transmit a PMDL Message.
			0 – Disables the LAPD Transmitter.
			1 – Enables the LAPD Transmitter.

Table 631: TxE3 LAPD Status/Interrupt Register - G.751 (Address Location= 0xN334)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused				TxDL Start	TxDL Busy	TxLAPD Interrupt Enable	TxLAPD Interrupt Status
R/O	R/O	R/O	R/O	R/W	R/O	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3	TxDL Start	R/W	Transmit LAPD Message Command:
			A "0" to "1" transition, within this bit field commands the LAPD Transmitter to begin the following activities:
			Reading out the contents of the Transmit LAPD Message Buffer.
			Zero-Stuffing of this data
			FCS Calculation and Insertion
			Fragmentation of this composite PMDL Message, and insertion into the "DL" bit-fields, within each outbound DS3 frame.
2	TxDL Busy	R/O	Transmit LAPD Controller Busy Indicator:
			This "READ-ONLY" bit-field indicates whether or not the Transmit LAPD Controller is currently busy transmitting a PMDL Message to the remote terminal equipment. The user can continuously poll this bit-field in order to check for completion of transmission of the LAPD/PMDL Message.
			0 – LAPD Transmitter is NOT busy transmitting a PMDL Message.
			1 APD Transmitter is currently busy transmitting a PMDL Message.
1	TxLAPD	R/W	Transmit LAPD Interrupt Enable:
	Interrupt Enable	blogh	This READ/WRITE bit-field permits the user to either enable or disable the Transmit LAPD Interrupt". If the user enables this interrupt, then the channel will generate an interrupt anytime the LAPD Transmitter has completed its transmission of a given LAPD/PMDL Message to the remote terminal.
	V/V	XO.	– Disables Transmit LAPD Interrupt.
		9,000	1 – Enables Transmit LAPD Interrupt.
0	TxLAPD	RUR	Transmit LAPD Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Transmit LAPD Interrupt" has occurred since the last read of this register.
			0 - Transmit LAPD Interrupt has NOT occurred since the last read of this register.
			1 – Transmit LAPD Interrupt has occurred since the last read of this register.

EXAR

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 632: TxE3 Service Bits Register – G.751 (Address Location= 0xN335)

Віт 7	Віт 6	Bit 5 Bit 4 Bit 3 Bit 2				Віт 1	Віт 0
		TxA	TxN				
R/O	R/O R/O R/O R/O R/O						R/W
0	0 0 0		0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 2	Unused	R/O	
1	TxA	R/W	Transmit A Bit:
			This READ/WRITE bit-field permits the user to control the state of the "A" bit, within each "outbound" E3 frame, as indicated below.
			0 – Forces each A bit (within the "outbound" E3 frame) to "0".
			1 – Forces each A bit (within the "outbound" E3 frame) to "1".
			Note: This bit-field is only valid in the Frame Generator block has been configured to use this bit-field as the source of the "A" bit (e.g., if "TxASrcSel[1:0] = "0, 0").
0	TxN	R/W	Transmit N Bit:
			This READ/WRITE bit-field permits the user to control the state of the "N" bit, within each "outbound" E3 frame, as indicated below.
			0 – Forces each N bit (within the "outbound" E3 frame) to "0".
			1 – Forces each N bit (within the "outbound" E3 frame) to "1".
			Note: This bit-field is only valid if the Frame Generator block has been configured to use this bit-field as the source of the "N" bit (e.g., if "TxNSroSel[1:0] = "0, 0").
		The	Note: This bit-field is only valid if the Frame Generator block has been configured to use this bit-field as the source of the "N" bit (e.g., if "TxNSrcSel[1:0] = "0, 0").

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 633: TxE3 FAS Error Mask Upper Register – G.751 (Address Location= 0xN348)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		TxFAS_Error_Mask_Upper[4:0]				
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 5	Unused	R/O	
4-0	TxFAS_Error_Mask_ Upper[4:0]	R/W	TxFAS Error Mask Upper[4:0]: These READ/WRITE bit-fields permit the user to insert bit errors into the upper five bits, within the FAS (Framing Alignment Signal), within the outbound E3 data stream. The Frame Generator will perform an XOR operation with the contents of these FAS bits, and this register. The results of this calculation will be inserted into the upper 5 FAS bit positions within the "outbound" E3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the FAS will be in error. Note: For normal operation, the user should set this register to 0x00.

Table 634: TxE3 FAS Error Mask Lower Register - G.751 (Address Location= 0xN349)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		000	TxFAS_	_Error_Mask_Lo	wer[4:0]	
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0,0	0	0	0	0
		k	0.00				

		<u></u>	
BIT NUMBER	Name	TYPE	DESCRIPTION
7 – 5	Unused	R/O	
4-0	TxFAS_Error_Mask_Lower[4:0]	R/W	TxFAS Error Mask Lower[4:0]: These READ/WRITE bit-fields permit the user to insert bit errors into the lower five bits, within the FAS (Framing Alignment Signal), within the outbound E3 data stream. The Frame Generator will perform an XOR operation with the contents of these FAS bits, and this register. The results of this calculation will be inserted into the lower 5 FAS bit positions within the "outbound" E3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the FAS will be in error. Note: For normal operation, the user should set this register to 0x00.

EXAR Experience Our Connectivit

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 635: TxE3 BIP-4 Mask Register – G.751 (Address Location= 0xN34A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unu	sed		TxBIP-4_Mask[3:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 4	Unused	R/O	
3 - 0	TxBIP-4_Mask_[3:0]	R/W	TxBIP-4 Error Mask[3:0]:
			These READ/WRITE bit-fields permit the user to insert bit errors into the BIP-4 bits, within the outbound E3 data stream.
			The Frame Generator will perform an XOR operation with the contents of the BIP-4 bits, and this register. The results of this calculation will be inserted into the BIP-4 bit positions within the "outbound" E3 data stream. For each bit-field (within this register) that is set to "1" the corresponding bit, within the BIP-4 will be in error. Note: For normal operation, the user should set this register to 0000.
	The product	corporate and analysis of the second	Note: For normal operation, the user should set this register to 0x00.



TRANSMIT E3, ITU-T G.832 RELATED REGISTERS 1.12.8

Table 636: TxE3 Configuration Register – G.832 (Address Location= 0xN330)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		TxDL in NR	Reserved	TxAIS Enable	TxLOS Enable	TxMA Rx
R/O	R/O	R/O	R/W	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 5	Unused	R/O	nis ed
4	TxDL in NR	R/W	Transmit DL (Data Link Channel) in NR Byte:
			This READ/WRITE bit-field permits the user to configure the Frame Generator to use either the NR or the GC byte as the LAPD/PMDL channel.
			0 – Configures the Frame Generator to transmit all "outbound" LAPD/PMDL Messages via the GC byte.
			1 – Configures the Frame Generator to transmit all "outbound" LAPD/PMDL Messages via the NR byte.
3	Unused	R/O	16 16 BS
2	TxAIS Enable	R/W	Transmit AIS Indicator
			This READ/WRITE bit-field permits the user to (by software control) force the Frame Generator to generate and transmit the AIS indicator to the remote terminal equipment.
		<u>k</u>	Does not configure the Frame Generator to generate and transmit the AIS indicator.
		oduc	1 Configures the Frame Generator to generate and transmit the AIS indicator. In this case, the Frame Generator will force all bits (within the courtbound" E3 data stream) to an "All Ones" pattern.
	100	Sh	Note: This bit-field is ignored if the Frame Generator has been configured to transmit the LOS pattern.
1	TxLOS Enable	R/W	Transmit LOS (Pattern) Enable:
	O	and	This READ/WRITE bit-field permits the user to (by software control) force the Frame Generator block to transmit the LOS (Loss of Signal) pattern to the remote terminal equipment.
			0 – Does not configure the Frame Generator block to generate and transmit the LOS pattern.
			1 – Configures the Frame Generator block to generate and transmit the LOS pattern. In this case, the Frame Generator block will force all bits (within the "outbound" E3 data stream) to an "All Zeros" pattern.
0	TxMA Rx	R/W	Transmit MA Byte from Receiver (Frame Synchronizer) Select:
			This READ/WRITE bit-field permits the user to configure the Frame Generator block to use either the Frame Synchronizer block or the "Tx MA Byte" Register as the source of the FERF and FEBE bit-fields (within the MA byte-field of the "outbound" E3 data stream); as indicated below.
			0 – Configures the Frame Generator to read in the contents of the "Tx MA Byte" register (Address Location= 0xN336), and write it into the "MA" byte-field

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

within each "outbound" E3 frame.
Note: This option permits the user to send FERF and FEBE indicators, under software control.
1 – Configures the Frame Generator to set the FERF and FEBE bit-fields to values, based upon conditions detected by the companion Frame Synchronizer block.

The product are no longered (OBS)

The product are no longered (OBS)

The product are no longered (OBS)

Table 637: TxE3 LAPD Configuration Register – G.832 (Address Location= 0xN333)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused			Auto Retransmit	Reserved	TxLAPD Message Length	TxLAPD Enable
R/O	R/O	R/O	R/O	R/W	R/O	R/W	R/W
0	0	0	0	1	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3	Auto	R/W	Auto-Retransmit of LAPD Message:
	Retransmit		This READ/WRITE bit-field permits the user to configure the LAPD Transmitter to transmit PMDL messages, repeatedly at one-second intervals. Once the user enables this feature, and then commands the LAPD Transmitter to transmit a given PMDL Message, the LAPD Transmitter will then proceed to transmit this PMDL Message (based upon the contents within the Transmit LAPD Message Buffer) repeatedly at one second intervals.
			0 – Disables the Auto-Retransmit Feature.
			In this case, the PMDL Message will only be transmitted once, afterwards the LAPD Transmitter will proceed to transmit a continuous stream of Flag Sequence octets (0x7E) via the DL bits, within each output DS3 frame. No more PMDL Messages will be transmitted until the user commands another transmission.
			1 – Enables the Auto-Retransmit Feature.
			In this case, the LAPD Transmitter will transmit PMDL messages (based upon the contents within the Transmit LAPD Buffer) repeatedly at one-second intervals.
			Note: This bit-field is ignored if the LAPD Transmitter is disabled.
2	Reserved	R/O	
1	TxLAPD Message	R/W	Transmit LAPD Message Length Select:
	Length	Sh	This READ/WRITE bit-field permits the user to specify the length of the payload data within the outbound LAPD/PMDL Message, as indicated below.
	1/h	9,9	0 – Configures the LAPD Transmitter to transmit a LAPD/PMDL message that has a payload data size of 76 bytes.
		3 1.	1 – Configures the LAPD Transmitter to transmit a LAPD/PMDL message that has a payload data size of 82 bytes.
0	TxLAPD	R/W	LAPD Transmitter Enable:
	Enable		This READ/WRITE bit-field permits the user to enable the LAPD Transmitter, within the channel. Once the user enables the LAPD Transmitter, it will immediately begin transmitting the Flag Sequence octet (0x7E) to the remote terminal via the outbound "DL" bits, within each DS3 data stream. The LAPD Transmitter will continue to do this until the user commands the LAPD Transmitter to transmit a PMDL Message.
			0 – Disables the LAPD Transmitter.
			1 – Enables the LAPD Transmitter.

Table 638: TxE3 LAPD Status/Interrupt Register - G.832 (Address Location= 0xN334)

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused				TxDL Busy	TxLAPD Interrupt Enable	TxLAPD Interrupt Status
R/O	R/O	R/O	R/O	R/W	R/O	R/W	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3	TxDL Start	R/W	Transmit LAPD Message Command:
			A "0" to "1" transition, within this bit-field commands the LAPD Transmitter to begin the following activities:
			Reading out the contents of the Transmit LAPD Message Buffer.
			Zero-Stuffing of this data
			FCS Calculation and Insertion
			Fragmentation of this composite PMDL Message, and insertion into the "DL" bit-fields, within each outbound DS3 frame.
2	TxDL Busy	R/O	Transmit LAPD Controller Busy Indicator:
			This "READ-ONLY" bit-field indicates whether or not the Transmit LAPD Controller is currently busy transmitting a PMDL Message to the remote terminal equipment. The user can continuously poll this bit-field in order to check for completion of transmission of the LAPD/PMDL Message.
			0 – LAPD Transmitter is NOT busy transmitting a PMDL Message.
			1 – LAPD Transmitter is currently busy transmitting a PMDL Message.
1	TxLAPD	R/W	Transmit LAPD Interrupt Enable:
	Interrupt Enable	.(This READ/WRITE bit-field permits the user to either enable or disable the "Transmit LAPD Interrupt". If the user enables this interrupt, then the channel will generate an interrupt anytime the LAPD Transmitter has completed its transmission of a given LAPD/PMDL Message to the remote terminal.
		6,	0-Disables Transmit LAPD Interrupt.
		No X	1 – Enables Transmit LAPD Interrupt.
0	TxLAPD	RUR	Transmit LAPD Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Transmit LAPD Interrupt" has occurred since the last read of this register.
			0 - Transmit LAPD Interrupt has NOT occurred since the last read of this register.
			1 – Transmit LAPD Interrupt has occurred since the last read of this register.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 639: TxE3 GC Byte Register – G.832 (Address Location= 0xN335)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	TxGC_Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	TxGC_Byte[7:0]	R/W	Transmit GC Byte:
			This READ/WRITE bit-field permits the user to specify the contents of the GC byte, within the "outbound" E3 data stream. The Frame Generator block will load the contents of this register in the GC byte-field, within each outbound E3 frame. Note: This register is ignored if the GC byte is configured to be the "LAPD/PMDL" channel.

Table 640: TxE3 MA Byte Register – G.832 (Address Location = 0xN336)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TxMA Byte[7:0]							
R/W	R/W	R/W	R/W	OR/W	R/W	R/W	R/W
0	0	0	1		0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	TxMA_Byte[7:0]	R/W	Transmit MA Byte:
	a d	oduct	This READ/WRITE bit-field permits the user to specify the contents of the MA byte, within the "outbound" E3 data stream. The Frame Generator block will load the contents of this register in the MA byte-field, within each outbound E3 frame. Note:
	we !	25/18	This register is ignored if the "Transmit MA Byte – from Receiver" option is selected (e.g., by setting "TxMA Rx = 1").
	1,90	and	This feature permits the user to transmit FERF and FEBE indicators upon software command.

EXAR Experience Our Connectivit

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 641: TxE3 NR Byte Register – G.832 (Address Location= 0xN337)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TxNR_Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	TxNR_Byte[7:0]	R/W	Transmit NR Byte:
			This READ/WRITE bit-field permits the user to specify the contents of the NR byte, within the "outbound" E3 data stream. The Frame Generator block will load the contents of this register in the NR byte-field, within each outbound E3 frame. Note: This register is ignored if the NR byte is configured to be the "LAPD/PMDL" channel.

Table 642: TxE3 TTB-0 Register – G.832 (Address Location= 0xN338)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TxTTB_Byte_0							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	0	0	0	0	0	0

NAME	TYPE	DESCRIPTION
TxTTB_Byte_0[7:0]	R/W	Transmit TTB (Trail-Trace Buffer) Byte 0:
		These READ/WRITE bits permit the user to specify the contents of
		"Trail-Trace Buffer Byte 0" within the outbound E3 data stream.
		By default, the MSB (Most Significant Bit) of this register bit will be set to
	اللاح الله	"1" order to permit the remote terminal to be able to identify this particular byte, as being the first byte of the "Trail-Trace Buffer"
	AUL .	Message.

Table 643: TxE3 TTB-1 Register – G.832 (Address Location = 0xN339)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	TxTTB_Byte_1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	TxTTB_Byte_1[7:0]	R/W	Transmit TTB (Trail-Trace Buffer) Byte 1:
			These READ/WRITE bits permit the user to specify the contents of "Trail-Trace Buffer Byte 1" within the outbound E3 data stream.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 644: TxE3 TTB-2 Register - G.832 (Address Location= 0xN33A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TxTTB_Byte_2							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	TYPE	DESCRIPTION
7 – 0	TxTTB_Byte_2[7:0]	R/W	Transmit TTB (Trail-Trace Buffer) Byte 2:
			These READ/WRITE bits permit the user to specify the contents of "Trail-Trace Buffer Byte 2" within the outbound E3 data stream.

Table 645: TxE3 TTB-3 Register – G.832 (Address Location= 0xN33B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TxTTB_Byte_3							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0 (1)	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	TxTTB_Byte_3[7:0]	R/W	Transmit TTB (Trail-Trace Buffer) Byte 3:
			These READ/WRITE bits permit the user to specify the contents of "Trail-Trace Buffer Byte 3" within the outbound E3 data stream.

Table 646: TxE3 TTB-4 Register – G.832 (Address Location= 0xN33C)

Віт 7	Віт 6	Віт 5	Вгт 4	Віт 3	Віт 2	Віт 1	Віт 0
	TxTTB_Byte_4						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0 0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	TxTTB_Byte_4[7:0]	R/W	Transmit TTB (Trail-Trace Buffer) Byte 4:
			These READ/WRITE bits permit the user to specify the contents of "Trail-Trace Buffer Byte 4" within the outbound E3 data stream.

Rev 2.0.0

Table 647: TxE3 TTB-5 Register – G.832 (Address Location= 0xN33D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TxTTB_Byte_5							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	TxTTB_Byte_5[7:0]	R/W	Transmit TTB (Trail-Trace Buffer) Byte 5:
			These READ/WRITE bits permit the user to specify the contents of "Trail-Trace Buffer Byte 5" within the outbound E3 data stream.

Table 648:	TxE3 TTB-6 R	egister – G.8	32 (Address l	_ocation= 0xN	133E)KIIS	Ò	
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	•		TxTTB_	_Byte_6			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	TxTTB_Byte_6[7:0]	R/W	Transmit TTB (Trail-Trace Buffer) Byte 6: These READ/WRITE bits permit the user to specify the contents of "Trail-Trace Buffer Byte 6" within the outbound E3 data stream.

Table 649: TxE3 TTB-7 Register – G.832 (Address Location= 0xN33F)

Віт 7	Віт 6	Віт 5	Віт.4	Віт 3	Віт 2	Віт 1	Віт 0	
	CXTTB_Byte_7							
R/W	R/W	RW	R/W	R/W	R/W	R/W	R/W	
0	0	Ø 0	0	0	0	0	0	

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	TxTTB_Byte_7[7:0]	R/W	Transmit TTB (Trail-Trace Buffer) Byte 7:
			These READ/WRITE bits permit the user to specify the contents of "Trail-Trace Buffer Byte 7" within the outbound E3 data stream.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 650: TxE3 TTB-8 Register – G.832 (Address Location = 0xN340)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TxTTB_Byte_8							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	TxTTB_Byte_8[7:0]	R/W	Transmit TTB (Trail-Trace Buffer) Byte 8:
			These READ/WRITE bits permit the user to specify the contents of "Trail-Trace Buffer Byte 8" within the outbound E3 data stream.

Table 651: TxE3 TTB-9 Register – G.832 (Address Location= 0xN341)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	TxTTB_Byte_9						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	TxTTB_Byte_9[7:0]	R/W	Transmit TTB (Trail-Trace Buffer) Byte 9: These READ/WRITE bits permit the user to specify the contents of
			"Trail-Trace Buffer Byte 9" within the outbound E3 data stream.

Table 652: TxE3 TTB-10 Register - G.832 (Address Location= 0xN342)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	TxTTB_Byte_10						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0 0	3 0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	TxTTB_Byte_10[7:0]	R/W	Transmit TTB (Trail-Trace Buffer) Byte 10:
			These READ/WRITE bits permit the user to specify the contents of "Trail-Trace Buffer Byte 10" within the outbound E3 data stream.

Rev 2.0.0

Table 653: TxE3 TTB-11 Register – G.832 (Address Location= 0xN343)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	TxTTB_Byte_11							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	TxTTB_Byte_11[7:0]	R/W	Transmit TTB (Trail-Trace Buffer) Byte 11:
			These READ/WRITE bits permit the user to specify the contents of "Trail-Trace Buffer Byte 11" within the outbound E3 data stream.

Table 654: 1	Table 654: TxE3 TTB-12 Register – G.832 (Address Location= 0xN344)						
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			TxTTB_	Byte_12			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	TxTTB_Byte_12[7:0]	R/W	Transmit TTB (Trail-Trace Buffer) Byte 12: These READ/WRITE bits permit the user to specify the contents of "Trail-Trace Buffer Byte 12" within the outbound E3 data stream.

Table 655: TxE3 TTB-13 Register - G.832 (Address Location= 0xN345)

Віт 7	Віт 6	Віт 5	Віт.4	Віт 3	Віт 2	Віт 1	Віт 0
TxTTB_Byte_13							
R/W	R/W	RW	R/W	R/W	R/W	R/W	R/W
0	0	0 0	0	0	0	0	0
	That's diff						

BIT NUMBER	Name	TYPE	DESCRIPTION
7 – 0	TxTTB_Byte_13[7:0]	R/W	Transmit TTB (Trail-Trace Buffer) Byte 13:
			These READ/WRITE bits permit the user to specify the contents of "Trail-Trace Buffer Byte 13" within the outbound E3 data stream.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 656: TxE3 TTB-14 Register - G.832 (Address Location= 0xN346)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	TxTTB_Byte_14							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	TxTTB_Byte_14[7:0]	R/W	Transmit TTB (Trail-Trace Buffer) Byte 14:
			These READ/WRITE bits permit the user to specify the contents of "Trail-Trace Buffer Byte 14" within the outbound E3 data stream.

Table 657: TxE3 TTB-15 Register - G.832 (Address Location= 0xN347)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	TxTTB_Byte_15_0						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	TxTTB_Byte_15[7:0]	R/W	Transmit TTB (Trail-Trace Buffer) Byte 15:
			These READ/WRITE bits permit the user to specify the contents of Trail-Trace Buffer Byte 15" within the outbound E3 data stream.
		di	70 19e
	•	at long	
	odu	Co.	ot P
	o Prost	I'M	
	Theata	We	
	or and	,	

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 658: TxE3 FA1 Error Mask Register – G.832 (Address Location= 0xN348)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	TxFA1_Mask_Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	TxFA1_Mask_Byte[7:0]	R/W	TxFA1 Error Mask Byte[7:0]:
			These READ/WRITE bit-fields permit the user to insert bit errors into the FA1 bytes, within the outbound E3 data stream.
			The Frame Generator will perform an XOR operation with the contents of the FA1 byte, and this register. The results of this calculation will be inserted into the FA1 byte position within the "outbound" E3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the FA1 byte will be in error. *Note: For normal operation, the user should set this register to 0x00.

Table 659: TxE3 FA2 Error Mask Register – G.832 (Address Location= 0xN349)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 2	Віт 1	Віт 0
			TxFA2_Mask_Byte[7:0]			
R/W	R/W	R/W	R/W R/W	R/W	R/W	R/W
0	0	0	0 0 0	0	0	0

BIT NUMBER	NAME	Type	DESCRIPTION
7 - 0	TxFA2_Mask_Byte[7:0]	R/W	TxFA2 Error Mask Byte[7:0]: These READ/WRITE bit-fields permit the user to insert bit errors into the FA2 bytes, within the outbound E3 data stream. The Frame Generator will perform an XOR operation with the contents of the FA2 byte, and this register. The results of this calculation will be inserted into the FA2 byte position within the
	3 1		"outbound" E3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the FA2 byte will be in error. Note: For normal operation, the user should set this register to 0x00.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 660: TxE3 BIP-8 Error Mask Register - G.832 (Address Location= 0xN34A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TxBIP-8_Mask_Byte[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	TxBIP-8_Mask_Byte[7:0]	R/W	TxBIP-8 (B1) Error Mask[7:0]:
			These READ/WRITE bit-fields permit the user to insert bit errors into the B1 bytes, within the outbound E3 data stream.
			The Frame Generator will perform an XOR operation with the contents of the B1 byte, and this register. The results of this calculation will be inserted into the B1 byte position within the "outbound" E3 data stream. For each bit-field (within this register) that is set to "1", the corresponding bit, within the B1 byte will be in error. Note: For normal operation, the user should set this register to 0x00.

Table 661: TxE3 SSM Register – G.832 (Address Location= 0xN34B)

					/		
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TxSSM Enable		Unused	90	000	TxSS	M[3:0]	
R/W	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TVDE	DESCRIPTION
7	TxSSM Enable	TYPE R/W	Transmit SSM Enable: This READ/WRITE bit-field permits the user to configure the Frame Generator block to operate in either the "Old ITU-T G.832 Framing" format or in the "New ITU-T G.832 Framing" format. 0 — Configures the Frame Generator block to support the "Pre October 1998" version of the E3, ITU-T G.832 framing format. 1 — Configures the Frame Generator block to support the "October 1998"
6 - 4	Unused	R/O	version of the E3, ITU-T G.832 framing format.
3 - 0	TxSSM[3:0]	R/W	Transmit Synchronization Status Message[3:0]: These READ/WRITE bit-fields permit the user to exercise software control over the contents of the "SSM" bits, within the MA byte of the "outbound" E3 data-stream. Note: These bit-fields are only active if the DS3/E3 Frame Generator block is active, and if Bit 7 (TxSSM Enable) of this register is set to "1".

1.12.9 AIS/PDI-P ALARM ENABLE REGISTER

Table 662: Receive DS3/E3 AIS/PDI-P Alarm Enable Register (Address Location= 0xN34D)

Віт 7	Віт 6	Віт 5 Віт 4		Віт 3	Віт 2	Віт 1	Віт 0
Unu	Unused Transm P(Do stream) LO		Transmit AIS (Down- stream) upon LOS	Transmit PDI- P (Down- stream) upon LOF	Transmit AIS (Down- stream) upon LOF	Transmit PDI- P (Down- stream) upon AIS	Transmit AIS (Down- stream) upon AIS
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0 0		0	0	0

Dir Nimeses	Nase	Type	Decomprise
BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 6	Unused	R/O	
5	Transmit PDI-P	R/W	Transmit PDI-P (Down-stream) upon LOS:
	(Down-stream) upon LOS		This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block and the Transmit SONET POH Processor block to automatically transmit the PDI-R Path Payload Defect Indicator) anytime the LOS defect is declared within the DS3 Ingress Path.
			More specifically, if this configuration is implemented then the following events will occur.
			If the Primary Frame Synchronizer block is operating the in "DS3/E3 Ingress" path
			If the Primary Frame Synchronizer block is operating in the "DS3/E3 Ingress" path, and if it were to declare the LOS defect (within the Ingress Path), then the Transmit SONET POH Processor block will automatically transmit the PDI-P indicator, by setting the C2 byte (within each "downstream" STS-1SPE) to the value "0xFC".
			Once the Primary Frame Synchronizer block clears the LOS defect, then the Transmit SONET POH Processor block will automatically setting the C2 byte (within each "down-stream" STS-1 SPE) to the "0x04".
			If the Secondary Frame Synchronizer block is operating in the "DS3/E3 Ingress" path
		oduct	If the Secondary Frame Synchronizer block is operating in the "DS3/E3 Ingress" path, and if it were to declare the LOS defect (within the Ingress Path), then the Transmit SONET POH Processor block will automatically transmit the PDI-P indicator by setting the C2 byte (within each "downstream" STS-1 SPE) to the value "0xFC".
	The	rogra	then the Secondary Frame Synchronizer block clears the LOS defect, then the Transmit SONET POH Processor block will automatically terminate its transmission of the PDI-P indicator by setting the C2 byte (within each "down-stream" STS-1 SPE) to the value "0x04".
		Q .	0 – Disables this "Transmit PDI-P (Down-stream) upon LOS feature.
			1 - Enables this "Transmit PDI-P (Down-stream) upon LOS feature.
4	Transmit AIS	R/W	Transmit AIS (Down-stream) upon LOS:
	(Down-stream) upon LOS		This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block to do all of the following, if the LOS defect is declared.
			If the Primary Frame Synchronizer block declares LOS:
			If the Primary Frame Synchronizer block declares the LOS detect (within its Receive Path) then it will automatically transmit the AIS indicator, via its output Path.
			If the Secondary Frame Synchronizer block declares LOS:
			If the Secondary Frame Synchronizer block declares the LOS defect (within its Receive Path) then it will automatically force the "Frame

	T		One and all block to manage to and top and the AIO in director
			Generator" block to generate and transmit the AIS indicator.
			0 – Disables the "Transmit AIS (Down-stream) upon LOS feature.
			1 – Enables the "Transmit AIS (Down-stream) upon LOS feature.
3	Transmit PDI-P	R/W	Transmit PDI-P (Down-stream) upon LOF:
	(Down-stream) upon LOF		This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block and the Transmit SONET POH Processor block to automatically transmit the PDI-P (Path – Payload Defect Indicator) anytime the LOF defect is declared within the DS3 Ingress Path.
			More specifically, if this configuration is implemented then the following events will occur.
			If the Primary Frame Synchronizer block is operating the in "DS3/E3 Ingress" path
			If the Primary Frame Synchronizer block is operating in the "DS3/E3 Ingress" path, and if it were to declare the LOF defect (within the Ingress Path), then the Transmit SONET POH Processor block will automatically transmit the PDI-P indicator, by setting the C2 byte (within each "downstream" STS-1 SPE) to the value "0xFC".
			Once the Primary Frame Synchronizer block clears the LOF defect, then the Transmit SONET POH Processor block will automatically setting the C2 byte (within each "down-stream" STS-1 SPE) to the "0x04".
		, lor	If the Secondary Frame Synchronizer block is operating in the "DS3/E3 Ingress" path
			If the Secondary Frame Synchronizer block is operating in the "DS3/E3 Ingress" path, and if it were to declare the LOF defect (within the Ingress Path), then the Transmit SONET POH Processor block will automatically transmit the PDI-P indicator by setting the C2 byte (within each "downstream" STS-1 SPE) to the value "0xFC".
			Once the Secondary Frame Synchronizer block clears the LOF defect, then the Transmit SONET POH Processor block will automatically terminate its transmission of the PDI-P indicator by setting the C2 byte (within each "down-stream" STS-1 SPE) to the value "0x04".
	×	70 × 8	0 – Disables this "Transmit PDI-P (Down-stream) upon LOF feature.
	400	00	P Enables this "Transmit PDI-P (Down-stream) upon LOF feature.
2	Transmit AIS		Transmit AIS (Down-stream) upon LOF:
	(Down-stream) upon LOF	R/W	This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block to do all of the following, if the LOF defect is declared.
	26		If the Primary Frame Synchronizer block declares LOF:
			If the Primary Frame Synchronizer block declares the LOF detect (within its Receive Path) then it will automatically transmit the AIS indicator, via its output Path.
			If the Secondary Frame Synchronizer block declares LOS:
			If the Secondary Frame Synchronizer block declares the LOF defect (within its Receive Path) then it will automatically force the "Frame Generator" block to generate and transmit the AIS indicator.
			0 - Disables the "Transmit AIS (Down-stream) upon LOF feature.
			1 – Enables the "Transmit AIS (Down-stream) upon LOF feature.
1	Transmit PDI-P	R/W	Transmit PDI-P (Down-stream) upon AIS:
	(Down-stream) upon AIS		This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block and the Transmit SONET POH Processor block to

	1	l	automatically, transmit the DDLD (Dath Davids of Date 1 1 2 4)
			automatically transmit the PDI-P (Path – Payload Defect Indicator) anytime the AIS defect is declared within the DS3 Ingress Path.
			More specifically, if this configuration is implemented then the following events will occur.
			If the Primary Frame Synchronizer block is operating the in "DS3/E3 Ingress" path
			If the Primary Frame Synchronizer block is operating in the "DS3/E3 Ingress" path, and if it were to declare the AIS defect (within the Ingress Path), then the Transmit SONET POH Processor block will automatically transmit the PDI-P indicator, by setting the C2 byte (within each "downstream" STS-1 SPE) to the value "0xFC".
			Once the Primary Frame Synchronizer block clears the AIS defect, then the Transmit SONET POH Processor block will automatically setting the C2 byte (within each "down-stream" STS-1 SPE) to the "0x04".
			If the Secondary Frame Synchronizer block is operating in the "DS3/E3 Ingress" path
			If the Secondary Frame Synchronizer block is operating in the "DS3/E3 Ingress" path, and if it were to declare the AIS defect (within the Ingress Path), then the Transmit SONET POH Processor block will automatically transmit the PDI-P indicator by setting the C2 byte (within each "downstream" STS-1 SPE) to the value "0xFC".
			Once the Secondary Frame Synchronizer block clears the AIS defect, then the Transmit SONET POH Processor block will automatically terminate its transmission of the PDI-P indicator by setting the C2 byte (within each "down-stream" STS-1 SPE) to the value "0x04".
			0 – Disables this "Transmit PDI-P (Down-stream) upon AIS feature.
			1 – Enables this "Transmit PDI-P (Down-stream) upon AIS feature.
0	Transmit AIS (Down-stream)	R/W	Transmit AIS (Down-stream) upon AIS:
	upon AIS		This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block to do all of the following, if the AIS defect is declared.
		ٽي.	If the Primary Frame Synchronizer block declares AIS:
	Thed	odine	If the Primary Frame Synchronizer block declares the AIS detect (within its Receive Path) then it will automatically transmit the AIS indicator, via its output Path.
		W &	If the Secondary Frame Synchronizer block declares AIS:
		andn	If the Secondary Frame Synchronizer block declares the AIS defect (within its Receive Path) then it will automatically force the "Frame Generator" block to generate and transmit the AIS indicator.
			0 - Disables the "Transmit AIS (Down-stream) upon AIS feature.
			1 – Enables the "Transmit AIS (Down-stream) upon AIS feature.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 663: Receive DS3/E3 AlS/PDI-P Alarm Enable Register – Secondary Frame Synchronizer (Address Location= 0xN3F2)

Віт 7	Віт 7 Віт 6 Віт 5		Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused		Transmit PDI- P (Down- stream) upon LOS	Transmit AIS (Down- stream) upon LOS	Transmit PDI- P (Down- stream) upon LOF	Transmit AIS (Down- stream) upon LOF	Transmit PDI- P (Down- stream) upon AIS	Transmit AIS (Down- stream) upon AIS
R/O	R/O R/O R/W		R/W	R/W	R/W	R/W	R/W
0	0 0 0 0		0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 6	Unused	R/O	
5	Transmit PDI-	R/W	Transmit PDI-P (Down-stream) upon LOS:
	P (Down- stream) upon LOS		This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block and the Transmit SONET POH Processor block to automatically transmit the PDI-P (Path – Payload Defect Indicator) anytime the LOS defect is declared within the DS3 Ingress Path.
			If the Secondary Frame Synchronizer block is operating in the "DS3/E3 Ingress" path
			If the Secondary Frame Synchronizer block is operating in the "DS3/E3 Ingress" path, and if it were to declare the LOS defect (within the Ingress Path), then the Transmit SONET POH Processor block will automatically transmit the PDI-P indicator by setting the C2 byte (within each "down-stream" STS-1 SPE) to the value "0xFC".
			Once the Secondary Frame Synchronizer block clears the LOS defect, then the Transmit SONET POH Processor block will automatically terminate its transmission of the PDI-P indicator by setting the C2 byte (within each "downstream" STS-1 SPE) to the value "0x04".
			0 - Disables this "Transmit PDI-P (Down-stream) upon LOS feature.
			1 – Enables this "Transmit PDI-P (Down-stream) upon LOS feature.
4	Transmit AIS (Down-stream)	R/W	Transmit AIS (Down-stream) upon LOS:
	upon LOS	100	This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block to do the following, if the LOS defect is declared.
		5	If the Secondary Frame Synchronizer block declares LOS:
	411.9	and	If the Secondary Frame Synchronizer block declares the LOS defect (within its Receive Path) then it will automatically force the "Frame Generator" block to generate and transmit the AIS indicator.
		0	0 - Disables the "Transmit AIS (Down-stream) upon LOS feature.
			1 – Enables the "Transmit AIS (Down-stream) upon LOS feature.
3	Transmit PDI-	R/W	Transmit PDI-P (Down-stream) upon LOF:
	P (Down- stream) upon LOF		This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block and the Transmit SONET POH Processor block to automatically transmit the PDI-P (Path – Payload Defect Indicator) anytime the LOF defect is declared within the DS3 Ingress Path.
			If the Secondary Frame Synchronizer block is operating in the "DS3/E3 Ingress" path
			If the Secondary Frame Synchronizer block is operating in the "DS3/E3 Ingress" path, and if it were to declare the LOF defect (within the Ingress Path), then the Transmit SONET POH Processor block will automatically transmit the PDI-P indicator by setting the C2 byte (within each "down-stream" STS-1 SPE) to the

			value "0xFC".
			Once the Secondary Frame Synchronizer block clears the LOF defect, then the Transmit SONET POH Processor block will automatically terminate its transmission of the PDI-P indicator by setting the C2 byte (within each "downstream" STS-1 SPE) to the value "0x04".
			0 – Disables this "Transmit PDI-P (Down-stream) upon LOF feature.
			1 – Enables this "Transmit PDI-P (Down-stream) upon LOF feature.
2	Transmit AIS	R/W	Transmit AIS (Down-stream) upon LOF:
	(Down-stream) upon LOF		This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block to do the following, if the LOF defect is declared.
			If the Secondary Frame Synchronizer block declares LOS:
			If the Secondary Frame Synchronizer block declares the LOF defect (within its Receive Path) then it will automatically force the "Frame Generator" block to generate and transmit the AIS indicator.
			0 – Disables the "Transmit AIS (Down-stream) upon LOF feature.
			1 – Enables the "Transmit AIS (Down-stream) upon LOF feature.
1	Transmit PDI-	R/W	Transmit PDI-P (Down-stream) upon AIS:
	P (Down- stream) upon AIS		This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block and the Transmit SQNET POH Processor block to automatically transmit the PDI-P (Path – Payload Defect Indicator) anytime the AIS defect is declared within the DS3 Ingress Path.
			If the Secondary Frame Synchronizer block is operating in the "DS3/E3 Ingress" path
			If the Secondary Frame Synchronizer block is operating in the "DS3/E3 Ingress" path, and if it were to declare the AIS defect (within the Ingress Path), then the Transmit SONET POH Processor block will automatically transmit the PDI-P indicator by setting the C2 byte (within each "down-stream" STS-1 SPE) to the value "0xFC".
		,0	Once the Secondary Frame Synchronizer block clears the AIS defect, then the Transmit SONET POH Processor block will automatically terminate its transmission of the PDI-P indicator by setting the C2 byte (within each "downstream" STS-1 SPE) to the value "0x04".
		6,	O Disables this "Transmit PDI-P (Down-stream) upon AIS feature.
		S K	1 – Enables this "Transmit PDI-P (Down-stream) upon AIS feature.
0	Transmit AIS	R/W	Transmit AIS (Down-stream) upon AIS:
	(Down-stream) upon AIS	2	This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block to do the following, if the AIS defect is declared.
			If the Secondary Frame Synchronizer block declares AIS:
			If the Secondary Frame Synchronizer block declares the AIS defect (within its Receive Path) then it will automatically force the "Frame Generator" block to generate and transmit the AIS indicator.
			0 – Disables the "Transmit AIS (Down-stream) upon AIS feature.
			1 – Enables the "Transmit AIS (Down-stream) upon AIS feature.
		•	

Rev 2.0.0

1.12.10 Performance Monitor Registers

Table 664: PMON Excessive Zero Count Registers - MSB (Address Location= 0xN34E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3 Віт 2		Віт 1	Віт 0	
PMON_EXZ_Count_Upper_Byte[7:0]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	PMON_EXZ_Count_Upper_Byte[7:0]	RUR	Performance Monitor – Excessive Zero Event Count – Upper Byte: These RESET-upon-READ bits, along with that within the "PMON Excessive Zero Count Register – LSB" combine to reflect the cumulative number of instances that a string of three or more consecutive zeros (for DS3 applications) or four or more consecutive zeros (for E3 applications) has been detected by the "Primary Frame Synchronizer" block since the last read of this register. This register contains the Most Significant byte of this 16-bit expression.

Table 665: PMON Excessive Zero Count Registers – LSB (Address Location= 0xN34F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
PMON_EXZ_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	200	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	PMON_EXZ_Count_Upper_Byte[7:0]	RUR	Performance Monitor – Excessive Zero Event Count – Lower Byte:
	o and		These RESET-upon-READ bits, along with that within the "PMON Excessive Zero Count Register – MSB" combine to reflect the cumulative number of instances that a string of three or more consecutive zeros (for DS3 applications) or four or more consecutive zeros (for E3 applications) has been detected by the "Primary Frame Synchronizer" block since the last read of this register. This register contains the Least Significant byte of this 16-bit expression.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 666: PMON Line Code Violation Count Registers – MSB (Address Location= 0xN350)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3 Віт 2		Віт 1	Віт 0		
PMON_LCV_Count_Upper_Byte[7:0]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	PMON LCV Count Upper Byte[7:0]	RUR	Performance Monitor- Line Code Violation Count Register – Upper Byte:
			These RESET-upon-READ bits along with that within the "PMON Line Code Violation Count – LSB" combine to reflect the cumulative number of Line Code Violations that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Most Significant byte of this 16-bit expression.

Table 667: PMON Line Code Violation Count Registers – SB (Address Location= 0xN351)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
PMON_LCV_Count_Lower_Byte[7:0]								
RUR	RUR	RUR	RUR 🕠	RUR	RUR	RUR	RUR	
0	0	0	0	0 0	0	0	0	

BIT NUMBER	NAME	TYPE	0	DESCRIPTION
7 – 0	PMON LCV Count Lower	RUR		ormance Monitor- Line Code Violation Count Register –
	Byte[7:0] And data data data data data data data da	et not	Thes Line cum dete last i	se RESET-upon-READ bits along with that within the "PMON Code Violation Count – MSB" combine to reflect the ulative number of Line Code Violations that have been cted by the Primary Frame Synchronizer block, since the read of this register. register contains the Least Significant byte of this 16-bit ession.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 668: PMON Framing Bit/Byte Error Count Register – MSB (Address Location= 0xN352)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	PMON_Framing_Bit/Byte_Error_Count_Upper_Byte[7:0]						
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	7 - 0 PMON_Framing Bit/Byte Error_Count_Upper Byte[7:0]	Performance Monitor – Framing Bit/Byte Error Count – Upper Byte: These RESET-upon-READ bits, along with that within the "PMON Framing Bit/Byte Error Count Register – LSB" combine to reflect the cumulative number of Framing bit (or byte) errors that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Most Significant byte of this 16-bit expression. Note: For DS3 applications, this register will increment for each F or M bit error detected. For E3, ITU-T G 751 applications, this register will increment for each FAS error detected. For E3, ITU-T G 832 applications, this register will increment for each FA1 or EA2 but a great applications.	
	The data	ict of the state o	These register bits are not active if the Primary Frame Synchronizer block has been by passed.



Rev 2.0.0

Table 669: PMON Framing Bit/Byte Error Count Register – LSB (Address Location= 0xN353)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
PMON_Framing_Bit/Byte_Error_Count_L					ver_Byte[7:0]		
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	PMON_Framing	RUR	Performance Monitor – Framing Bit/Byte Error Count – Lower Byte:
	Bit/Byte Error_Count_Lower Byte[7:0]		These RESET-upon-READ bits, along with that within the "PMON Framing Bit/Byte Error Count Register – MSB" combine to reflect the cumulative number of Framing bit (or byte) errors that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Least Significant byte of this 16-bit expression. *Note:* For DS3 applications, this register will increment for each F or M bit error detected. For E3, ITU-T G.751 applications, this register will increment for each FAS error detected. For E3, ITU-T G.832 applications, this register will increment for each FA1 or FA2 byte error detected. These register bits are not active if the Primary Frame Synchronizer block has been by-passed.
	The	ata di canada di	These register bits are not active if the Primary Frame Synchronizer block has been by-passed.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 670: PMON Parity/P-Bit Error Count Register - MSB (Address Location= 0xN354)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	PMON_Parity_Error_Count_Upper_Byte[7:0]						
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	PMON_P-Bit/Parity Bit Error_Count_Upper Byte[7:0]	RUR	Performance Monitor – P Bit/Parity Bit Error Count – Upper Byte: These RESET-upon-READ bits, along with that within the "PMON P-Bit/Parity Bit Error Count Register – LSB" combine to reflect the cumulative number of P bit errors (for DS3 applications) or BIP-8/BIP-4 errors (for E3 applications) that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Most Significant byte of this 16-bit expression.
			Note: These register bits are not active if the Primary Frame Synchronizer block has been by-passed.

Table 671: PMON Parity/P-Bit Error Count Register — SB (Address Location= 0xN355)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		PMON.	_Parity_Error_C	ount_Lower_B	yte[7:0]		
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	90, 90	0	0	0	0

BIT NUMBER	Name	TYPE	DESCRIPTION
7 - 0	PMON_P-Bit/Parity Bit Error_Count_Lower Byte[7:0]	RURA	Performance Monitor – P Bit/Parity Bit Error Count – Lower Byte: These RESET-upon-READ bits, along with that within the "PMON P-Bit/Parity Bit Error Count Register – MSB" combine to reflect the cumulative number of P bit errors (for DS3 applications) or BIP-8/BIP-4 errors (for E3 applications) that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Least Significant byte of this 16-bit expression. Note: These register bits are not active if the Primary Frame Synchronizer block has been by-passed.

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 672: PMON FEBE Event Count Register – MSB (Address Location= 0xN356)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	PMON_FEBE_Event				yte[7:0]		
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	PMON_FEBE Event_Count_Upper Byte[7:0]	RUR	Performance Monitor – FEBE Event Count – Upper Byte: These RESET-upon-READ bits, along with that within the "PMON FEBE Event Count Register – LSB" combine to reflect the cumulative number of "erred" FEBE events that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Most Significant byte of this 16-bit expression.
			Note: These register bits are not active if the Primary Frame Synchronizer block has been by-passed.

Table 673: PMON FEBE Event Count Register – LSB (Address Location= 0xN357)

Віт 7	Віт 6	Віт 5 Віт 4		Віт 3	Віт 2	Віт 1	Віт 0		
	PMON_FEBE_Event_Count_bower_Byte[7:0]								
RUR	RUR	RUR	RUR 🔾	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		
	oro lolleree								

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PMON_FEBE Event_Count_Lower Byte[7:0]	RUR AND	Performance Monitor – FEBE Event Count – Lower Byte: These RESET-upon-READ bits, along with that within the "PMON FEBE Event Count Register – MSB" combine to reflect the cumulative number of "erred" FEBE events that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Least Significant byte of this 16-bit expression. Note: These register bits are not active if the Primary Frame Synchronizer block has been by-passed.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 674: PMON CP-Bit Error Count Register – MSB (Address Location= 0xN358)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
PMON_CP-Bit_Error_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	PMON_CP-Bit Error_Count_Upper Byte[7:0]	RUR	Performance Monitor – CP Bit Error Count – Upper Byte:
		in the second se	These RESET-upon-READ bits, along with that within the "PMON CP-Bit Error Count Register – LSB" combine to reflect the cumulative number of CP bit errors that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Most Significant byte of this 16-bit expression. Note: These register bits are not active if the Primary Frame Synchronizer block has been bypassed, or if the Frame Synchronizer has not been configured to operate in the DS3 C-Bit Parity Framing format.

Table 675: PMON CP-Bit Error Count Register LSB (Address Location= 0xN359)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		PMON_	_CP-Bit_Error (ount_Lower_B	yte[7:0]		
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	8	0	0	0	0

BIT NUMBER	NAME O	Түре	DESCRIPTION
7 - 0	PMON_CP-Bit Error_Count_Lower Byte[7:0]	RUR	Performance Monitor – CP Bit Error Count – Lower Byte:
	The date of the		These RESET-upon-READ bits, along with that within the "PMON CP-Bit Error Count Register – MSB" combine to reflect the cumulative number of CP bit errors that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Least Significant byte of this 16-bit expression.
			Note: These register bits are not active if the Primary Frame Synchronizer block has been bypassed, or if the Frame Synchronizer has not been configured to operate in the DS3 C-Bit Parity Framing Format.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 676: PMON PLCP BIP-8 Error Count Register - MSB (Address Location= 0xN35A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
PMON_BIP-8_Error_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	PMON_BIP-8_ Error_Count_Upper_Byte[7:0]	RUR	Performance Monitor – BIP-8 Error Count – Upper Byte:
			This "Reset-upon-Read" register, along with the "PMON BIP-8 Error Count Register - LSB" (Address = N35B) contains a 16-bit representation of the total number of BIP-8 Errors (in the incoming B1 byte) that have been detected by the Receive PLCP Processor, since the last read of these registers. This register contains the MSB (or Upper Byte) value of this 16 bit expression. Note: These register bits are not active if the Primary Frame Synchronizer block has been bypassed.

Table 677: PMON PLCP BIP-8 Error Count Register LSB (Address Location= 0xN35B)

			The second secon				
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
PMON_BIP-8_Error_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0 0	0	0	0	0

BIT NUMBER	NAME NAME	TYPE	DESCRIPTION
7 - 0	PMON_BIP-8_ Error_Count_Lower_Byte[7:0]	RUR	Performance Monitor – BIP-8 Error Count – Lower Byte:
	The bata and may		This "Reset-upon-Read" register, along with the "PMON BIP-8 Error Count Register - MSB" (Address = N35A) contains a 16-bit representation of the total number of BIP-8 Errors (in the incoming B1 byte) that have been detected by the Receive PLCP Processor, since the last read of these registers. This register contains the LSB (or Lower Byte) value of this 16 bit expression.
			Note: These register bits are not active if the Primary Frame Synchronizer block has been bypassed.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 678: PMON PLCP Framing Byte Error Count Register – MSB (Address Location= 0xN35C)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
PMON_Framing_Byte_Error_Count_Upper_Byte[7:0]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	PMON_Framing Byte_ Error_Count_Upper_Byte[7:0]	RUR	Performance Monitor – Framing Byte Error Count – Upper Byte:
			This "Reset-upon-Read" register, along with the "PMON Framing Byte Error Count Register - LSB" (Address = 0xN35D) contains a 16-bit representation of the total number of Framing Byte Errors (in the incoming A1 and A2 bytes) that have been detected by the Receive PLCP Processor, since the last read of these registers. This register contains the MSB (or Upper Byte) value of this 16 bit expression. Note: These register bits are not active if the Primary Frame Synchronizer block has been bypassed.

Table 679: PMON PLCP Framing Byte Error Count Register - LSB (Address Location= 0xN35D)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0
	PMON_Framing_Byte_Error_Count_Lower_Byte[7:0]						
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0 0	100	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	PMON_Framing Byte_ Error_Count_Lower_Byte[7:0]	RUR	Performance Monitor – Framing Byte Error Count – Lower Byte:
	The data and mo		This "Reset-upon-Read" register, along with the "PMON Framing Byte Error Count Register - MSB" (Address = 0xN35C) contains a 16-bit representation of the total number of Framing Byte Errors (in the incoming A1 and A2 bytes) that have been detected by the Receive PLCP Processor, since the last read of these registers. This register contains the LSB (or Lower Byte) value of this 16 bit expression.
			Note: These register bits are not active if the Primary Frame Synchronizer block has been bypassed.

EXAR Experience Our Connectivit

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 680: PMON PLCP FEBE Event Count Register – MSB (Address Location= 0xN35E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
PMON_PLCP_FEBE_Event_Count_Upper_Byte[7:0]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR	
0	0	0	0	0	0	0	0	

BIT NUMBER	Nаме	Түре	DESCRIPTION
7 - 0	PMON_PLCP_FEBE_Event_ Count_Upper_Byte[7:0]	RUR	Performance Monitor –PCLP FEBE Event Count – Upper Byte:
			This "Reset-upon-Read" register, along with the "PMON PLCP FEBE Event Count Register - LSB" (Address = 0xN35F) contains a 16-bit representation of the total of data within the FEBE field of the G1 Byte, that have been read by the Receive PLCP Processor, since the last read of these registers. This register contains the MSB (or Upper byte) value of this 16-bit expression. Note: These register bits are not active if the Primary Frame Synchronizer block has been by-passed.

Table 681: PMON PLCP FEBE Event Count Register - LSB (Address Location= 0xN35F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 2	Віт 1	Віт 0	
PMON_PLCP_FEBE_Event_Count_Lower_Byte[7:0]							
RUR	RUR	RUR	RUR RUR	RUR	RUR	RUR	
0	0	0	0 0 0	0	0	0	

BIT NUMBER	NAME TYPE	DESCRIPTION
7 - 0	PMON_PLCP_FEBE_Event_ Count_Lower_Byte[7:0]	Performance Monitor –PCLP FEBE Event Count – Lower Byte: This "Reset-upon-Read" register, along with the "PMON PLCP FEBE Event Count Register - MSB" (Address = 0xN35E) contains a 16-bit representation of the total of data within the FEBE field of the G1 Byte, that have been read by the Receive PLCP Processor, since the last read of these registers. This register contains the LSB (or Lower byte) value of this 16-bit expression. Note: These register bits are not active if the Primary Frame Synchronizer block has been by-passed.



Table 682: PRBS Error Count Register – MSB (Address Location= 0xN368)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	PRBS_Error_Count_Upper_Byte[7:0]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	PRBS Error_Count_Upper Byte[7:0]	RUR	PRBS Error Count – Upper Byte:
			These RESET-upon-READ bits, along with that within the "PRBS Error Count Register – LSB" combine to reflect the cumulative number of PRBS bit errors that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Most Significant byte of this 16-bit expression. Note: These register bits are not active if the Primary Frame Synchronizer block has been bypassed, and if the PRBS Receiver has not been enabled.

Table 683: PRBS Error Count Register – LSB (Address Location= 0xN369)

Віт 7	Віт 6	Віт 5	Віт4	Віт 3	Віт 2	Віт 1	Віт 0		
	PRBS_Error_Count_Lower_Byte[7:0]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		
0	0	0	700	0	0	0	0		

)	T
BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	PRBS Error_Count_Lower Byte[7:0]	RUR	PRBS Error Count – Lower Byte:
	the data and may !		These RESET-upon-READ bits, along with that within the "PRBS Error Count Register – MSB" combine to reflect the cumulative number of PRBS bit errors that have been detected by the Primary Frame Synchronizer block, since the last read of this register. This register contains the Least Significant byte of this 16-bit expression.
			Note: These register bits are not active if the Primary Frame Synchronizer block has been bypassed, and if the PRBS Receiver has not been enabled.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 684: PMON Holding Register (Address Location= 0xN3, 0x6C; Address Location= 0xN36C)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
PMON_Hold_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	PMON Holding Value	R/O	PMON Holding Value: These READ-ONLY bit-fields were specifically allocated to support READ operations to the PMON (Performance Monitor) Registers, within the DS3/E3 Framer blocks.
			Since the PMON Register (within the DS3/E3 Framer block) are 16-bit registers. Therefore, given that the bi-directional data bus of the XRT94L33 is only 8-bits wide, it will require two read operations in order to read out the entire 16 bit content of these registers.
			The other thing to note is that the PMON Registers (within the DS3/E3 Framer blocks) are RESET-upon-READ type registers. As consequence, the entire 16-bit contents of a given PMON Register will be cleared to "0x0000" immediately after the user has executed the first (of two) read operations to this register. In order to avoid losing the contents of the other byte, the contents of the "un-read" byte is automatically loaded into this register.
			Hence, once the user reads a register, from a given PMON Register, he/she is suppose to obtain the contents of the other byte, by reading the contents of this register.
	e prod	juct of	Hence, once the user reads a register, from a given PMON Register, he/she is suppose to obtain the contents of the other byte, by reading the contents of this register.
	The data	da	

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 685: One Second Error Status Register (Address Location= 0xN36D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Unu	Errored Second	Severe Errored Second			
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 2	Unused	R/O	
1	Errored Second	R/O	Errored Second Indicator:
			This READ-ONLY bit-field indicates whether or not the DS3/E3 Framer block has declared the last one-second accumulation period as a "Errored Second".
			The DS3/E3 Framer block will declare a "errored second" if it detects any of the following events.
			For DS3 Applications
			P-Bit Errors
			CP Bit Errors
			Framing Bit (F or M bit) Errors
			For E3 Applications
			BIP-4/BIP-8 Errors
			FAS or Framing Byte (FA1, FA2) Errors
			0 + Indicates that the DS3/E3 Framer block has NOT declared the last one-second accumulation period as being an errored second.
		× (c	1 – Indicates that the DS3/E3 Framer block has declared the last one-second accumulation period as being an errored second.
	5	JC C	Note: This bit-field is only active if the Primary Frame Synchronizer block is enabled.
0	Severely Errored	R/O	Severely Errored Second Indicator:
	Second P	qua	This READ-ONLY bit-field indicates whether or not the DS3/E3 Framer block has declared the last one second accumulation period as being a "Severely Errored Second".
	· ·		The DS3/E3 Framer block will declare a given second as being a "severely errored" second if it determines that the BER (Bit Error Rate) during this "one-second accumulation" period is greater than 10 ⁻³ errors/second.
			0 – Indicates that the DS3/E3 Framer block has not declared the last one-second accumulation period as being a "severely-errored" second.
			1 – Indicates that the DS3/E3 Framer block has declared the last one-second accumulation period as being a "severely-errored" second.
			Note: This bit-field is only active if the Primary Frame Synchronizer block is enabled.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 686: One Second – LCV Count Accumulator Register – MSB (Address Location= 0xN36E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	One_Second_LCV_Count_Accum_MSB[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	TYPE	DESCRIPTION
7 - 0	One_Second_LCV_Count Accum_LSB[7:0]	R/O	One Second LCV Count Accumulator Register – MSB: These READ-ONLY bits, along with that within the "One Second LCV Count Accumulator Register – MSB" combine to reflect the cumulative number of "Line Code Violations" that have been detected by the Frame Synchronizer block, in the last "one second" accumulation period. This register contains the Most Significant byte of this 16-bit expression.

Table 687: One Second – LCV Count Accumulator Register (SB (Address Location= 0xN36F)

					VO.		
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		One_S	Second_LCV_C	ount_Accum_LS	B[7:0]		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	5, 000	0	0	0

			7 A 7 A 7
BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	One_Second_LCV_Count Accum_LSB[7:0]	ale l	One Second LCV Count Accumulator Register – LSB: These READ-ONLY bits, along with that within the "One Second LCV Count Accumulator Register – LSB" combine to reflect the cumulative number of "Line Code Violations" that have been detected by the Frame Synchronizer block, in the last "one second" accumulation period. This register contains the Least Significant byte of this 16-bit expression.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 688: One Second - Parity Error Accumulator Register - MSB (Address Location= 0xN370)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
One_Second_Parity_Error_Accum_MSB[7:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	One_Second_Parity Error Accum_MSB[7:0]	R/O	One Second Parity Error Accumulator Register – MSB:
			These READ-ONLY bits, along with that within the "One Second Parity Error Accumulator Register – LSB" combine to reflect the cumulative number of "Parity Errors" that have been detected by the Frame Synchronizer block, in the last "one second" accumulation period. This register contains the Most Significant byte of this 16-bit expression.
			Note: For DS3 applications, the register will reflect the number of P-bit errors, detected within the last "one second" accumulation period.
			For E3, ITU-T G.751 applications, this register will reflect the number of BIP-4 errors, detected within the last "one second" accumulation period.
		du	For E3 ITU-T G.832 applications, this register will reflect the number of BIP-8 (B1 Byte) errors detected within the last "one second" accumulation period.
	The product (of	pro line be	ordere

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 689: One Second – Parity Error Accumulator Register – LSB (Address Location= 0xN371)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	One_Second_Parity_Error_Accum_LSB[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	One_Second_Parity Error	R/O	One Second Parity Error Accumulator Register – LSB:
	Accum_LSB[7:0]		These READ-ONLY bits, along with that within the "One Second Parity Error Accumulator Register – MSB" combine to reflect the cumulative number of "Parity Errors" that have been detected by the Frame Synchronizer block, in the last "one second" accumulation period. This register contains the Least Significant byte of this 16-bit expression.
			Note:
			For DS3 applications, the register will reflect the number of P-bit errors, detected within the last "one second" accumulation period.
			For E3, ITUT G.751 applications, this register will reflect the number of BIP-4 errors, detected within the last "one second" accumulation period
			For E3, ITUT G.832 applications, this register will reflect the number of BIP-8 (B1 Byte) errors detected within the last "one second" accumulation period.
	duct	Cator	to ordere
	The product	naynu	

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 690: One Second – CP Bit Error Accumulator Register – MSB (Address Location= 0xN372)

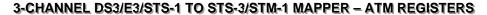
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	One_Second_CP_Bit_Error_Accum_MSB[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	One_Second_CP Bit Error Accum_MSB[7:0]	R/O	One Second CP Bit Error Accumulator Register – MSB: These READ-ONLY bits, along with that within the "One Second CP-Bit Error Accumulator Register – LSB" combine to reflect the cumulative number of "CP Bit Errors" that have been detected by the Frame Synchronizer block, in the last "one second" accumulation period. This register contains the Most Significant byte of this 16-bit expression. Note: This register is inactive if the Frame Synchronizer block is "by-passed" or if the Frame Synchronizer block has not been configured to operate in the DS3, C-Bit Parity framing format.

Table 691: One Second – CP Bit Error Accumulator Register LSB (Address Location= 0xN373)

Віт 7	Віт 6	Віт 5	Віт 4	Віт3	Віт 2	Віт 1	Віт 0
		One_S	econd_CP_Bit2	Error_Accum_L	SB[7:0]		
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	9, 00,0	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	One_Second_CP Bit Error Accum_LSB[7:0]	RO	One Second CP Bit Error Accumulator Register – LSB: These READ-ONLY bits, along with that within the "One Second CP-Bit Error Accumulator Register – MSB" combine to reflect the cumulative number of "CP Bit Errors" that have been detected by the Frame Synchronizer block, in the last "one second" accumulation period. This register contains the Least Significant byte of this 16-bit expression. Note: This register is inactive if the Frame Synchronizer block is "by-passed" or if the Frame Synchronizer block has not been configured to operate in the DS3, C-Bit Parity framing format.





1.12.11 GENERAL PURPOSE I/O PIN CONTROL REGISTERS

Table 692: Line Interface Drive Register (Address Location= 0xN380)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Internal Remote Loop-back				Unused			
R/W	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	1	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Internal Remote Loop-	R/W	Internal Remote Loop-back Mode:
	back		This READ/WRITE bit-field permits the user to configure the DS3/E3 Framer block to operate in the "Remote Loop-back" Mode.
			If the user enables this feature, then the Receive Input of the Primary Frame Synchronizer block will automatically be routed to the Transmit Output of the Frame Generator block.
			0 - Disables the Remote Loop-back Mode.
			1 – Enables the Remote Loop-back Mode.
			Note: This feature is only available if both the Frame Generator and the Primary Frame Synchronizer blocks are enabled.
6 - 0	Unused	R/O	31 30 9
	The production of the producti	inest n	ot be ordered to

1.12.12 LAPD CONTROLLER BYTE COUNT REGISTERS

Table 693: TxLAPD Byte Count Register (Address Location= 0xN383)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	TxLAPD_MESSAGE_SIZE[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	TxLAPD_MESSAGE_SIZE[7:0]	R/W	Transmit LAPD Message Size: These READ/WRITE bit-fields permit the user to specify the size of the information payload (in terms of bytes) within the very next outbound LAPD/PMDL Message, whenever Bit 7 (TxLAPD Any) within the "Transmit Tx LAPD Configuration" Register has been set to "1".

Table 694: RxLAPD Byte Count Register (Address Location = 0xN384)

Віт 7	Віт 6	Віт 5	Віт 4	Bit 3	Віт 2	Віт 1	Віт 0			
	RxLAPD_MESSAGE_SIZE[7:0]									
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O			
0	0	0	0 %	000	0	0	0			

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	RxLAPD_MESSAGE_SIZE[7:	pj R/O	Receive LAPD Message Size:
	The product at	O	These READ-ONLY bit-fields indicate the size of the most recently received LAPD/PMDL Message, whenever Bit 7 (RxLAPD Any) within the "Rx LAPD Control" Register; has been set to "1". The contents of these register bits, reflects the Received LAPD Message size, in terms of bytes.



Rev 2.0.0

Table 695: Receive PLCP Configuration and Status Register (Address Location= 0xN390)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unu	sed	Nibble Boundary Shift	Speed Count	Reframe	POOF Status	PLOF Status	Yellow Status
R/O	R/O	R/W	R/W	R/W	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	Description
7 – 6	Unused	R/O	
5	Nibble Boundary Shift	R/W	.5 8
4	Speed Count	R/W	th ire
3	Reframe	R/W	Receive PLCP Processor Reframe Operation: This "Read/Write" bit-field allows the user to command the Receive PLCP Processor to perform a "Reframe" operation of the user invokes this command, the Receive PLCP Processor will transition from the "In-Frame" state to the "Loss-of-Frame" state. Afterwards, it will attempt to reacquire framing. 1 – The Receive PLCP Processor will perform a "reframe: operation O – The Receive PLCP Processor will NOT perform a "Reframe" operation
2	POOF Status	R/O	POOF (Receive PLCP Processor Out-of-Frame) Status: This "Read-Only" bit-field indicates whether or not the Receive PLCP Processor is in the "Out-of-Frame (OOF)" condition or not. 0 — Receive PLCP Processor is either in the "In-Frame" condition or in the "Loss-of-Frame" condition. 1 — Receive PLCP is currently in the "OOF Condition".
1	PLOF Status	R/O	PLOP (Receive PLCP Processor Loss of Frame) Status: This "Read-Only" bit-field indicates whether or not the Receive PLCP Processor is in the "Loss of Frame (LOF) condition or not. PLCP Loss of Frame is declared if PLCP Out-of-Frame (POOF), in bit 2 of this register, is declared for more than 1ms. PLOF is deasserted if POOF is off for more than 12 ms. 0 - Receive PLCP Processor is either in the "In-Frame" condition or in the "Out-of-Frame" condition. 1 - Receive PLCP Processor is currently in the "LOF Condition".
0	Yellow Status	R/O	Yellow Status: This "Read-Only" bit field indicates whether or not the Receive PLCP Processor has detected a prolonged "Yellow Alarm" indication in the G1 bytes of the incoming PLCP frames.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

If a "Far-End" Receive PLCP Processor has trouble receiving valid PLCP data from the "Near-End" Transmit PLCP Processor, it (the Far End Transmit PLCP Processor) will begin to transmit PLCP frames that contain G1 bytes with the asserted "Yellow Alarm - RAI" indicators. If the "Near-End" Receive PLCP Processor determines that it has been receiving PLCP frames with these kind of G1 bytes for a 10 or more consecutive frames; then the Receive PLCP Processor will set this bit-field to "1".
1 – Indicates 10 or more consecutive frames received contain Yellow Alarm Indicators in G1 bytes.
0 – Indicates 10 or more consecutive frames received without Yellow Alarm Indicators in G1 bytes.

Table 696: Receive PLCP Interrupt Enable Register (Address Location= 0xN391)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused			aned h	Jia	POOF Interrupt Enable	PLOF Interrupt Enable	
R/O	R/O	R/O	R/O	R/O	R/O	R/W	R/W
0	0	0	0	0	0	0	0

		-6	
BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 2	Unused)R/O	
1	POOF Interrupt Enable	R/W	POOF Interrupt Enable:
	iot Pro	19,	This "Read-Write" bit-field allows the user to enable or disable the "Change in POOF Condition" interrupt.
		© O	0 – Disables PLCP Out-of-Frame (OOF) interrupt condition
	All tains		1 – Enables PLCP Out-of-Frame (OOF) interrupt condition
0	PLOF Interrupt Enable	R/W	PLOF Interrupt Enable:
	ne prostrati		This "Read-Write" bit-field allows the user to enable or disable the "Change in PLOF Condition" interrupt.
	1, gard		0 – Disables PLCP Loss-of-Frame (LOF) interrupt condition
	&		1 – Enables PLCP Loss-of-Frame (LOF) interrupt condition



Rev 2.0.0

Table 697: Receive PLCP Interrupt Status Register (Address Location= 0xN392)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused							PLOF Interrupt Status
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 2	Unused	R/O	
1	POOF Interrupt Status	R/W	POOF Interrupt Status:
			This "Read-Only" bit-field indicates whether a "Change in POOF (Receive PLCP Processor Out of Frame) condition interrupt has been generated since the last read of this register.
			If this bit-field is "0", then the "Change in POOF Condition interrupt has not occurred since the last read of this register However, if this bit-field is "1", then the "Change in POOI Condition" interrupt has occurred since the last read of this register.
			This bit-field will be asserted under the following two conditions:
		. \$	10 The Receive PLCP Processor transitions from the "In Frame" or "Loss of Frame" condition to the "Out of Frame condition.
		Col	2. The Receive PLCP Processor transitions from the "Out of-Frame" condition to the "In-Frame" condition.
	orodi	66, 4	The local μP can read the "Rx PLCP Configuration/Status Register (Address = 0xN390), in order to determine the current "POOF" status.condition
0	PLOF Interrupt Status	R/W	PLOF Interrupt Status:
	The date		This "Read Only" bit-field indicates whether a "Change in PLOF (Receive PLCP Processor Loss of Frame) condition interrupt has been generated since the last read of this register.
			If this bit-field is "0", then the "Change in PLOF Condition interrupt has not occurred since the last read of this register However, if this bit-field is "1", then the "Change in PLOI Condition" interrupt has occurred since the last read of this register.
			This bit-field will be asserted under the following two conditions:
			The Receive PLCP Processor transitions from the "In Frame" condition to the "Loss of Frame" condition.
			2. The Receive PLCP Processor transitions from the "Los of Frame" or "Out of Frame" condition to the "In-Frame





3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

	condition.
	The local μP can read the "Rx PLCP Configuration/Status" Register (Address = 0xN390), in order to determine the current "PLOF" status.

The product of products mentioned in this red to longered (OBS)

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 698: Transmit PLCP A1 Byte Error Mask Register (Address Location= 0xN398)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	A1_Byte_Error_Mask [7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/w	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	A1_Byte_Error_Mask [7:0]	R/W	A1_Byte_Error_Mask [7:0]:
			This register allows the user to insert errors into the A1 Byte of each outgoing PLCP Frame. The Transmit PLCP Processor automatically performs the XOR operation on the A1 byte of every outbound PLCP frame with the contents of this register. Therefore, if this register contains any "15", then errors will be inserted into the A1 byte. If the user wishes to operate the Transmit PLCP in a normal mode (e.g., by NOT inserting errors into the A1 byte), then he/she must insure that this register contains the default value, 00h.

Table 699: Transmit PLCP A2 Byte Error Mask Register (Address Location= 0xN399)

					_		
Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			A2_Byte_Em	or_Mask [7:0]			
R/W	R/W	R/W	R/W	⊘R/W	R/W	R/w	R/W
0	0	0	0,0		0	0	0

bic 10 dele							
BIT NUMBER	NAME	TYPE	DESCRIPTION				
7 – 0	A2_Byte_Error_Mask [7:0]	RW	A2 Byte_Error_Mask [7:0]: This register allows the user to insert errors into the A2 Byte of each outgoing PLCP Frame. The Transmit PLCP Processor automatically performs the XOR operation on the A2 byte of every outbound PLCP frame with the contents of this register. Therefore, if this register contains any "1s", then errors will be inserted into the A2 byte. If the user wishes to operate the Transmit PLCP in a normal mode (e.g., by NOT inserting errors into the A2 byte), then he/she must insure that this register contains the default value, 00h.				

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 700: Transmit PLCP B1 Byte (BIP-8) Error Mask Register (Address Location= 0xN39A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	B1_Byte_Error_Mask [7:0]								
R/W	R/W	R/W	R/W	R/W	R/W	R/w	R/W		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	B1_Byte_Error_Mask	R/W	B1_Byte_Error_Mask [7:0]:
	[7:0]		This register allows the user to insert errors into the B1 Byte of each outgoing PLCP Frame. The Transmit PLCP Processor automatically performs the XOR operation on the B1 byte of every outbound PLCP frame with the contents of this register. Therefore, if this register contains any "1s", then errors will be inserted into the B1 byte. If the user wishes to operate the Transmit PLCP in a normal mode (e.g., by NOT inserting errors into the B1 byte), then he/she must insure that this register contains the default value, 00h.
	The production of the data and	t of a land	Roducts Inention manufactoring in the condered (OBS) and the ordered (OBS)

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 701: Transmit PLCP G1 Byte Register (Address Location= 0xN39B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused		Tx FEBE Mask					
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION			
7 - 5	Unused	R/O				
4	Tx FEBE Mask	R/W	Tx FEBE Mask:			
			This "Read/Write" bit-field allows the user to command the Transmit PLCP Processor to insert a value of "0000" into the FEBE field of the G1 byte in the outbound PLCP Frame.			
			1 – Transmit FEBE count with the value of "0000" overwritten by the Transmit PLCP Processor			
			0 – Transmit Received FEBE count			
3	Yellow Alarm	R/W	Yellow Alarm:			
			This "Read/Write" bit field allows the user to command the Transmit PLCP to send a "Yellow Alarm" via the G1 byte (within the outbound PLCP frame) to the far-end Receive PLCP Processor.			
			1 – The Transmit PLCP will orce the "RAI" bit (Yellow Alarm), within the G1 byte, to "1" 0 – "RAI" bit (Yellow Alarm) will NOT be forced.			
2-0	LSS [2:0]	R/W	LSS (Link Status Signal) 2:0]:			
- v			This "Read/Mrite" hit-fields allows the user to transmit their own			
"proprietary" data link messages, via the 3 unused bits within the G1 bytes, of each outbound PLCP frame.						

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 702: Receive DS3/E3 Configuration Register – Secondary Frame Synchronizer (Address Location= 0xN3F0)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused		Primary Frame - Clock Output Invert Primary Frame - Transmit AIS Enable		Secondary Frame – Single-Rail Input	Primary Frame - Dual- Rail Output	Primary Frame – Idle Pattern Insert
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Віт	NAME	Түре	DESCRIPTION
Number			.6 \
7 - 5	Unused	R/O	"HIS LEEP
4	Primary Frame – Clock Output Invert	R/W	Primary Frame Synchronizer - Clock Output Invert:
	Clock Gulput IIIveit		This READ/WRITE bit-field permits the user to configure the Primary Frame Synchronizer block to update the "DS3/E3/STS1_DATA_OUT_n" output pins upon either the rising or falling edge of "DS3/E3/STS1_CLK_OUT_n.
			0 - DS3/E3/STS1_DATA_OUT_n is updated upon the rising edge of "DS3/E3/STS1_CIk_OUT_n". The user should insure that the LIU IC will sample "DS3/E3/STS1_DATA_OUT_n" upon the falling edge of "DS3/E3/STS1_CLK_OUT_n"
			1 – DS3/E3/STS1_DATA_OUT_n" is updated upon the falling edge of "DS3/E3/STS1_Clk_OUT_n". The user should insure that the LIU IC will sample "DS3/E3/STS1_DATA_OUT_n" upon the rising edge of "DS3/E3/STS1_CLK_OUT_n".
			Note: This bit-field is only active if the "Primary Frame Synchronizer" block has been configured to operate in the "Egress" Direction.
3	Primary Frame – Transmit AIS	R/W	Primary Frame Synchronizer Block – Transmit AIS Enable:
		JUC'S	This READ/WRITE bit-field permits the user to either enable or disable the AIS Pattern Generator, within the Primary Frame Synchronizer block
	Enable	SHOO	In the user enables the "AIS Pattern Generator", then the data, that is output via the Primary Frame Synchronizer block, will be overwritten with the AIS Pattern.
	11,93f	9	0 –Disables the "AIS Pattern Generator" within the Primary Frame Synchronizer block.
	•		1 – Enables the "AIS Pattern Generator" within the Primary Frame Synchronizer block.
2	Secondary Frame – Single-Rail Input	R/W	Secondary Frame Synchronizer Block -Single-Rail/Dual Rail Input Select:
			This READ/WRITE bit-field permits the user to configure the Secondary Frame Synchronizer block to accept data via either the "Single-Rail" or "Dual-Rail" manner.
			0 – Configures the Secondary Frame Synchronizer block to accept data via the "Single-Rail" Mode.
			1 – Configures the Secondary Frame Synchronizer block to accept data via the "Dual-Rail" Mode.
			Note: This register bit is only valid if the Secondary Frame Synchronizer block has been configured to operate in the "Ingress" Direction.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

1	Primary Frame –	R/W	Primary Frame Synchronizer – Dual-Rail Output:
	Dual-Rail Output		This READ/WRITE bit-field permits the user configure the Primary Frame Synchronizer block to output data (to the LIU IC) in either the Single-Rail or Dual-Rail Manner.
			0 – Configures the Primary Frame Synchronizer block to output data (to the LIU IC) in a Single-Rail Manner.
			1 – Configures the Primary Frame Synchronizer block to output data (to the LIU IC) in a Dual-Rail Manner.
			Note: This register bit is only valid if the Primary Frame Synchronizer block has been configured to operate in the "Egress" Direction.
0	Primary Frame –	R/O	Primary Frame Synchronizer Block – Idle Pattern Insert:
	Idle Pattern Insert		This READ/WRITE bit-field permits the user to either enable or disable the Idle Pattern Generator, within the Primary Frame Synchronizer block
			If the user enables the "Idle Pattern Generator", then the data, that is output via the Primary Frame Synchronizer block will be overwritten with the Idle Pattern.
			0 –Disables the "Idle Pattern Generator" within the Primary Frame Synchronizer block.
			1 – Enables the "Idle Pattern Generator" within the Primary Frame Synchronizer block.
	The	ata and	1 - Enables the "Idle Pattern Generator" within the Primary Frame Synchronizer block.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 703: Receive DS3/E3 Status Register – Secondary Frame Synchronizer (Address Location= 0xN3F1)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Secondary Frame Synchronizer - AIS Defect Declared	Secondary Frame Synchronizer – LOS Defect Declared	Secondary Frame Synchronizer – DS3 Idle Pattern Detected	Secondary Frame Synchronizer – OOF Defect Declared		Unu	ised	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	1	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7	Secondary Frame Synchronizer – AIS Defect Declared	R/O	Secondary Frame Synchronizer Block AIS Defect Declared: This READ/WRITE bit-field indicates whether or not the Secondary Frame Synchronizer block is currently declaring the AIS condition. 0 — Indicates that the Secondary Frame Synchronizer block is NOT declaring the AIS defect. 1 — Indicates that the Secondary Frame Synchronizer block is currently declaring the AIS defect.
6	Secondary Frame Synchronizer – LOS Defect Declared	R/O	Secondary Frame Synchronizer Block – LOS Defect Declared: This READ/WRITE bit-field indicates whether or not the Secondary Frame Synchronizer block is currently declaring the LOS condition. 0 — Indicates that the Secondary Frame Synchronizer block is NOT declaring the LOS defect. 1— Indicates that the Secondary Frame Synchronizer block is currently declaring the LOS defect.
5	Secondary Frame Synchronizer – Idle Pattern Detected	RO	Secondary Frame Synchronizer Block – Idle Pattern Detected: This READ/WRITE bit-field indicates whether or not the Secondary Frame Synchronizer block is currently detecting the DS3 Idle Pattern, within its incoming Receive Path. O – Indicates that the Secondary Frame Synchronizer block is NOT detecting the DS3 Idle Pattern. 1 – Indicates that the Secondary Frame Synchronizer block is currently detecting the DS3 Idle Pattern. Note: This bit-field is only valid if the DS3/E3 Frame Synchronizer block has been configured to operate in the DS3 Mode.
4	Secondary Frame Synchronizer – OOF Defect Declared	R/O	Secondary Frame Synchronizer Block – OOF Defect Declared: This READ/WRITE bit-field indicates whether or not the Secondary Frame Synchronizer block is currently declaring the OOF condition. 0 — Indicates that the Secondary Frame Synchronizer block is NOT declaring the OOF defect. 1 — Indicates that the Secondary Frame Synchronizer block is currently declaring the OOF defect.
3 – 0	Unused	R/O	



Rev 2.0.0

Table 704: Receive DS3/E3 Interrupt Enable Register – Secondary Frame Synchronizer Block (Address Location= 0xN3F8)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Change of LOS Condition Interrupt Enable	Change of AIS Condition Interrupt Enable	Change of DS3 Idle Condition Interrupt Enable	Unused		Change of OOF Condition Interrupt Enable	Unused
R/O	R/W	R/W	R/W	R/O	R/O	R/W	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	Description
7	Unused	R/O	"His reo
6	Change of LOS	R/W	Change of LOS Condition Interrupt Enable:
	Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of LOS Condition" Interrupt for the Secondary Frame Synchronizer block.
			If the user enables this interrupt, then the Secondary Frame Synchronizer block will generate an interrupt in response to either of the following conditions.
			Whenever the Secondary Frame Synchronizer block declares the LOS defect.
			Whenever the Secondary Frame Synchronizer block clears the LOS defect.
			0 Disables the "Change of LOS Condition" Interrupt.
		. (1 - Enables the "Change of LOS Condition" Interrupt.
5	Change of AIS	R/W	Change of AIS Condition Interrupt Enable:
	Condition Interrupt Enable	duce	This READ/WRITE bit-field permits the user to either enable or disable the "Change of AIS Condition" Interrupt for the Secondary Frame Synchronizer block.
	Change of AIS Condition Interrupt Enable	Shus	If the user enables this interrupt, then the Secondary Frame Synchronizer block will generate an interrupt in response to either of the following conditions.
	. 00	and	Whenever the Secondary Frame Synchronizer block declares the AIS defect.
			Whenever the Secondary Frame Synchronizer block clears the AIS defect.
			0 - Disables the "Change of AIS Condition" Interrupt.
			1 – Enables the "Change of AIS Condition" Interrupt.
4	Change in DS3 Idle	R/W	Change of DS3 Idle Condition Interrupt Enable:
	Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of DS3 Idle Condition" Interrupt for the Secondary Frame Synchronizer block.
			If the user enables this interrupt, then the Secondary Frame Synchronizer block will generate an interrupt in response to either of the following conditions.
			Whenever the Secondary Frame Synchronizer block detects the DS3

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

		Idle pattern within its receive path.
		Whenever the Secondary Frame Synchronizer block ceases to detect the DS3 Idle pattern within its receive path.
		0 – Disables the "Change of DS3 Idle Condition" Interrupt.
		1 – Enables the "Change of DS3 Idle Condition" Interrupt.
		Note: This bit-field is only active if the DS3/E3 Framer block has been configured to operate in the DS3 Mode.
Unused	R/O	
Change of OOF	R/W	Change of OOF Condition Interrupt Enable:
Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of OOF Condition" Interrupt for the Secondary Frame Synchronizer block.
		If the user enables this interrupt, then the Secondary Frame Synchronizer block will generate an interrupt in response to either of the following conditions.
		Whenever the Secondary Frame Synchronizer block declares the OOF defect.
		Whenever the Secondary Frame Synchronizer block clears the OOF defect.
		0 – Disables the "Change of OOF Condition" Interrupt.
		1 – Enables the "Change of OOF Condition" Interrupt.
Unused	R/O	incres (Or
The production of the data and	ct of a last of the last of th	and long red so the long red s
	Change of OOF Condition Interrupt Enable	Change of OOF R/W Condition Interrupt

Rev 2.0.0

Table 705: Receive DS3/E3 Interrupt Status Register – Secondary Frame Synchronizer Block (Address Location= 0xN3F9)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Change of LOS Condition Interrupt Status	Change of AIS Condition Interrupt Status	Change of DS3 Idle Condition Interrupt Status	Unu	ised	Change of OOF Condition Interrupt Status	Unused
R/O	RUR	RUR	RUR	R/O	R/O	RUR	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Unused	R/O	"his red
6	Change of LOS Condition	RUR	Change of LOS Condition Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of LOS Condition" Interrupt (per the Secondary Frame Synchronizer block) has occurred since the last read of this register.
			0 – Indicates that the "Change of LOS Condition" Interrupt (per the Secondary Frame Synchronizer block) has NOT occurred since the last read of this register.
			1 – Indicates that the "Change of LOS Condition" Interrupt (per the Secondary Frame Synchronizer block) has occurred since the last read of this register.
		t or	Note: The user can determine the current state of "LOS" (per the Secondary Frame Synchronizer" block) by reading out the state of Bit 6 (Secondary Frame Synchronizer – LOS Defect Declared) within the Receive DS3/E3 Status Register – Secondary Frame Synchronizer block" register (Address Location= 0xN3F1).
5	Change of AIS Condition	RUR	Change of AIS Condition Interrupt Status:
	Change of AIS Condition Interrupt Status	May	This RESET-upon-READ bit-field indicates whether or not the "Change of AIS Condition" Interrupt (per the Secondary Frame Synchronizer block) has occurred since the last read of this register.
	deane		0 – Indicates that the "Change of AIS Condition" Interrupt (per the Secondary Frame Synchronizer block) has NOT occurred since the last read of this register.
			1 – Indicates that the "Change of AIS Condition" Interrupt (per the Secondary Frame Synchronizer block) has occurred since the last read of this register.
			Note: The user can determine the current state of "LOS" (per the Secondary Frame Synchronizer" block) by reading out the state of Bit 7 (Secondary Frame Synchronizer – AIS Defect Declared) within the Receive DS3/E3 Status Register – Secondary Frame Synchronizer block" register (Address Location= 0xN3F1).
4	Change of DS3 Idle	RUR	Change of DS3 Idle Condition Interrupt Status:
	Condition Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change of DS3 Idle Condition" Interrupt (per the Secondary Frame Synchronizer block) has occurred since the last read of this

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			register.
			0 – Indicates that the "Change of DS3 Idle Condition" Interrupt (per the Secondary Frame Synchronizer block) has NOT occurred since the last read of this register.
			1 – Indicates that the "Change of DS3 Idle Condition" Interrupt (per the Secondary Frame Synchronizer block) has occurred since the last read of this register.
			Note: The user can determine the current "DS3 Idle" state (per the Secondary Frame Synchronizer" block) by reading out the state of Bit 5 (Secondary Frame Synchronizer – DS3 Idle Pattern Detected) within the Receive DS3/E3 Status Register – Secondary Frame Synchronizer block" register (Address Location= 0xN3F1).
3 - 2	Unused	R/O	٠ ۵ ک
1	Change of OOF Condition	RUR	Change of OOF Condition Interrupt Status:
	Interrupt Status	of Production	This RESET-upon-READ bit-field indicates whether or not the "Change of OOF Condition" Interrupt (per the Secondary Frame Synchronizer block) has occurred since the last read of this register. 0 – Indicates that the "Change of OOF Condition" Interrupt (per the Secondary Frame Synchronizer block) has NOT occurred since the last read of this register. 1 – Indicates that the "Change of OOF Condition" Interrupt (per the Secondary Frame Synchronizer block) has occurred since the last read of this register. Note. The user can determine the current state of "LOS" (per the Secondary Frame Synchronizer" block) by reading out the state of Bit 4 (Secondary Frame Synchronizer – OOF Defect Declared) within the Receive DS3/E3 Status Register – Secondary Frame Synchronizer block" register (Address Location= 0xN3F1).
0	Unused	R/O	
	Unused Under the problem of the prob	No	



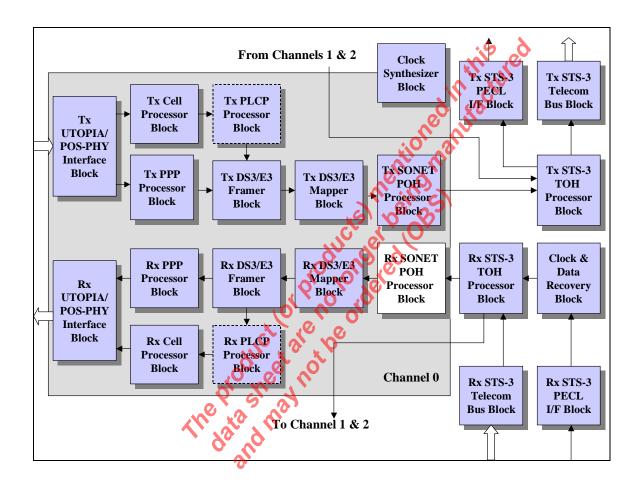
1.13 RECEIVE STS-3C POH PROCESSOR BLOCK

The register map for the Receive STS-3c POH Processor Block is presented in the Table below. Additionally, a detailed description of each of the "Receive STS-3c POH Processor" block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33, with the "Receive STS-3c POH Processor Block "highlighted" is presented below in

Figure 14.

Figure 14: Illustration of the Functional Block Diagram of the XRT94L33, with the Receive STS-3c POH Processor Block "High-lighted".





1.13.1 RECEIVE STS-3c POH PROCESSOR BLOCK REGISTER

Table 706: Receive STS-3c POH Processor Block - Register Address Map

INDIVIDUAL REGISTER ADDRESS	Address Location	REGISTER NAME	DEFAULT VALUES
0x00 – 0x81	0x1000 – 0x1181	Reserved	0x00
0x82	0x1182	Receive STS-3c Path – Control Register – Byte 1	0x00
0x83	0x1183	Receive STS-3c Path – Control Register – Byte 0	0x00
0x84, 0x85	0x1184, 0x1185	Reserved	0x00
0x86	0x1186	Receive STS-3c Path – Status Register – Byte 1	0x00
0x87	0x1187	Receive STS-3c Path – Status Register Byte 0	0x00
0x88	0x1188	Reserved	0x00
0x89	0x1189	Receive STS-3c Path – Interrupt Status Register – Byte 2	0x00
0x8A	0x118A	Receive STS-3c Path – Interrupt Status Register – Byte 1	0x00
0x8B	0x118B	Receive STS-3c Path - Interrupt Status Register - Byte 0	0x00
0x8C	0x118C	Reserved	0x00
0x8D	0x118D	Receive STS-3c Path Interrupt Enable Register – Byte 2	0x00
0x8E	0x118E	Receive STS-3c Path - Interrupt Enable Register - Byte 1	0x00
0x8F	0x118F	Receive STS-3c Path Interrupt Enable Register – Byte 0	0x00
0x90 - 0x92	0x1190 – 0x1192	Reserved &	0x00
0x93	0x1193	Receive STS-3c Path – SONET Receive RDI-P Register	0x00
0x94, 0x95	0x1194, 0x1195	Reserved	0x00
0x96	0x1196	Receive STS-3c Path – Received Path Label Byte (C2) Register	0x00
0x97	0x1197	Receive STS-3c Path – Expected Path Label Byte (C2) Register	0x00
0x98	0x1198	Receive STS-3c Path – B3 Error Count Register – Byte 3	0x00
0x99	0x1199	Receive STS-3c Path – B3 Error Count Register – Byte 2	0x00
0x9A	0x119A	Receive STS-3c Path – B3 Error Count Register – Byte 1	0x00
0x9B	0x119B	Receive STS-3c Path – B3 Error Count Register – Byte 0	0x00
0x9C	0x119C	Receive STS-3c Path – REI-P Error Count Register – Byte 3	0x00
0x9D	0x119D	Receive STS-3c Path – REI-P Error Count Register – Byte 2	0x00
0x9E	0x119E	Receive STS-3c Path – REI-P Error Count Register – Byte 1	0x00
0x9F	0x119F	Receive STS-3c Path – REI-P Error Count Register – Byte 0	0x00
0xA0 - 0xA2	0x11A0 -	Reserved	0x00

XRT94L33

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Individual Register Address	Address Location	REGISTER NAME	DEFAULT VALUES
	0x11A2		
0xA3	0x11A3	Receive STS-3c Path – Receive J1 Byte Control Register	0x00
0xA4, 0xA5	0x11A4, 0x11A5	Reserved	0x00
0xA6	0x11A6	Receive STS-3c Path – Pointer Value Register – Byte 1	0x00
0xA7	0x11A7	Receive STS-3c Path – Pointer Value Register – Byte 0	0x00
0xA8 – 0xAA	0x11A8 – 0x11AA	Reserved	0x00
0xAB	0x11AB	Receive STS-3c Path – Loss of Pointer – Concatenation Status Register	0x00
0xAC - 0xB2	0x11AC - 0x11B2	Reserved	0x00
0xB3	0x11B3	Receive STS-3c Path – AIS - Concatenation Status Register	0x00
0xB4 – 0xBA	0x11B4 – 0x11BA	Reserved	0x00
0xBB	0x11BB	Receive STS-3c Path – AUTO AIS Control Register	0x00
0xBC - 0xBE	0x11BC - 0x11BE	Reserved	0x00
0xBF	0x11BF	Receive STS-3c Path Serial Port Control Register	0x00
0xC0 - 0xC2	0x11C0 - 0x11C2	Reserved	0x00
0xC3	0x11C3	Receive STS-3c Path - SONET Receive Auto Alarm Register - Byte 0	0x00
0xC4 - 0xD2	0x11C4 – 0x11D2	Reserved	0x00
0xD3	0x11D3	Receive STS-3c Path – Receive J1 Byte Capture Register	0x00
0xD4 - 0xD6	0x11D4 – 0x11D6	Reserved	0x00
0xD7	0x11D7	Receive STS-3c Path – Receive B3 Byte Capture Register	0x00
0xD8 – 0xDA	0x11D8 – 0x11DA	Reserved	0x00
0xDB	0x11DB	Receive STS-3c Path – Receive C2 Byte Capture Register	0x00
0xDC - 0xDE	0x11DC - 0x11DE	Reserved	0x00
0xDF	0x11DF	Receive STS-3c Path – Receive G1 Byte Capture Register	0x00
0xE0 - 0xE2	0x11E0 – 0x11E2	Reserved	0x00
0xE3	0x11E3	Receive STS-3c Path – Receive F2 Byte Capture Register	0x00
0xE4 - 0xE6	0x11E4 – 0x11E6	Reserved	0x00
0xE7	0x11E7	Receive STS-3c Path – Receive H4 Byte Capture Register	0x00

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

INDIVIDUAL REGISTER ADDRESS	Address Location	REGISTER NAME	DEFAULT VALUES
0xE8 – 0xEA	0x11E8 – 0x11EA	Reserved	0x00
0xEB	0x11EB	Receive STS-3c Path – Receive Z3 Byte Capture Register	0x00
0xEC - 0xEE	0x11EC - 0x11EE	Reserved	0x00
0xEF	0x11EF	Receive STS-3c Path – Receive Z4 (K3) Byte Capture Register	0x00
0xF0 - 0xF2	0x11F0 – 0x11F2	Reserved	0x00
0xF3	0x11F3	Receive STS-3c Path – Receive Z5 Byte Capture Register	0x00
0xF4 - 0xFF	0x11F4 – 0x11FF	Reserved	



1.13.2 RECEIVE STS-3c POH PROCESSOR BLOCK REGISTER DESCRIPTION

Table 707: Receive STS-3c Path - Control Register - Byte 0 (Address Location= 0x1183)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused				Check	RDI-P	REI-P	B3 Error Type
				Stuff	Type	Error Type	
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION	
7 – 4	Unused	R/O	nis ed	
3	Check Stuff	R/W	Check (Pointer Adjustment) Stuff Select:	
			This READ/WRITE bit-field permits the user to enable/disable the SONET standard recommendation that a pointer increment or decrement operation, detected within 3 SONET frames of a previous pointer adjustment operation (e.g., negative stuff, positive stuff) is ignored.	
			0 - Disables this SQNET standard implementation. In this mode, all pointer-adjustment operations that are detected will be accepted.	
			1 – Enables this "SONET standard" implementation. In this mode, all pointer-adjustment operations that are detected within 3 SONET frame periods of a previous pointer-adjustment operation, will be ignored.	
2	RDI-P Type	R/W	Path – Remote Defect Indicator Type Select:	
		duc	This READ/WRITE bit-field permits the user to configure the Receive STS-3c POH Processor block to support either the "Single-Bit" or the "Enhanced" RDI-P, as described below.	
			0 - Configures the Receive STS-3c POH Processor block to support the Single-Bit RDI-P. In this mode, the Receive STS-3c POH Processor block will only monitor Bit 5, within the G1 byte (of incoming SPE data), in order to declare and clear the RDI-P indicator.	
	Z, K	solo ex	1 – Configures the Receive STS-3c POH Processor block to support the Enhanced RDI-P (ERDI-P). In this mode, the Receive STS-3c POH Processor block will monitor bits 5, 6 and 7, within the G1 byte, in order to declare and clear the RDI-P indicator.	
1	REI-P Error	R/W	REI-P Error Type:	
	Туре		This READ/WRITE bit-field permits the user to specify how the "Receive Path REI-P Error Count" register is incremented.	
			0 – Configures the Receive STS-3c POH Processor block to count REI-P Bit Errors.	
			In this case, the "Receive Path REI-P Error Count" register will be incremented by the value of the lower nibble within the G1 byte.	
			1 – Configures the Receive STS-3c POH Processor block to count REI-P Frame Errors.	
			In this case, the "Receive Path REI-P Error Count" register will be incremented by a single count each time the Receive STS-3c POH Processor block receives a G1 byte, in which bits 1 through 4 are set to a "non-zero" value.	



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

0	B3 Error Type	R/W	B3 Error Type:
			This READ/WRITE bit-field permits the user to specify how the "Receive Path B3 Error Count" register is incremented.
			0 – Configures the Receive STS-3c POH Processor block to count B3 bit errors. In this case, the "Receive Path B3 Error Count" register will be incremented by the number of bits, within the B3 value, that is in error.
			1 - Configures the Receive STS-3c POH Processor block to count B3 frame errors. In this case, the "Receive Path B3 Error Count" register will be incremented by the number of erred STS-3c frames.

The product or products mentioned in this are no ordered (OBS)

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 708: Receive STS-3c Path – Control Register – Byte 0 (Address Location= 0x1186)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			Unused				
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/W
0	0	0	0	0	0	0	0

0	J1 Unstable Indicator	R/O R/O	J1 – Path Trace Unstable Indicator:
ι	Unstable	R/O	J1 – Path Trace Unstable Indicator:
		hepro	This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the Path Trace Unstable condition. The Receive STS-3c POH Processor block will declare a J1 (Path Trace) Unstable condition, whenever the "J1 Unstable" counter reaches the value "8". The "J0 Unstable" counter will be incremented for each time that it receives a J1 message that differs from the previously received message. The "J1 Unstable" counter is cleared to "0" whenever the Receive STS-3c POH Processor block has received a given J1 Message 3 (or 5) consecutive times. **Note:** Receiving a given J1 Message 3 (or 5) consecutive times also sets this bit-field to "0". 0 - Path Trace Instability condition is NOT declared. 1 - Path Trace Instability condition is currently declared.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 709: Receive STS-3c Path – SONET Receive POH Status – Byte 0 (Address Location= 0x1187)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TIM-P	C2 Byte	UNEQ-P	PLM-P	RDI-P	RDI-P	LOP-P	AIS-P
Defect	Unstable	Defect	Defect	Defect	Unstable	Defect	Defect
Declared	Condition	Declared	Declared	Declared	Condition	Declared	Declared
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	TIM-P Defect	R/O	Trace Identification Mismatch (TIM-P) Defect Indicator:
	Declared		This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the Trace Identification Mismatch" (TIM-P) condition.
			The Receive STS-3c POH Processor block will declare the "TIM-P" condition, when none of the received 64 byte String (received via the J1 byte) matches the expected 64 byte message.
			The Receive STS-3c POH Processor block will clear the "TIM-P" condition, when 80% of the received 64 byte string (received via the J1 byte) matches the expected 64 byte message.
			0 – Indicates that the Receive STS-3c POH Processor block is NOT currently declaring the TIM-P condition.
			1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the TIM-P condition.
6	C2 Byte	R/O	C2 Byte (Path Signal Label Byte) Unstable Indicator:
	Unstable Condition		This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the "Path Signal Label Byte" Unstable condition.
	The	product	The Receive STS-3c POH Processor block will declare a C2 (Path Signal Label Byte) Unstable condition, whenever the "C2 Unstable" counter reaches the value "5". The "C2 Unstable" counter will be incremented for each time that it receives an STS-3c SPE with a C2 byte value that differs from the previously received C2 byte value. The "C2 Unstable" counter is cleared to "0" whenever the Receive STS-3c POH Processor block has received 3 (or 5) consecutive SPEs of the same C2 byte value.
		yo and	Note: Receiving a given C2 byte value in 3 (or 5) consecutive SPEs also sets this bit-field to "0".
			0 – C2 (Path Signal Label Byte) Unstable condition is NOT declared.
			1 – C2 (Path Signal Label Byte) Unstable condition is currently declared.
5	UNEQ-P	R/O	Path – Unequipped Indicator (UNEQ-P):
			This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the UNEQ-P condition.
			The Receive STS-3c POH Processor block will declare a UNEQ-P condition, if it receives at least five (5) consecutive STS-3c frames, in which the C2 byte was set to 0x00 (which indicates that the SPE is "Unequipped").
			The Receive STS-3c POH Processor block will clear the UNEQ-P condition, if it receives at least five (5) consecutive STS-3c frames, in which the C2 byte was set to a value other than 0x00.
			0 - Indicates that the Receive STS-3c POH Processor block is NOT declaring

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			the UNEQ-P condition.
			1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the UNEQ-P condition.
			Note:
			1. The Receive STS-3c POH Processor block will not declare the UNEQ-P condition if it configured to expect to receive SONET frames with C2 bytes being set to "0x00" (e.g., if the "Receive STS-3c Path – Expected Path Label Value" Register is set to "0x00".
			2. The Address Locations of the "Receive STS-3c Path – Expected Path Label Value" Register is 0x1197
4	PLM-P	R/O	Path Payload Mismatch Indicator (PLM-P):
	Defect Declared		This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the PLM-P condition.
			The Receive STS-3c POH Processor block will declare an PLM-P condition, if it receives at least five (5) consecutive STS-3c frames, in which the C2 byte was set to a value other than that which it is expecting to receive.
			Whenever the Receive STS-3c POH Processor block is determine whether or not it should declare the PLM-P defect, it checks the contents of the following two registers.
			The "Receive STS-3c Path – Received Path Label Value" Register
			The "Receive STS-3c Path Expected Path Label Value" Register
			The "Receive STS-3c Path – Expected Path Label Value" Register contains the value of the C2 bytes, that the Receive STS-3c POH Processor blocks expects to receive.
			The "Receive STS-3c Path – Received Path Label Value" Register contains the value of the C2 byte that the Receive STS-3c POH Processor block has most received "validated" (by receiving this same C2 byte in five consecutive SONET frames).
		8	The Receive STS-3c POH Processor block will declare the PLM-P defect, if the contents of these two register do not match. The Receive STS-3c POH Processor block will clear the PLM-P condition if whenever the contents of these two registers do match.
		No	QOPLMP defect is currently not being declared.
	A	10/10	— PLM-P defect is currently being declared. Note:
		9,00	The Receive STS-3c POH Processor block will clear the PLM-P defect, upon detecting the UNEQ-P condition.
			2. The Address Location of the "Receive STS-3c Path – Received Path Label Value" Register is 0x1196
			3. The Address Location of the Receive STS-3c Path – Expected Path Label Value" Register is 0x1196
3	RDI-P	R/O	Path Remote Defect Indicator (RDI-P):
			This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the RDI-P condition.
			If the Receive STS-3c POH Processor block is configured to support the "Single-bit RDI-P" function, then it will declare an RDI-P condition if Bit 5 (within the G1 byte of the incoming STS-3c frame) is set to "1" for "RDI-P_THRD" number of consecutive STS-3c frames.
			If the Receive STS-3c POH Processor block is configured to support the Enhanced RDI-P" (ERDI-P) function, then it will declare an RDI-P condition if

Bits 5, 6 and 7 (within the G1 byte of the incoming STS-3c frame) are set to [0, 1, 0], 1, 0, 1, 0, 1 or 11, 1, 0] for "RDI-P_THRD" number of consecutive STS-3c Ponteriors. 0 - Indicates that the Receive STS-3c POH Processor block is NOT declaring an RDI-P condition. 1 - Indicates that the Receive STS-3c POH Processor block is currently declaring an RDI-P condition. Note: 1. The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P_THRD) within the "Receive STS-3c Path - SONET Receive RDI-P Register. 2 RDI-P Unstable R/O RDI-P (Path - Remote Defect Indicator) Unstable: This READ-ONLY bit-fled indicates whether or not the Receive STS-3c POH Processor block is currently declaring the "RDI-P Unstable" condition whenever the "RDI-P Unstable" counter is consensed for each time that the Receive STS-3c POH Processor block receives an RDI-P value that differs from that of the provibus StS-3c trame. The "RDI-P Unstable" counter is cleared to "0" whenever the same RDI-P value is received in "RDI-P_THRD" consecutive STS-3c frames. Note: Receiving a given (2DI-P value, in "RDI-P THRD" consecutive STS-3c frames on StS-3c POH Processor block receives an RDI-P value that differs to mit that of the provibus StS-3c erame. The "RDI-P Unstable counter is cleared to "0" whenever the same RDI-P value is received in "RDI-P_THRD" consecutive STS-3c grain—SONET Receive RDI-P Register. 2 The Address Location of the Receive STS-3c Path — SONET Receive RDI-P Registers is ox 1193 1 LOP-P Defect Declared 1 Receive STS-3c POH Processor block will declare the LOP-P condition. The Receive STS-3c POH Processor block is to 10 consecutive SONET frames. Further, the Receive STS-3c POH Processor block will declare the LOP-P condition. The Receive STS-3c POH Processor block will clear the LOP-P condition. 1 - Indicates that th	1, 0], [1, 0, 1] or [1, 1, 0] for "RDI-P_THRD" number of consecutive STS-3c frames. 0 - Indicates that the Receive STS-3c POH Processor block is NOT declaring an RDI-P condition. 1 - Indicates that the Receive STS-3c POH Processor block is currently declaring an RDI-P condition. Note: 1. The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P_THRD) within the "Receive STS-3c Path - SONET Receive RDI-P Registers. 2. The Address Location of the "Receive STS-3c Path - SONET Receive RDI-P Registers is 0x1193 2. RDI-P Unstable R/O R/O R/O R/O R/O R/O R/O R/				
an RDI-P condition. 1 - Indicates that the Receive STS-3c POH Processor block is currently declaring an RDI-P condition. Note: 1. The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-3c Path - SONET Receive RDI-P Registers. 2. The Address Location of the "Receive STS-3c Path - SONET Receive RDI-P Registers is 0x1193 2. RDI-P (Path - Remote Defect Indicator) Usefable: This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the "RDI-P Unstable" condition. The Receive STS-3c POH Processor block will declare a "RDI-P I Unstable" condition whenever the "RDI-P Unstable condition or reaches the value "RDI-P THRD". The "RDI-P Unstable" condition is incremented for each time that the Receive STS-3c POH Processor block receives an RDI-P value that differs from that of the previous STS-3c frames. Note: Receiving a gilven RDI-P value, in "RDI-P_THRD" consecutive STS-3c frames. Note: Receiving a gilven RDI-P value, in "RDI-P_THRD" consecutive STS-3c frames and the stable properties data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-3c path — SONET Receive RDI-P Register. 2. The Address Location of the Receive STS-3c Path — SONET Receive RDI-P Register. 2. The Address Location of the Receive STS-3c Path — SONET Receive RDI-P Register. 2. This Address Location of the Receive STS-3c Path — SONET Receive RDI-P Register. 2. This Address Location of the Receive STS-3c Path — SONET Receive RDI-P Register. 3. This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block will declare the LOP-P condition. The Receive STS-3c POH Processor block will declare the LOP-P condition, whenever the Receive STS-3c POH Processor block will declare the LOP-P condition, whenever the Receive STS-3c POH Processor block will clear the LOP-P condition, whenever the Receive STS-3c POH Processor block is currently declaring the LOP-P condition. 1 - Indicates t	an RDI-P condition. 1 - Indicates that the Receive STS-3c POH Processor block is currently declaring an RDI-P condition. Note: 1. The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-3c Path - SONET Receive RDI-P Register. 2. The Address Location of the "Receive STS-3c Path - SONET Receive RDI-P Registers is 0x1193 2. RDI-P Unstable RIO RIO RIO-P Processor block is currently declaring the "RDI-P Unstable" condition. The Receive STS-3c POH Processor block is currently declaring the "RDI-P Unstable" condition whenever the "RDI-P Unstable" condition is received in "RDI-P Unstable" condition whenever the "RDI-P Unstable" condition is Currently declared. Note: Note: Receiver STS-3c POH Processor block will declare an RDI-P Value in "RDI-P THRD" consecutive STS-3c Value in "RDI-P Unstable" condition is currently declared. Note: 1. The Address Location of the Receive STS-3c Path - SONET Receive STS-3c Path - SONET Receive RDI-P Register. 2. The Address Location of the Receive STS-3c Path - SONET Receive RDI-P Processor block will declare the LOP-P condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the "CPH processor block will declare the LOP-P condition, whenever the Receive STS-3c POH Processor block will declare the LOP-P condition, whenever the Receive STS-3c POH Processor block will declare the LOP-P condition, and the LO				
declaring an RDI-P condition. Note: 1. The user can specify the value for "RDI-P. THRD" by writing the appropriate date into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-3c Path – SONET Receive RDI-P Registers. 2. The Address Location of the "Receive STS-3c Path – SONET Receive RDI-P Registers is 0x1193 RIO Unstable RIO RDI-P (Path – Remote Defect Indicator) Ustable: This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the "RDI-P Unstable" condition. The Receive STS-3c POH Processor block receives an RDI-P value that differs from that of the previous STS-3c FOH Processor block receives an RDI-P value that differs from that of the previous STS-3c FOH Processor block receives an RDI-P value that differs from that of the previous STS-3c FOH Processor block receives an RDI-P value that differs from that of the previous STS-3c FOH Processor block receives an RDI-P value is received in "RDI-P_THRD" consecutive STS-3c FOH Processor block receives an RDI-P value is received in "RDI-P_THRD" consecutive STS-3c FOH processor description is NOT declared. Note: Receiving a given PDI-P value, in "RDI-P_THRD" consecutive STS-3c FOH processor block will declared. 1. RPI-P Unstable condition is currently declared. Note: Receive STS-3c FOH Processor block will declare the LOP-P condition. The Address Location of the Receive STS-3c POH Processor block will declare the LOP-P condition. The Receive STS-3c POH Processor block will declare the LOP-P condition. The Receive STS-3c POH Processor block will declare the LOP-P condition, whenever the Receive STS-3c POH Processor detects valid pointer bytes (e.g., the H1 and H2 bytes, within the TOH) within 8 to 10 consecutive NoTe Trames. 1. Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-P condition. 1. Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-P condition.	declaring an RDI-P condition. Note: 1. The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-3c Path – SONET Receive RDI-P Register. 2. The Address Location of the "Receive STS-3c Path – SONET Receive RDI-P Registers is 0x1193 R/O Unstable R/O Unst				
1. The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through (RDI-P THRD) within the "Receive STS-3c Path – SONET Receive RDI-P Register. 2. The Address Location of the "Receive STS-3c Path – SONET Receive RDI-P Registers is 0x1193 2. RDI-P Unstable R/O Unstable R/O Unstable R/O RDI-P (Pgth – Remote Defect Indicator) Unstable: This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently deplaring the "RDI-P Unstable" condition. The Receive STS-3c POH Processor block will declare at RDII-P I Unstable' condition whenever the "RDI-P Unstable" condition. The Receive STS-3c POH Processor block receives an RDI-P value that the Receive STS-3c POH Processor block receives an RDI-P value that differs from that of the previous STS-3c frame. The "RDI-P Unstable" counter is cleared to "0" whenever the same RDI-P value, in "RDI-P_THRD" consecutive STS-3c frames. Note: Receiving a given RDI-P value, in "RDI-P_THRD" consecutive STS-3c Fath — SONET Receive RDI-P register. Note: Note: Receiving a given RDI-P value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-3c Fath — SONET Receive RDI-P Register. 2. The Address Location of the Receive STS-3c Path — SONET Receive RDI-P Registers is 0x1193 1. LOP-P Defect Declared 1. LOP-P Defect Declared 1. RRD-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block will declare the LOP-P condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the TOH) within 8 to 10 consecutive SONET frames. Further, the Receive STS-3c POH Processor block will declare the LOP-P condition, whenever the Receive STS-3c POH Processor block will declare the LOP-P condition, whenever the Receive STS-3c POH Processor block is not detects avail pointer bytes (e.g., the H1 and H2 bytes, within the TOH) and normal NDF value for three consecutive SONET frames. 0. Indicates that the Receive STS-3c POH Processor block is current	1. The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-3c Path – SONET Receive RDI-P Register. 2. The Address Location of the "Receive STS-3c Path – SONET Receive RDI-P Registers is 0x1193 2. RDI-P (Path – Remote Defect Indicator) Unstable: This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently deplaring the "RDI-P Unstable" condition. The Receive STS-3c POH Processor block will declare a "RDI-P Unstable" condition whenever the "RDI-P Unstable" content is incremented for each time that the Receive STS-3c POH Processor block receives an RDI-P value that differs from that of the previous STS-3c frame. The "RDI-P Unstable" consecutive STS-3c POH Processor block receives an RDI-P value that differs from that of the previous STS-3c frame. Note: Receive STS-3c frames 1. The Unstable condition is NOT declared. 1. RDI-P Unstable condition is currently declared. 1. RDI-P U				•
appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-3c Path – SONET Receive RDI-P Register. 2. The Address Location of the "Receive STS-3c Path – SONET Receive RDI-P Registers is 0x1193 2. RDI-P (Instable) R/O Unstable R/O RDI-P (Path – Remote Defect Indicator) Upstable: This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the "RDI-P Unstable" condition. The Receive STS-3c POH Processor block will declare a "RDI-P Instable" condition whenever the "RDI-P Unstable" counter is incremented for each time that the Receive STS-3c POH-Processor block receives an RDI-P value that differs from that of the previous \$15.3c frame. The "RDI-P Unstable" counter is cleared to "0" whenever the same RDI-P value is received in "RDI-P_THRD" consecutive STS-3c frames. Note: Receiving a given RDI-P value, in "RDI-P_THRD" consecutive STS-3c frames also clears this bit-field to "0". 0 - RDI-R Unstable condition is NOT declared. 1 - RDI-P Unstable condition is currently declared. Note: 1 - The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-3c Path SONET Receive RDI-P Registers. 2 - The Address Location of the Receive STS-3c Path – SONET Receive RDI-P Registers is 0x1193 1 LOP-P Defect Declared 1 - RDI-P Unstable condition is currently declaring the LOP-P (Loss of Pointer) condition. The Receive STS-3c POH Processor block will declare the LOP-P condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the TOH) within 8 to 0 consecutive SONET frames. Further, the Receive STS-3c POH Processor block will declare the LOP-P condition, whenever the Receive STS-3c POH Processor detects valid pointer bytes (e.g., the H1 and H2 bytes, within the TOH) and normal NDF value for three consecutive SONET frames. 0 - Indicates that the Receive STS-3c POH Processor block is NOT declaring the LOP-P condition. 1 - Indicates that the Receive STS-3c POH Process	appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-3c Path – SONET Receive RDI-P Register. 2. The Address Location of the "Receive STS-3c Path – SONET Receive RDI-P Registers is 0x1193 RIO Unstable RIO RDI-P (Path – Remote Defect Indicator) Unstable: This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently deflaring the "RDI-P Unstable" condition. The Receive STS-3c POH Processor block will declare a "RDI-P I Unstable" condition whenever the "RDI-P Unstable" contents in caremented for each time that the Receive STS-3c POH Processor block receives an RDI-P value that differs from that of the previous STS-3c frame. The "RDI-P Unstable" counter is cleared to "0" whenever the same RDI-P value, in "RDI-P Unstable" counter is cleared to "0" whenever the same RDI-P value, in "RDI-P THRD" consecutive STS-3c/Grames plso clears this bit-field to "0". 0 - RDI-P Unstable condition is NOT declared. 1 - RDI-P Unstable condition is Currently declared. Note: 1 The Address Location of the Receive STS-3c Path – SONET Receive STS-3c Path — SONET Receive STS-3c Path — SONET Receive STS-3c Path — SONET Receive RDI-P Register. 2 The Address Location of the Receive STS-3c Path — SONET Receive RDI-P Registers is Sufficient in the Receive STS-3c POH Processor block will declare the LOP-P condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the TOH) within 8 to 10 consecutive SONET frames. Further, the Receive STS-3c POH Processor block will declare the COP-P condition, whenever the Receive STS-3c POH Processor block will clear the LOP-P condition, whenever the Receive STS-3c POH Processor block will declare the COP-P condition, if the COP-P condition, 1 - Indicates that the Receive STS-3c POH Processor block is Currently declaring the LOP-P condition. 1 - Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-P condition.				Note:
RDI-P (Path – Remote Defect Indicator) Unstable: RIOP (Unstable) RIOP (Path – Remote Defect Indicator) Unstable: This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently deplaring in explicit Processor block mild declare a "RDI-P Unstable" condition. The Receive STS-3c POH Processor block will declare a "RDI-P Unstable" condition whenever the "RDI-P Unstable" content in exception whenever the "RDI-P Unstable" content in that the Receive STS-3c POH Processor block receives an RDI-P value that differs from that of the prevolus STS-3c frame. The "RDI-P unstable" content is cleared to "0" whenever the same RDI-P value is received in "RDI-P_THRD" consecutive STS-3c (fathes siles clears this bit-field to "0". 0 - RDI-P Unstable condition is NOT declared. 1 - RDI-P Unstable condition is currently declared. Note: 1 - RDI-P Unstable condition is currently declared. Note: 1 - RDI-P Unstable condition of the Receive STS-3c Path – SONET Receive RDI-P Registers. 2 - The Address Location of the Receive STS-3c Path – SONET Receive RDI-P Registers is 0x1193 1 LOP-P Defect Declared 1 - RDI-P This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the LOP-P (Loss of Pointer) condition. The Receive STS-3c POH Processor block will declare the LOP-P condition. The Receive STS-3c POH Processor block will declare the LOP-P condition, whenever the Receive STS-3c POH Processor detects valid pointer bytes (e.g., the H1 and H2 bytes, within the TOH) and normal NDF value for three consecutive SONET frames. 0 - Indicates that the Receive STS-3c POH Processor block is NOT declaring the LOP-P condition. 1 - Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-P condition.	RDI-P (Path – Remote Defect Indicator) Unstable: This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the "RDI-P Unstable" condition. The Receive STS-3c POH Processor block will declare a "RDI-P I Unstable" condition whenever the "RDI-P Unstable" condition whenever the "RDI-P Unstable" counter reaches the value "RDI-P THRD". The "RDI-P Unstable" counter is incremented for each time that the Receive STS-3c POH Processor block receives an RDI-P value that differs from that of the prevolus STS-3c Fohner. The "RDI-P unstable" counter is cleared to "0" whenever the same RDI-P value is received in "RDI-P_THRD" consecutive STS-3c frames. Note: Receiving a given RDI-P value, in "RDI-P_THRD" consecutive STS-3c frames also clears this bit-field to "0". 0 - RDI-P Unstable condition is NOT declared. 1 - RDI-P Unstable condition is currently declared. Note: 1 - RDI-P Unstable condition is currently declared. Note: 2 - The Address Location of the Receive STS-3c Path - SONET Receive RDI-P Registers is 0x1193 1 LOP-P Defect Declared 1 - RDI-P Indicator (LOP-P): This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the LOP-P (Loss of Pointer) condition. The Receive STS-3c POH Processor block will declare the LOP-P condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the TOH) within 8 to 0 consecutive SONET frames. Further, the Receive STS-3c POH Processor block will clear the LOP-P condition, whenever the Receive STS-3c POH Processor block will clear the LOP-P condition, whenever the Receive STS-3c POH Processor detects valid pointer bytes (e.g., the H1 and H2 bytes, within the TOH) and normal NDF value for three consecutive SONET frames. 0 - Indicates that the Receive STS-3c POH Processor block is NOT declaring the LOP-P condition. 1 - Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-P condition.				appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-
Unstable This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the "RDI-P Unstable" condition. The Receive STS-3c POH Processor block will declare and RDI-P I Unstable" condition whenever the "RDI-P Unstable Counter" reaches the value "RDI-P THRD". The "RDI-P Unstable Counter is incremented for each time that the Receive STS-3c POH Processor block receives an RDI-P value that differs from that of the previous STS-3c trame. The "RDI-P Unstable" counter is cleared to "0" whenever the same RDI-P value in "RDI-P_THRD" consecutive STS-3c frames. **Note:** Receiving a given RDI-P value, in "RDI-P_THRD" consecutive STS-3c (amies also clears this bit-field to "0". 0 - RDI-P Unstable condition is NOT declared. 1 - RDI-P Unstable condition is currently declared. Note: 1 - The Address Location of the Receive STS-3c Path - SONET Receive RDI-P Register. 2 - The Address Location of the Receive STS-3c Path - SONET Receive RDI-P Register. 2 - The Address Location of the Receive STS-3c Poth Processor block is currently declaring the LOP-P (Loss of Pointer) condition. The Receive STS-3c POH Processor block will declare the LOP-P condition. The Receive STS-3c POH Processor block will declare the LOP-P condition, whenever the Receive STS-3c POH Processor block will clear the LOP-P condition, whenever the Receive STS-3c POH Processor block will clear the LOP-P condition, whenever the Receive STS-3c POH Processor block will clear the LOP-P condition, whenever the Receive STS-3c POH Processor block will clear the LOP-P condition, whenever the Receive STS-3c POH Processor block will clear the LOP-P condition, whenever the Receive STS-3c POH Processor block is NOT declaring the LOP-P condition. 1 - Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-P condition.	Unstable This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the "RDI-P Unstable" condition. The Receive STS-3c POH Processor block will declare a "RDI-P I Unstable" condition whenever the "RDI-P Unstable" condition whenever the "RDI-P Unstable" condition whenever the "RDI-P Unstable" counter is incremented for each time that the Receive STS-3c POH Processor block receives an RDI-P value that differs from that of the previous STS-3c frame. The "RDI-P Unlatable" counter is cleared to "0" whenever the same RDI-P value in "RDI-P THRD" consecutive STS-3c frames. **Note:** Receiving a given RDI-P value, in "RDI-P THRD" consecutive STS-3c frames. **Note:** Receiving a given RDI-P value, in "RDI-P THRD" consecutive STS-3c frames. **Note:** Receiving a given RDI-P value in "RDI-P THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-3c Path - SONET Receive RDI-P Register. **2. The Address Location of the Receive STS-3c Path - SONET Receive RDI-P Registers is 0x1193 1 LOP-P Defect Declared **1. This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the LOP-P (Loss of Pointer) condition. The Receive STS-3c POH Processor block will declare the LOP-P condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the TOH) within 8 to 10 consecutive SONET frames. Further, the Receive STS-3c POH Processor block will declare the LOP-P condition, whenever the Receive STS-3c POH Processor block will clear the LOP-P condition, whenever the Receive STS-3c POH Processor block will depointer bytes (e.g., the H1 and H2 bytes, within the TOH) and normal NDF value for three consecutive SONET frames. **O - Indicates that the Receive STS-3c POH Processor block is NOT declaring the LOP-P condition. 1 - Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-P condition.				
This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the "RDI-P Unstable" condition whenever the "RDI-P Unstable" counter" reaches the value "RDI-P THRD". The "RDI-P Unstable" counter is incremented for each time that the Receive STS-3c POH Processor block receives an RDI-P value that differs from that of the previous STS-3c Frame. The "RDI-P Unstable" counter is cleared to "0" whenever the same RDI-P value is received in "RDI-P_THRD" consecutive STS-3c frames. **Note:** **	This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently dealaring the "RDI-P Unstable" condition. The Receive STS-3c POH Processor block will declare a "RDI-P I Unstable" condition whenever the "RDI-P Unstable" counter is incremented for each time that the Receive STS-3c POH Processor block receives an RDI-P value that differs from that of the previous STS-3c frames. **ROI-P Unstable condition is STS-3c frames.** **Note: Receiving a given RDI-P value, in "RDI-P_THRD" consecutive STS-3c frames.** **Note: Receiving a given RDI-P value, in "RDI-P_THRD" consecutive STS-3c frames.** **Note: Receiving a given RDI-P value, in "RDI-P_THRD" consecutive STS-3c frames.** **Note: Receiving a given RDI-P value, in "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-3c Raith." SONET Receive RDI-P Register. **The Address Location of the Receive STS-3c Path - SONET Receive RDI-P Registers is 0x1193* 1 LOP-P Defect Declared LOP-P Defect Declared LOP-P Receive RDI-P Receive RDI-P Receive STS-3c POH Processor block is currently declaring the LOP-P (Loss of Pointer) condition. The Receive STS-3c POH Processor block will declare the LOP-P condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the TOH) within 8 to 10 consecutive SONET frames. Further, the Receive STS-3c POH Processor block will declare the LOP-P condition, whenever the Receive STS-3c POH Processor block will clear the LOP-P condition, whenever the Receive STS-3c POH Processor block will clear the LOP-P condition, whenever the Receive STS-3c POH Processor block will clear the LOP-P condition, whenever the Receive STS-3c POH Processor block is NOT declaring the LOP-P condition. 1 - Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-P condition. 2 - Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-P condition.	2		R/O	RDI-P (Path – Remote Defect Indicator) Unstable:
3c trames also clears this bit-field to "0". 0 - RDI-P Unstable condition is NOT declared. 1 - RDI-P Unstable condition is currently declared. Note 1 The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-3c Rath - SONET Receive RDI-P Register. 2 The Address Location of the Receive STS-3c Path - SONET Receive RDI-P Registers is 0x1193 1 LOP-P Defect Declared R/O Loss of Pointer Indicator (LOP-P): This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the LOP-P (Loss of Pointer) condition. The Receive STS-3c POH Processor block will declare the LOP-P condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the TOH) within 8 to 10 consecutive SONET frames. Further, the Receive STS-3c POH Processor block will declare the LOP-P condition, whenever the Receive STS-3c POH Processor detects 8 to 10 consecutive NDF events. The Receive STS-3c POH Processor block will clear the LOP-P condition, whenever the Receive STS-3c POH Processor detects valid pointer bytes (e.g., the H1 and H2 bytes, within the TOH) and normal NDF value for three consecutive SONET frames. 0 - Indicates that the Receive STS-3c POH Processor block is NOT declaring the LOP-P condition. 1 - Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-P condition.	3c trames also clears this bit-field to "0". 0 - RDI-P Unstable condition is NOT declared. 1 - RDI-P Unstable condition is currently declared. Note 1 The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-3c, Rath.—SONET Receive RDI-P Register. 2 The Address Location of the Receive STS-3c Path — SONET Receive RDI-P Registers is 0x1193 1 LOP-P Defect Declared 1 LOP-P Defect Declared 1 R/O 1 LOP-P Condition, If it cannot detect a valid pointer (LOP-P): 1 This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the LOP-P (Loss of Pointer) condition. The Receive STS-3c POH Processor block will declare the LOP-P condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the TOH) within 8 to 10 consecutive SONET frames. Further, the Receive STS-3c POH Processor block will clear the LOP-P condition, whenever the Receive STS-3c POH Processor detects valid pointer bytes (e.g., the H1 and H2 bytes, within the TOH) and normal NDF value for three consecutive SONET frames. 1 O – Indicates that the Receive STS-3c POH Processor block is NOT declaring the LOP-P condition. 2 NO Endicates that the Receive STS-3c POH Processor block is currently declaring the LOP-P condition.		Unstable		Processor block is currently declaring the "RDI-P Unstable" condition. The Receive STS-3c POH Processor block will declare a "RDI-P I Unstable" condition whenever the "RDI-P Unstable Counter" reaches the value "RDI-P THRD". The "RDI-P Unstable" counter is incremented for each time that the Receive STS-3c POH Processor block receives an RDI-P value that differs from that of the previous STS-3c frame. The "RDI-P Unstable" counter is cleared to "0" whenever the same RDI-P value is received in "RDI-P_THRD"
1 - RDI-P Unstable condition is currently declared. Note: 1 The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-3c Path - SONET Receive RDI-P Register. 2 The Address Location of the Receive STS-3c Path - SONET Receive RDI-P Registers is 0x1193 1 LOP-P Defect Declared R/O Loss of Pointer Indicator (LOP-P): This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the LOP-P (Loss of Pointer) condition. The Receive STS-3c POH Processor block will declare the LOP-P condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the TOH) within 8 to 10 consecutive SONET frames. Further, the Receive STS-3c POH Processor block will clear the LOP-P condition, whenever the Receive STS-3c POH Processor detects valid pointer bytes (e.g., the H1 and H2 bytes, within the TOH) and normal NDF value for three consecutive SONET frames. 0 - Indicates that the Receive STS-3c POH Processor block is NOT declaring the LOP-P condition. 1 - Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-P condition.	1 - RDI-P Unstable condition is currently declared. Note: 1 The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-3c Rath. SONET Receive RDI-P Register. 2 The Address Location of the Receive STS-3c Path - SONET Receive RDI-P Registers is 0x1193 1 LOP-P Defect Declared Company D				
Note 1 The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-3c Path SONET Receive RDI-P Register. 2 The Address Location of the Receive STS-3c Path – SONET Receive RDI-P Registers is 0x1193 1 LOP-P Defect Declared 1 LOP-P Defect Declared 1 This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the LOP-P (Loss of Pointer) condition. The Receive STS-3c POH Processor block will declare the LOP-P condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the TOH) within 8 to 10 consecutive SONET frames. Further, the Receive STS-3c POH Processor block will clear the LOP-P condition, whenever the Receive STS-3c POH Processor detects valid pointer bytes (e.g., the H1 and H2 bytes, within the TOH) and normal NDF value for three consecutive SONET frames. 0 - Indicates that the Receive STS-3c POH Processor block is NOT declaring the LOP-P condition. 1 - Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-P condition.	Note 1 The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-3c Path - SONET Receive RDI-P Register. 2 The Address Location of the Receive STS-3c Path - SONET Receive RDI-P Registers is 0x1193 1 LOP-P Defect Declared R/O Declared R/O Declared R/O Defect Declared R/O Declare				0 – RDI-P Unstable condition is NOT declared.
Defect Declared This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the LOP-P (Loss of Pointer) condition. The Receive STS-3c POH Processor block will declare the LOP-P condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the TOH) within 8 to 10 consecutive SONET frames. Further, the Receive STS-3c POH Processor block will declare the LOP-P condition, if it detects 8 to 10 consecutive NDF events. The Receive STS-3c POH Processor block will clear the LOP-P condition, whenever the Receive STS-3c POH Processor detects valid pointer bytes (e.g., the H1 and H2 bytes, within the TOH) and normal NDF value for three consecutive SONET frames. 0 – Indicates that the Receive STS-3c POH Processor block is NOT declaring the LOP-P condition. 1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-P condition.	Defect Declared This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the LOP-P (Loss of Pointer) condition. The Receive STS-3c POH Processor block will declare the LOP-P condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the TOH) within 8 to 10 consecutive SONET frames. Further, the Receive STS-3c POH Processor block will declare the LOP-P condition, if it detects 8 to 10 consecutive NDF events. The Receive STS-3c POH Processor block will clear the LOP-P condition, whenever the Receive STS-3c POH Processor detects valid pointer bytes (e.g., the H1 and H2 bytes, within the TOH) and normal NDF value for three consecutive SONET frames. 0 – Indicates that the Receive STS-3c POH Processor block is NOT declaring the LOP-P condition. 1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-P condition.			roduct	Note 1. The user can specify the value for "RDI-P_THRD" by writing the appropriate data into Bits 3 through 0 (RDI-P THRD) within the "Receive STS-3c Path — SONET Receive RDI-P Register. 2. The Address Location of the Receive STS-3c Path — SONET Receive RDI-
Defect Declared This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the LOP-P (Loss of Pointer) condition. The Receive STS-3c POH Processor block will declare the LOP-P condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the TOH) within 8 to 10 consecutive SONET frames. Further, the Receive STS-3c POH Processor block will declare the LOP-P condition, if it detects 8 to 10 consecutive NDF events. The Receive STS-3c POH Processor block will clear the LOP-P condition, whenever the Receive STS-3c POH Processor detects valid pointer bytes (e.g., the H1 and H2 bytes, within the TOH) and normal NDF value for three consecutive SONET frames. 0 – Indicates that the Receive STS-3c POH Processor block is NOT declaring the LOP-P condition. 1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-P condition.	Defect Declared This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is currently declaring the LOP-P (Loss of Pointer) condition. The Receive STS-3c POH Processor block will declare the LOP-P condition, if it cannot detect a valid pointer (H1 and H2 bytes, within the TOH) within 8 to 10 consecutive SONET frames. Further, the Receive STS-3c POH Processor block will declare the LOP-P condition, if it detects 8 to 10 consecutive NDF events. The Receive STS-3c POH Processor block will clear the LOP-P condition, whenever the Receive STS-3c POH Processor detects valid pointer bytes (e.g., the H1 and H2 bytes, within the TOH) and normal NDF value for three consecutive SONET frames. 0 – Indicates that the Receive STS-3c POH Processor block is NOT declaring the LOP-P condition. 1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-P condition.	1	LOP-P	R/O	Loss of Pointer Indicator (LOP-P):
it cannot detect a valid pointer (H1 and H2 bytes, within the TOH) within 8 to 10 consecutive SONET frames. Further, the Receive STS-3c POH Processor block will declare the LOP-P condition, if it detects 8 to 10 consecutive NDF events. The Receive STS-3c POH Processor block will clear the LOP-P condition, whenever the Receive STS-3c POH Processor detects valid pointer bytes (e.g., the H1 and H2 bytes, within the TOH) and normal NDF value for three consecutive SONET frames. 0 – Indicates that the Receive STS-3c POH Processor block is NOT declaring the LOP-P condition. 1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-P condition.	it cannot detect a valid pointer (H1 and H2 bytes, within the TOH) within 8 to 10 consecutive SONET frames. Further, the Receive STS-3c POH Processor block will declare the LOP-P condition, if it detects 8 to 10 consecutive NDF events. The Receive STS-3c POH Processor block will clear the LOP-P condition, whenever the Receive STS-3c POH Processor detects valid pointer bytes (e.g., the H1 and H2 bytes, within the TOH) and normal NDF value for three consecutive SONET frames. 0 – Indicates that the Receive STS-3c POH Processor block is NOT declaring the LOP-P condition. 1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-P condition.			ato of	This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH
whenever the Receive STS-3c POH Processor detects valid pointer bytes (e.g., the H1 and H2 bytes, within the TOH) and normal NDF value for three consecutive SONET frames. 0 – Indicates that the Receive STS-3c POH Processor block is NOT declaring the LOP-P condition. 1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-P condition.	whenever the Receive STS-3c POH Processor detects valid pointer bytes (e.g., the H1 and H2 bytes, within the TOH) and normal NDF value for three consecutive SONET frames. 0 – Indicates that the Receive STS-3c POH Processor block is NOT declaring the LOP-P condition. 1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-P condition. 0 AIS-P R/O Path AIS (AIS-P) Indicator:			all	it cannot detect a valid pointer (H1 and H2 bytes, within the TOH) within 8 to 10 consecutive SONET frames. Further, the Receive STS-3c POH Processor block will declare the LOP-P condition, if it detects 8 to 10 consecutive NDF
the LOP-P condition. 1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-P condition.	the LOP-P condition. 1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-P condition. 0 AIS-P R/O Path AIS (AIS-P) Indicator:				whenever the Receive STS-3c POH Processor detects valid pointer bytes (e.g., the H1 and H2 bytes, within the TOH) and normal NDF value for three
declaring the LOP-P condition.	declaring the LOP-P condition. O AIS-P R/O Path AIS (AIS-P) Indicator:				
0 AIS-P R/O Path AIS (AIS-P) Indicator:	i am i no (i no i) maioaiori				
	This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH	0	AIS-P	R/O	Path AIS (AIS-P) Indicator:
This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH					This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Processor block is currently declaring an AIS-P condition. The Receive STS-
3c POH Processor block will declare an AIS-P if it detects all of the following
conditions for three consecutive STS-3c frames.

- a. The H1, H2 and H3 bytes are set to an "All Ones" pattern.
- b. The entire SPE is set to an "All Ones" pattern.

The Receive STS-3c POH Processor block will clear the AIS-P indicator when it detects a valid STS-3c pointer (H1 and H2 bytes) and a "set" or "normal" NDF for three consecutive STS-3c frames.

- 0 Indicates that the Receive STS-3c POH Processor block is NOT currently declaring the AIS-P defect.
- 1 Indicates that the Receive STS-3c POH Processor block is currently declaring the AIS-P defect.

Note: The Receive STS-3c POH Processor block will NOT declare the LOP-P condition if it detects an "All Ones" pattern in the H1, H2 and H3 bytes. It will, instead, declare the AlS-P condition.

798

Table 710: Receive STS-3c Path – SONET Receive Path Interrupt Status – Byte 2 (Address Location= 0x1189)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Change in AIS-C Condition Interrupt Status	Change in LOP-C Condition Interrupt Status	Detection of AIS Pointer Interrupt Status	Detection of Pointer Change Interrupt Status	POH Capture Interrupt Status	Change in TIM-P Condition Interrupt Status	Change in J1 Unstable Condition Interrupt Status
R/O	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7	Unused	R/O	thing
6	Change in AIS-C Condition Interrupt Status Change in LOP-C Condition Interrupt Status	RUR	Change in AIS-C (AIS Concatenation) Condition Interrupt Status: This RESET upon-READ bit-field permits indicates whether or not the "Change in AIS-C Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then an interrupt will be generated in response to either of the following events. a. Whenever the Receive STS-3c POH Processor block declares an AIS-C condition with one of the STS-1 signals; within the incoming STS-3c signal. b. Whenever the Receive STS-3c POH Processor block clears the AIS-C condition with one of the STS-1 signals; within the incoming STS-3c signal. O Indicates that the "Change in AIS-C Condition" Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the "Change in AIS-C Condition" Interrupt has occurred since the last read of this register. Note: The user can determine the current state of AIS-C by reading out the contents of the "Receive STS-3c Path
5	Change in LOP-C Condition	RUR	 AIS-C Status" Register (Address Locations: 0x11B3). Change in LOP-C (Loss of Pointer - Concatenation)
	Interrupt Status		Condition Interrupt Status:
			This RESET-upon-READ bit-field permits indicates whether or not the "Change in LOP-C Condition" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then an interrupt will be generated in response to either of the following events.
			 a. Whenever the Receive STS-3c POH Processor block declares an LOP-C condition with one of the STS-1 signals; within the incoming STS-3c signal.
			 Whenever the Receive STS-3c POH Processor block clears the LOP-C condition with one of the STS-1 signals; within the incoming STS-3c signal.
			0 – Indicates that the "Change in LOP-C Condition" Interrupt has NOT occurred since the last read of this register.

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			1 – Indicates that the "Change in LOP-C Condition" Interrupt has occurred since the last read of this register.
			Note: The user can determine the current state of AIS-C by reading out the contents of the "Receive STS-3c Path – LOP-C Status" Register (Address Locations: 0x11AB).
4	Detection of AIS Pointer	RUR	Detection of AIS Pointer Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of AIS Pointer" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate this interrupt anytime it detects an "AIS Pointer" in the incoming STS-3c data stream.
			Note: An "AIS Pointer" is defined as a condition in which both the H1 and H2 bytes (within the TOH) are each set to an "All Ones" pattern.
			0 - Indicates that the 'Detection of AIS Pointer" interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Detection of AIS Pointer" interrupt has occurred since the last read of this register.
3	Detection of Pointer Change	RUR	Detection of Pointer Change Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Change" Interrupt has occurred since the last read of this register.
		.(0	If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt anytime it accepts a new pointer value (e.g., H1 and H2 bytes, in the TOH bytes).
		Ol 6.	0 – Indicates that the "Detection of Pointer Change" Interrupt has NOT occurred since the last read of this register.
	رين المارين	310	17 Indicates that the "Detection of Pointer Change" Interrupt has occurred since the last read of this register.
2	POH Capture Interrupt	RUR	Path Overhead Data Capture Interrupt Status:
	Status	181	This RESET-upon-READ bit-field indicates whether or not the "POH Capture" Interrupt has occurred since the last read of this register.
	The and the		If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt once the Z5 byte (e.g., the last POH byte) has been loaded into the POH Capture Buffer. The contents of the POH Capture Buffer will remain intact for one SONET frame period. Afterwards, the POH data, for the next SPE will be loaded into the "POH Capture" buffer.
			0 – Indicates that the "POH Capture" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "POH Capture" Interrupt has occurred since the last read of this register.
			Note: The user can obtain the contents of the POH, within the most recently received SPE by reading out the contents of address locations "0xN0D3" through "0xN0F3").
1	Change in TIM-P Condition Interrupt Status	RUR	Change in TIM-P (Trace Identification Mismatch) Condition Interrupt.

			This RESET-upon-READ bit-field indicates whether or not the "Change in TIM-P" Condition interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following events.
			If the TIM-P condition is declared.
			If the TIM-P condition is cleared.
			0 – Indicates that the "Change in TIM-P Condition" Interrupt has not occurred since the last read of this register.
			1 – Indicates that the "Change in TIM-P Condition" Interrupt has occurred since the last read of this register.
0	Change in J1 Unstable Condition Interrupt Status	RUR	Change in "J1 (Trace Identification Message) Unstable Condition" Interrupt Status:
			This RESET-upon-READ bit-field indicates whether or not the "Change in J1 Unstable Condition" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following events.
			When the Receive STS-3c POH Processor block declare the "J1 Unstable" Condition.
		.0	When the Receive STS-3c POH Processor block clears the "J1 Unstable" condition.
		odu	0 Indicates that the "Change in J1 Unstable Condition" Interrupt has NOT occurred since the last read of this register.
	. 6	610	1 Indicates that the "Change in J1 Unstable Condition" Interrupt has occurred since the last read of this register.
	The product of and may	hotbe	

sperience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 711: Receive STS-3c Path – SONET Receive Path Interrupt Status – Byte 1 (Address Location= 0x118A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
New J1 Message Interrupt Status	Detection of REI-P Event Interrupt Status	Change in UNEQ-P Condition Interrupt Status	Change in PLM-P Condition Interrupt Status	New C2 Byte Interrupt Status	Change in C2 Byte Unstable Condition Interrupt Status	Change in RDI-P Unstable Condition Interrupt Status	New RDI-P Value Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	Description
7	NEW J1 Message	RUR	New J1 (Trace Identification) Message Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "New J1 Message" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt anytime it has accepted (or validated) and new J1 (Trace Identification) Message.
			0 – Indicates that the "New J1 Message" Interrupt has NOT occurred since the last read of this register.
			1 - Indicates that the "New 11 Message" Interrupt has occurred since the last read of this register.
6	Detection of REI-P	RUR	Detection of REI-P Event Interrupt Status:
	Event Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of REI-P Event" Interrupt has occurred since the last read of this register.
		Ž	If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt anytime it detects an REI-P condition in the coming STS-3c data-stream.
		odu	0 – Indicates that the "Detection of REI-P Event" Interrupt has NOT occurred since the last read of this register.
	ne (1 Indicates that the "Detection of REI-P Event" Interrupt has occurred since the last read of this register.
5	Change in UNEQ-	RUR	Change in UNEQ-P (Path – Unequipped) Condition Interrupt Status:
	P Condition Interrupt Status	all	This RESET-upon-READ bit-field indicates whether or not the "Change in UNEQ-P Condition" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following conditions.
			When the Receive STS-3c POH Processor block declares the UNEQ-P Condition.
			When the Receive STS-3c POH Processor block clears the UNEQ-P Condition.
			0 – Indicates that the "Change in UNEQ-P Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in UNEQ-P Condition" Interrupt has occurred since the last read of this register.
			Note:

r	ı		
			 The user can determine the current state of UNEQ-P by reading out the state of Bit 5 (UNEQ-P Defect Declared) within the "Receive STS-3c Path – SONET Receive POH Status – Byte 0" Register.
			2. The Address Location of the Receive STS-3c Path – SONET Receive POH Status – Byte 0" Registers is 0x1187
4	Change in PLM-P Condition Interrupt	RUR	Change in PLM-P (Path - Payload Mismatch) Condition Interrupt Status:
	Status		This RESET-upon-READ bit indicates whether or not the "Change in PLM-P Condition" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following conditions.
			When the Receive STS-3c POH Processor block declares the "PLM-P" Condition.
			When the Receive STS-3c POH Processor block clears the "PLM-P" Condition.
			0 - Indicates that the "Change in PLM-P Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in PLM-P Condition" Interrupt has occurred since the last read of this register.
3	New C2 Byte	RUR	New C2 Byte Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "New C2 Byte" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt anytime it has accepted a new C2 byte.
			0 - Indicates that the "New C2 Byte" Interrupt has NOT occurred since the last read of this register.
		O	1 - Indicates that the "New C2 Byte" Interrupt has occurred since the last read of this register.
2	Change in C2 Byte	RUR	Change in C2 Byte Unstable Condition Interrupt Status:
	Unstable Condition Interrupt Status	heet	This RESET-upon-READ bit-field indicates whether or not the "Change in C2 Byte Unstable Condition" Interrupt has occurred since the last read of this register.
	The to	2,43	If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following events.
	80	10	• When the Receive STS-3c POH Processor block declares the "C2 Byte Unstable" condition.
			• When the Receive STS-3c POH Processor block clears the "C2 Byte Unstable" condition.
			0- Indicates that the "Change in C2 Byte Unstable Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in C2 Byte Unstable Condition" Interrupt has occurred since the last read of this register.
			Note:
			1. The user can determine the current state of "C2 Byte Unstable Condition" by reading out the state of Bit 6 (C2 Byte Unstable Condition) within the "Receive STS-3c Path – SONET Receive POH Status – Byte 0" Register.
			2. The Address Location of the Receive STS-3c Path – SONET Receive POH Status – Byte 0" Register is 0x1187

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

1	Change in RDI-P Unstable Condition	RUR	Change in RDI-P Unstable Condition Interrupt Status:
	Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Change in RDI-P Unstable Condition" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following conditions.
			When the Receive STS-3c POH Processor block declares an "RDI-P Unstable" condition.
			When the Receive STS-3c POH Processor block clears the "RDI-P Unstable" condition.
			0 – Indicates that the "Change in RDI-P Unstable Condition" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in RDI-P Unstable Condition" Interrupt has occurred since the last read of this register.
			Note:
			1. The user can determine the current state of "RDI-P Unstable" by reading out the state of Bit 2 (RDI-P Unstable Condition) within the "Receive STS-3c Path – SONET Receive POH Status – Byte 0" Register.
			2. The Address Location of the Receive STS-3c Path – SONET Receive POH Status – Byte 0" Register is 0x1187
0	New RDI-P Value Interrupt Status	RUR	New RDI-P Value Interrupt Status: This RESET-upon-READ bit field indicates whether or not the "New RDI-P Value" interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate this interrupt anytime it receives and "validates" a new RDI-P value.
			0 - Indicates that the "New RDI-P Value" Interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "New RDI-P Value" Interrupt has occurred since the last read of this register.
		900	Note:
	the	ato a	1. The user can obtain the "New RDI-P Value" by reading out the contents of the "RDI-P ACCEPT[2:0]" bit-fields. These bit-fields are located in Bits 6 through 4, within the "Receive STS-3c Path – SONET Receive RDI-P Register".
	. 6	and	2. The Address Location of the Receive STS-3c Path – SONET Receive POH Status – Byte 0" Register is 0x1193

Table 712: Receive STS-3c Path – SONET Receive Path Interrupt Status – Byte 0 (Address Location= 0x118B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Detection of B3 Byte Error Interrupt Status	Detection of New Pointer Interrupt Status	Detection of Unknown Pointer Interrupt Status	Detection of Pointer Decrement Interrupt Status	Detection of Pointer Increment Interrupt Status	Detection of NDF Pointer Interrupt Status	Change of LOP-P Condition Interrupt Status	Change of AIS-P Condition Interrupt Status
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Detection of B3	RUR	Detection of B3 Byte Error Interrupt Status:
	Byte Error Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of B3 Byte Error" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt anytime it detects a B3 byte error in the incoming STS-3c data stream.
			0 – Indicates that the "Detection of B3 Byte Error" Interrupt has NOT occurred since the last read of this interrupt.
			1 – Indicates that the "Detection of B3 Byte Error" Interrupt has occurred since the last read of this interrupt.
6	Detection of	RUR	Detection of New Pointer Interrupt Status:
	New Pointer Interrupt Status		This RESET-upon-READ indicates whether the "Detection of New Pointer Interrupt has occurred since the last read of this register.
		do	If the user enables this interrupt, then the Receive STS-3c POH Processor block will generate an interrupt anytime it detects a new pointer value in the incoming STS-3c frame.
		170 6	Note: Pointer Adjustments with NDF will not generate this interrupt.
	4	o lest	Indicates that the "Detection of New Pointer" Interrupt has NOT occurred since the last read of this register.
	Theol	s, Way	1 – Indicates that the "Detection of New Pointer" Interrupt has occurred since the last read of this register.
5	Detection of	RUR	Detection of Unknown Pointer Interrupt Status:
	Unknown Pointer Interrupt Status	%	This RESET-upon-READ bit-field indicates whether or not the "Detection of Unknown Pointer" interrupt has occurred since the last read of this register.
			If the user enables this interrupt, then the Receive STS-3c POH Processor block will generate an interrupt anytime that it detects a "pointer" that does not fit into any of the following categories.
			An Increment Pointer
			A Decrement Pointer
			An NDF Pointer
			An AIS (e.g., All Ones) Pointer
			New Pointer
			0 - Indicates that the "Detection of Unknown Pointer" interrupt has NOT

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			occurred since the last read of this register.
			-
			1 – Indicates that the "Detection of Unknown Pointer" interrupt has occurred since the last read of this register.
4	Detection of	RUR	Detection of Pointer Decrement Interrupt Status:
	Pointer Decrement Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Decrement" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt anytime it detects a "Pointer Decrement" event.
			0- Indicates that the "Detection of Pointer Decrement" interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Detection of Pointer Decrement" interrupt has occurred since the last read of this register.
3	Detection of	RUR	Detection of Pointer Increment Interrupt Status:
	Pointer Increment Interrupt Status		This RESET-upon-READ bit-field indicates whether or not the "Detection of Pointer Increment" Interrupt has occurred since the last read of this register.
			If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt anytime it detects a "Pointer Increment" event.
			0 – Indicates that the "Detection of Pointer Increment" interrupt has NOT occurred since the last read of this register.
			Indicates that the "Detection of Pointer Increment" interrupt has occurred since the last read of this register.
2	Detection of NDF Pointer	RUR	Detection of NDF Pointer Interrupt Status:
	Interrupt Status	*	This RESET-upon-READ bit-field indicates whether or not the "Detection of NDF Pointer" interrupt has occurred since the last read of this register. If the user enables this interrupt, then the Receive STS-3c POH Processor block will generate an interrupt anytime it detects an NDF Pointer event.
		duc	0 Indicates that the "Detection of NDF Pointer" interrupt has NOT occurred since the last read of this register.
		Proshe	1 — Indicates that the "Detection of NDF Pointer" interrupt has occurred since the last read of this register.
1	Change of LOP	RUR	Change of LOP-P Condition Interrupt Status:
	P Condition Interrupt Status	go and	This RESET-upon-READ bit-field indicates whether or not the "Change in LOP-P Condition" interrupt has occurred since the last read of this register.
			If the user enables this interrupt, then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following events.
			 When the Receive STS-3c POH Processor block declares the "Loss of Pointer" defect.
			 When the Receive "STS-3c POH Processor" block clears the "Loss of Pointer" defect.
			0 - Indicates that the "Change in LOP-P Condition" interrupt has NOT occurred since the last read of this register.
			1 – Indicates that the "Change in LOP-P Condition" interrupt has occurred since the last read of this register.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM I	I KEGIS I EKS
--	---------------

state of Bit 1 (LOP-P Defect Declared) within the "Receive STS-3c Path SONET Receive POH Status – Byte 0" Register. 2. The Address Location of the "Receive STS-3c Path – SONET Receiped POH Status – Byte 0" Register is 0x1187 O Change of AIS-P Condition Interrupt Status: This RESET-upon-READ bit-field indicates whether or not the "Change AIS-P Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-3c POH Processor blowill generate an interrupt in response to either of the following events. When the Receive STS-3c POH Processor block declares an AIS condition. When the Receive STS-3c POH Processor block clears the AIS condition. Indicates that the "Change of AIS-P Condition" Interrupt has Not occurred since the last read of this register. I – Indicates that the "Change of AIS-P Condition" Interrupt has occurred since the last read of this register. Note: The user can determine the current state of AIS-P by reading out to state of Bit 0 (AIS-P Defect Declared) within the "Receive STS-3c Path SONET Receive POH Status – Byte 0" Register.			Note:
POH Status – Byte 0" Register is 0x1187 Change of AIS-P Condition Interrupt Status: P Condition Interrupt Status RUR P Condition Interrupt Status This RESET-upon-READ bit-field indicates whether or not the "Change AIS-P Condition" Interrupt has occurred since the last read of this register If this interrupt is enabled, then the Receive STS-3c POH Processor blowill generate an interrupt in response to either of the following events. When the Receive STS-3c POH Processor block declares an AIS condition. When the Receive STS-3c POH Processor block clears the AIS condition. Indicates that the "Change of AIS-P Condition" Interrupt has NO occurred since the last read of this register. I - Indicates that the "Change of AIS-P Condition" Interrupt has occurred since the last read of this register. Note: 1. The user can determine the current state of AIS-P by reading out the state of Bit 0 (AIS-P Defect Declared) within the "Receive STS-3c Path SONET Receive POH Status - Bute 0" Register.			1. The user can determine the current state of LOP-P by reading out the state of Bit 1 (LOP-P Defect Declared) within the "Receive STS-3c Path – SONET Receive POH Status – Byte 0" Register.
P Condition Interrupt Status This RESET-upon-READ bit-field indicates whether or not the "Change AIS-P Condition" Interrupt has occurred since the last read of this registed. If this interrupt is enabled, then the Receive STS-3c POH Processor blow will generate an interrupt in response to either of the following events. • When the Receive STS-3c POH Processor block declares an AIS condition. • When the Receive STS-3c POH Processor block clears the AIS condition. 0 - Indicates that the "Change of AIS-P Condition" Interrupt has NO occurred since the last read of this register. 1 - Indicates that the "Change of AIS-P Condition" Interrupt has occurred since the last read of this register. Note: 1. The user can determine the current state of AIS-P by reading out the state of Bit 0 (AIS-P Defect Declared) within the "Receive STS-3c Path SONET Receive POH Status - Byte 0" Register.			2. The Address Location of the "Receive STS-3c Path – SONET Receive POH Status – Byte 0" Register is 0x1187
Interrupt Status This RESET-upon-READ bit-field indicates whether or not the "Change AIS-P Condition" Interrupt has occurred since the last read of this register. If this interrupt is enabled, then the Receive STS-3c POH Processor blowill generate an interrupt in response to either of the following events. When the Receive STS-3c POH Processor block declares an AIS condition. When the Receive STS-3c POH Processor block clears the AIS condition. Indicates that the "Change of AIS-P Condition" Interrupt has NO occurred since the last read of this register. Indicates that the "Change of AIS-P Condition" Interrupt has occurred the last read of this register. Note: In The user can determine the current state of AIS-P by reading out the state of Bit O (AIS-P Defect Declared) within the "Receive STS-3c Path Son/ET Raceive POH Status - Bute O" Register.	0	RUR	Change of AIS-P Condition Interrupt Status:
will generate an interrupt in response to either of the following events. • When the Receive STS-3c POH Processor block declares an AIS condition. • When the Receive STS-3c POH Processor block clears the AIS condition. 0 – Indicates that the "Change of AIS-P Condition" Interrupt has NO occurred since the last read of this register. 1 – Indicates that the "Change of AIS-P Condition" Interrupt has occurred since the last read of this register. Note: 1. The user can determine the current state of AIS-P by reading out the state of Bit 0 (AIS-P Defect Declared) within the "Receive STS-3c Path SONET Receive POH Status – Bute 0" Register.			This RESET-upon-READ bit-field indicates whether or not the "Change of AIS-P Condition" Interrupt has occurred since the last read of this register.
condition. • When the Receive STS-3c POH Processor block clears the AIS condition. 0 – Indicates that the "Change of AIS-P Condition" Interrupt has NO occurred since the last read of this register. 1 – Indicates that the "Change of AIS-P Condition" Interrupt has occurred since the last read of this register. Note: 1. The user can determine the current state of AIS-P by reading out the state of Bit O (AIS-P Defect Declared) within the "Receive STS-3c Path SONET Receive POH Status — Bute O" Register.			If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following events.
condition. 0 – Indicates that the "Change of AIS-P Condition" Interrupt has NO occurred since the last read of this register. 1 – Indicates that the "Change of AIS-P Condition" Interrupt has occurred since the last read of this register. Note: 1. The user can determine the current state of AIS-P by reading out the state of Bit 0 (AIS-P Defect Declared) within the "Receive STS-3c Path SONET Receive POH Status - Bute 0" Register.			When the Receive STS-3c POH Processor block declares an AIS-P condition.
occurred since the last read of this register. 1 – Indicates that the "Change of AIS-P Condition" Interrupt has occurred since the last read of this register. Note: 1. The user can determine the current state of AIS-P by reading out the state of Bit 0 (AIS-P Defect Declared) within the "Receive STS-3c Path SONET Receive POH Status - Bute 0" Register.			When the Receive STS-3c POH Processor block clears the AIS-P condition.
since the last read of this register. Note: 1. The user can determine the current state of AIS-P by reading out to state of Bit 0 (AIS-P Defect Declared) within the "Receive STS-3c Path SONET Receive POH Status - Bute 0" Register.			0 - Indicates that the "Change of AIS-P Condition" Interrupt has NOT occurred since the last read of this register.
The user can determine the current state of AIS-P by reading out to state of Bit 0 (AIS-P Defect Declared) within the "Receive STS-3c Path SONET Receive POH Status – Byte 0" Register.			1 – Indicates that the "Change of AIS-P Condition" Interrupt has occurred since the last read of this register.
state of Bit 0 (AIS-P Defect Declared) within the "Receive STS-3c Path			Note:
2. The Address Location of the Receive STS-3c Path – SONET Receiped Political Address Location of the Receive STS-3c Path – SONET Receiped Political Address Location of the Receive STS-3c Path – SONET Receiped Political Address Location of the Receive STS-3c Path – SONET Receiped Political Address Location of the Receive STS-3c Path – SONET Receiped Political Address Location of the Receive STS-3c Path – SONET Receiped Political Address Location of the Receive STS-3c Path – SONET Receiped Political Address Location of the Receive STS-3c Path – SONET Receiped Political Address Location of the Receive STS-3c Path – SONET Receiped Political Address Location of the Receive STS-3c Path – SONET Receiped Political Address Location of the Receive STS-3c Path – SONET Receiped Political Address Location of the Receive STS-3c Path – SONET Receiped Political Address Location of the Receive STS-3c Path – SONET Receiped Political Address Location of the Receive STS-3c Path – SONET Receiped Political Address Location of the Receive STS-3c Path – SONET Receiped Political Address Location of the Receive STS-3c Path – SONET Receiped Political Address Location of the Receive STS-3c Path – SONET Receiped Political Address Location of the Receive STS-3c Path – SONET Receiped Political Address Location of the Receip			1. The user can determine the current state of AIS-P by reading out the state of Bit 0 (AIS-P Defect Declared) within the "Receive STS-3c Path – SONET Receive POH Status – Byte 0" Register.
The product or proto lordere			2. The Address Location of the Receive STS-3c Path – SONET Receive POH Status – Byte 0" Registers is 0x1187



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 713: Receive STS-3c Path – SONET Receive Path Interrupt Enable – Byte 2 (Address Location= 0x118D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
New K3 Byte Interrupt Enable	Change in AIS-C Condition Interrupt Enable	Change in LOP-C Condition Interrupt Enable	Detection of AIS Pointer Interrupt Enable	Detection of Pointer Change Interrupt Enable	POH Capture Interrupt Enable	Change in TIM-P Condition Interrupt Enable	Change in J1 Unstable Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	New K3 Byte Interrupt Enable	R/W	New K3 Byte Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "New K3 Byte" Interrupt. If this interrupt is enabled, then the Receive SONET POH Processor block will generate an interrupt anytime it has accepted (or validated) and new K3 Byte. 0 – Disables the "New K3 Byte" Interrupt. 1 – Enables the "New K3 Byte" Interrupt.
6	Change in AIS-C Condition Interrupt Enable	R/W	Change in AlS-C (AlS Concatenation) Condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change in AIS-C Condition" Interrupt. If this interrupt is enabled, then an interrupt will generated in response to either of the following events. a. Whenever the Receive STS-3c POH Processor block declares an AIS-C condition with one of the STS-1 signals; within the incoming STS-3c signal. b. Whenever the Receive STS-3c POH Processor block clears the AIS-C condition with one of the STS-1 signals; within the incoming STS-3c signal. 0 – Disables the "Change in AIS-C Condition" Interrupt. 1 – Enables the "Change in AIS-C Condition" Interrupt Note: This bit-field is only valid if the XRT94L33 is receiving an STS-3 signal that contains one or more STS-3c signals. This bit-field is only valid for the following Address Locations: "0x118D" (for STS-3c)
5	Change in LOP-C Condition Interrupt Enable	R/W	Change in LOP-C (Loss of Pointer - Concatenation) Condition Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Change in LOP-C Condition" Interrupt. If this interrupt is enabled, then an interrupt will generated in response to either of the following events. a. Whenever the Receive STS-3c POH Processor block declares an LOP-C condition with one of the STS-1 signals;

	T		within the incoming CTC 2e cianal
			within the incoming STS-3c signal.
			 Whenever the Receive STS-3c POH Processor block clears the LOP-C condition with one of the STS-1 signals; within the incoming STS-3c signal.
			0 – Disables the "Change in LOP-C Condition" Interrupt.
			1 – Enables the "Change in LOP-C Condition" Interrupt
			Note:
			This bit-field is only valid if the XRT94L33 is receiving an STS-3 signal that contains one or more STS-3c signals.
			This bit-field is only valid for the following Address Locations: "0x118D" (for STS-3c)
4	Detection of AIS Pointer	R/W	Detection of AIS Pointer Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of AIS Pointer" interrupt.
			If the user enables this interrupt, then the Receive STS-3c POH Processor block will generate an interrupt anytime it detects an "AIS Pointer", in the incoming STS-3c data stream.
			Note: An "AIS Pointer" is defined as a condition in which both the H1 and H2 bytes (within the TOH) are each set to an "All Ones" Pattern.
			0 - Disables the "Detection of AIS Pointer" Interrupt.
			1 – Enables the "Detection of AIS Pointer" Interrupt.
3	Detection of Pointer	R/W	Detection of Pointer Change Interrupt Enable:
	Change Interrupt Enable	30	This READWRITE bit-field permits the user to either enable or disable the "Detection of Pointer Change" Interrupt.
	N. C.	orpr	If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt anytime it has accepted a new pointer value.
	,,,(0)	. 2	O Disables the "Detection of Pointer Change" Interrupt.
	, odk	s, 10	1 – Enables the "Detection of Pointer Change" Interrupt.
2	POH Capture Interrupt Enable	R/W	Path Overhead Data Capture Interrupt Enable:
	Enable		This READ/WRITE bit-field permits the user to either enable or disable the "POH Capture" Interrupt.
	and		If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt once the Z5 byte (e.g., the last POH byte) has been loaded into the POH Capture Buffer. The contents of the POH Capture Buffer will remain intact for one SONET frame period. Afterwards, the POH data for the next SPE will be loaded into the "POH Capture" Buffer.
			0 - Disables the "POH Capture" Interrupt
			1 – Enables the "POH Capture" Interrupt.
1	Change in TIM-P Condition Interrupt	R/W	Change in TIM-P (Trace Identification Mismatch) Condition Interrupt:
	Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in TIM-P Condition" interrupt.
			If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

			ayanta				
			events.				
			If the TIM-P condition is declared.				
			If the TIM-P condition is cleared.				
			0 – Disables the "Change in TIM-P Condition" Interrupt.				
			1 – Enables the "Change in TIM-P Condition" Interrupt.				
0	Change in J1 Unstable Condition Interrupt	R/W	Change in "J1 (Trace Identification Message) Unstable Condition" Interrupt Status:				
	Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in J1 (Trace Identification) Message Unstable Condition" Interrupt.				
			If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following events.				
			When the Receive STS-3c POH Processor block declares the "J1 Unstable" Condition.				
			When the Receive STS-36 POH Processor block clears the "J1 Unstable" Condition.				
			0 - Disables the "Change in J1 Message Unstable Condition" interrupt.				
			1 - Enables the "Change in J1 Message Unstable Condition" interrupt.				
	1 – Enables the "Change in J1 Message Unstable Condition" interrupt.						

Table 714: Receive STS-3c Path – SONET Receive Path Interrupt Enable – Byte 1 (Address Location= 0x118E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
New J1 Message Interrupt Enable	Detection of REI-P Event Interrupt Enable	Change in UNEQ-P Condition Interrupt Enable	Change in PLM-P Condition Interrupt Enable	New C2 Byte Interrupt Enable	Change in C2 Byte Unstable Condition Interrupt Enable	Change in RDI-P Unstable Condition Interrupt Enable	New RDI-P Value Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	NEW J1	R/W	New J1 (Trace Identification) Message Interrupt Enable:
	Message Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "New J1 Message" Interrupt
			If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt anytime it has accepted (or validated) and new J1 (Trace Identification) Message.
			0 - Disables the "New J1 Message" Interrupt.
			1 – Enables the "New J1 Message" Interrupt.
6	Detection of	R/W	Detection of REI-P Event Interrupt Enable:
	REI-P Event Interrupt Enable		This READ WRITE bit-field permits the user to either enable or disable the "Detection of REI-P Event" Interrupt.
		101	If this interrupt is enabled, then he Receive STS-3c POH Processor block will generate an interrupt anytime it detects an REI-P condition in the coming STS-3c data-stream.
			6 – Disables the "Detection of REI-P Event" Interrupt.
		AUG K	1 - Enables the "Detection of REI-P Event" Interrupt.
5	Change in	R/W	Change in UNEQ-P (Path – Unequipped) Condition Interrupt Enable:
	UNEQ-P Condition		This READ/WRITE bit-field permits the user to either enable or disable the "Change in UNEQ-P Condition" interrupt.
	11,99		If this interrupt is enabled , then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following conditions.
			When the Receive STS-3c POH Processor block declares the UNEQ-P Condition.
			When the Receive STS-3c POH Processor block clears the UNEQ-P Condition.
			0 – Disables the "Change in UNEQ-P Condition" Interrupt.
			1 – Enables the "Change in UNEQ-P Condition" Interrupt.
4	Change in PLM-P Condition	R/W	Change in PLM-P (Path – Payload Mismatch) Condition Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit permits the user to either enable or disable the "Change in PLM-P Condition" interrupt.
			If this interrupt is enabled, then the Receive STS-3c POH Processor block

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

	_	ı	
			will generate an interrupt in response to either of the following conditions.
			When the Receive STS-3c POH Processor block declares the "PLM-P" Condition.
			When the Receive STS-3c POH Processor block clears the "PLM-P" Condition.
			0 – Disables the "Change in PLM-P Condition" Interrupt.
			1 – Enables the "Change in PLM-P Condition" Interrupt.
3	New C2 Byte	R/W	New C2 Byte Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "New C2 Byte" Interrupt.
			If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt anytime it has accepted a new C2 byte.
			0 – Disables the "New C2 Byte" Interrupt.
			1 – Enables the "New C2 Byte" Interrupt:
			Note:
			1. The user can obtain the value of this "New C2" byte by reading the contents of the "Receive STS 3c Path – Received Path Label Value" Register.
			2. The Address Location of the Receive STS-3c Path – Received Path Label Value" Register is 0x1196
2	Change in C2	R/W	Change in C2 Byte Unstable Condition Interrupt Enable:
	Byte Unstable Condition Interrupt Enable		This READ/WRITE bit field permits the user to either enable or disable the "Change in C2 Byte Unstable Condition" Interrupt.
			If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following events.
		Š.	• When the Receive STS-3c POH Processor block declares the "C2 Byte Unstable" condition.
		odule	When the Receive STS-3c POH Processor block clears the "C2 Byte Unstable" condition.
		6, 24,	0+ Disables the "Change in C2 Byte Unstable Condition" Interrupt.
	10	NO C	- Enables the "Change in C2 Byte Unstable Condition" Interrupt.
1	Change in RDI-	R/W	Change in RDI-P Unstable Condition Interrupt Enable:
	P Unstable Condition Interrupt Enable	2	This READ/WRITE bit-field permits the user to either enable or disable the "Change in RDI-P Unstable Condition" interrupt.
			If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following conditions.
			When the Receive STS-3c POH Processor block declares an "RDI-P Unstable" condition.
			When the Receive STS-3c POH Processor block clears the "RDI-P Unstable" condition.
			0 – Disables the "Change in RDI-P Unstable Condition" Interrupt.
			1 – Enables the "Change in RDI-P Unstable Condition" Interrupt.
0	New RDI-P Value Interrupt Enable	R/W	New RDI-P Value Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "New RDI-P Value" interrupt.
	İ	1	ı

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

If this interrupt is enabled, then the Receive STS-3c POH Processor block will generate this interrupt anytime it receives and "validates" a new RDI-P value.
0 – Disables the "New RDI-P Value" Interrupt.
1 – Enable the "New RDI-P Value" Interrupt.

The product are no products man to be ordered (OBS)



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 715: Receive STS-3c Path – SONET Receive Path Interrupt Enable – Byte 0 (Address Location= 0x118F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Detection of B3 Byte Error Interrupt Enable	Detection of New Pointer Interrupt Enable	Detection of Unknown Pointer Interrupt Enable	Detection of Pointer Decrement Interrupt Enable	Detection of Pointer Increment Interrupt Enable	Detection of NDF Pointer Interrupt Enable	Change of LOP-P Condition Interrupt Enable	Change of AIS-P Condition Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	Description >
7	Detection of B3	R/W	Detection of B3 Byte Error Interrupt Enable:
	Byte Error Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of B3 Byte Error" Interrupt. If the user enables this interrupt, then the Receive STS-3c POH Processor block will generate an interrupt anytime it detects a B3-byte error in the incoming STS-3c data-stream.
			0 – Disables the "Detection of B3 Byte Error" interrupt.
			1 – Enables the "Detection of B3 Byte Error" interrupt.
6	Detection of New Pointer Interrupt Enable	R/W	Detection of New Pointer Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Detection of New Pointer" interrupt. If the user enables this interrupt, then the Receive STS 3c POH Processor block will generate an interrupt anytime it detects a new pointer value in the incoming STS-3c frame. Note: Pointer Adjustments with NDF will not generate this interrupt.
		, c'	0 – Disables the "Detection of New Pointer" Interrupt. 1 Enables the "Detection of New Pointer" Interrupt.
5	Detection of Unknown Pointer Interrupt Enable	Programme Asia Asia Asia Asia Asia Asia Asia Asia	Detection of Unknown Pointer Interrupt Enable: This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Unknown Pointer" interrupt. If the user enables this interrupt, then the Receive STS-3c POH Processor block will generate an interrupt anytime it detects a "Pointer Adjustment" that does not fit into any of the following categories.
		2	An Increment Pointer.
			A Decrement Pointer
			An NDF Pointer
			AIS Pointer
			New Pointer.
			0 - Disables the "Detection of Unknown Pointer" Interrupt.
			1 – Enables the "Detection of Unknown Pointer" Interrupt.
4	Detection of Pointer Decrement Interrupt Enable	R/W	Detection of Pointer Decrement Interrupt Enable: This READ/WRITE bit-field permits the user to enable or disable the "Detection of Pointer Decrement" Interrupt. If the user enables this interrupt, then the Receive STS-3c POH Processor block will generate an

<u></u>	T	1	
			interrupt anytime it detects a "Pointer-Decrement" event.
			0 – Disables the "Detection of Pointer Decrement" Interrupt.
			1 – Enables the "Detection of Pointer Decrement" Interrupt.
3	Detection of	R/W	Detection of Pointer Increment Interrupt Enable:
	Pointer Increment Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of Pointer Increment" Interrupt. If the user enables this interrupt, then the Receive STS-3c POH Processor block will generate an interrupt anytime it detects a "Pointer Increment" event.
			0 – Disables the "Detection of Pointer Increment" Interrupt.
			1 – Enables the "Detection of Pointer Increment" Interrupt.
2	Detection of NDF	R/W	Detection of NDF Pointer Interrupt Enable:
	Pointer Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Detection of NDF Pointer" interrupt. If the user enables this interrupt, then the Receive STS-3c POH Processor block will generate an interrupt anytime it detects an NDF Pointer event.
			0 – Disables the "Detection of NDF Pointer" interrupt.
			1 – Enables the "Detection of NDF Pointer" interrupt.
1	Change of LOP-	R/W	Change of LOP-P Condition Interrupt Enable:
	P Condition Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change in LOP (Loss of Pointer)" Condition interrupt. If the user enables this interrupt, then the Receive STS-3c POH Processor will generate an interrupt in response to either of the following events. a. When the Receive STS-3c POH Processor block declares a "Loss of Pointer" condition.
			b When the Receive STS-3c POH Processor block clears the "Loss of Pointer" condition.
		16	0 Disable the "Change of LOP-P Condition" Interrupt.
		duction	1 – Enables the "Change of LOP-P Condition" Interrupt. Note:
	ise pr	sheed	The user can determine the current state of "LOP-P" by reading out the contents of Bit 1 (LOP-P) within the "Receive STS-3c Path – SONET Receive POH Status – Byte 0".
	11,981	nd	2. The Address Location of the Receive STS-3c Path – SONET Receive POH Status Byte 0" Register is 0x1187
0	Change of AIS-P	R/W	Change of AIS-P Interrupt Enable:
	Interrupt Enable		This READ/WRITE bit-field permits the user to either enable or disable the "Change of AIS-P (Path AIS)" interrupt. If the user enables this interrupt, then the Receive STS-3c POH Processor block will generate an interrupt in response to either of the following events.
			a. When the Receive STS-3c POH Processor block declares an "AIS-P" condition.
			b. When the Receive STS-3c POH Processor block clears the "AIS-P" condition.
			0 - Disables the "Change of AIS-P" Interrupt.
			1 – Enables the "Change of AIS-P" Interrupt.
			Note:
			1. The user can determine the current state of "AIS-P" by reading out the

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

contents of Bit 0 (AIS-P) within the "Receive STS-3c Path – SONET Receive POH Status – Byte 0" Register.
2. The Address Location of the Receive STS-3c Path – SONET Receive POH Status – Byte 0" Register is 0x1187

The product are no longered (OBS)

The product are no longered (OBS)

The product are no longered (OBS)

Table 716: Receive STS-3c Path – SONET Receive RDI-P Register (Address Location= 0x1193)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Unused	nused RDI-P_ACCEPT[2:0]			RDI-P THRESHOLD[3:0]				
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION		
7	Unused	R/O			
6 – 4	RDI- P_ACCEPT[2:0]	R/O	Accepted RDI-P Value: These READ-ONLY bit-fields contain the value of the most recently "accepted" RDI-P (e.g., bits 5, 6 and 7 within the G1 byte) value. Note: A given RDI-P value will be "accepted" by the Receive STS-3c POH Processor block, if this RDI-P value has been consistently received in "RDI-P THRESHOLD[3:0]" number of SONET frames.		
3-0	RDI-P THRESHOLD[3:0]	R/W	RDI-P Threshold: These READ/WRITE bit-fields permit the user to defined the "RDI-P Acceptance Threshold" for the Receive STS-3c POH Processor Block. The "RDI-P Acceptance Threshold" is the number of consecutive SONET frames, in which the Receive STS-3c POH Processor block must receive a given RDI-P value, before it "accepts" or "validates" it. The most recently "accepted" RDI-P value is written into the "RDI-P ACCEPT[2:0]" bit-fields, within this register.		
The most recently "accepted" RDI-P value is written into the "REACCEPT[2:0]" bit-fields, within this register.					

EXAR Experience Our Connectivit

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 717: Receive STS-3c Path – Received Path Label Value (Address Location= 0x1196)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
Received_C2_Byte_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O	
1	1	1	1	1	1	1	1	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Received C2 Byte	R/O	Received "Filtered" C2 Byte Value:
	Value[7:0]		These READ-ONLY bit-fields contain the value of the most recently "accepted" C2 byte, via the Receive STS-3c POH Processor block.
			The Receive STS-3c POH Processor block will "accept" a C2 byte value (and load it into these bit-fields) if it has received a consistent C2 byte, in five (5) consecutive SONET frames.
			Note:
			1. The Receive STS-3c POH Processor block uses this register, along the "Receive STS-3c Path – Expected Path Label Value" Register, when declaring or clearing the UNEQ-P and PLM-P alarm conditions.
			2. The Address Location of the Receive STS-3c Path – Expected Path Label Value" Register is 0x1197

Table 718: Receive STS-3c Path – Expected Path Label Value (Address Location= 0x1197)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Expected_C2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	(0, 1(, 0)	1	1	1	1

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Expected C2 Byte Value[7:0]	R/W	Expected C2 Byte Value:
	The data dina	3	These READ/WRITE bit-fields permits the user to specify the C2 (Path Label Byte) value, that the Receive STS-3c POH Processor block should expect when declaring or clearing the UNEQ-P and PLM-P alarm conditions.
	*		If the contents of the "Received C2 Byte Value[7:0]" (see "Receive STS-3c Path – Received Path Label Value" register) matches the contents in these register, then the Receive STS-3c POH will not declare any alarm conditions.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 719: Receive STS-3c Path - B3 Error Count Register - Byte 3 (Address Location= 0x1198)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	B3_Error_Count[31:24]									
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR			
0	0	0	0	0	0	0	0			

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	B3_Error_Count[31:24]	RUR	B3 Error Count – MSB:
			This RESET-upon-READ register, along with "Receive STS-3c Path – B3 Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3c POH Processor block detects a B3 byte error. Note: If the B3 Error Type is configured to be "bit errors", then the Receive STS-3c POH Processor block will increment this 32 bit counter by the number of bits, within the B3 value that are in error. If the B3 Error Type is configured to be "frame errors", then the Receive STS-3c POH Processor block will increment this 32 bit counter by the number of frames that contain erred B3 bytes.

Table 720: Receive STS-3c Path - B3 Error Count Register - Byte 2 (Address Location= 0x1199)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0
			B3_Error_C	ount[23:16]			
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0 0	000	0	0	0	0

BIT NUMBER	NAME TY	PE.	DESCRIPTION
7 – 0	B3_Error_Count[23:16] RL	JR	B3 Error Count (Bits 23 through 16):
	the data and man		This RESET-upon-READ register, along with "Receive STS-3c Path – B3 Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3c POH Processor block detects a B3 byte error. Note:
			If the B3 Error Type is configured to be "bit errors", then the Receive STS-3c POH Processor block will increment this 32 bit counter by the number of bits, within the B3 value that are in error.
			If the B3 Error Type is configured to be "frame errors", then the Receive STS-3c POH Processor block will increment this 32 bit counter by the number of frames that contain erred B3 bytes.

Table 721: Receive STS-3c Path - B3 Error Count Register - Byte 1 (Address Location= 0x119A)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	B3_Error_Count[15:8]								
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR		

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

^	^			^		^	
()	()	()	()	()	()	()	. ()
•	•			•		•	

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	B3_Error_Count[15:8]	RUR	B3 Error Count – (Bits 15 through 8):
			This RESET-upon-READ register, along with "Receive STS-3c Path – B3 Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3c POH Processor block detects a B3 byte error.
			Note:
			If the B3 Error Type is configured to be "bit errors", then the Receive STS-3c POH Processor block will increment this 32 bit counter by the number of bits, within the B3 value that are in error.
			If the B3 Error Type is configured to be "frame errors", then the Receive STS-3c POH Processor block will increment this 32 bit counter by the number of frames that contain erred B3 bytes.

Table 722: Receive STS-3c Path - B3 Error Count Register - Byte (Address Location= 0x119B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			B3_Error_	Count[7:0]			
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	3/10/0	0	0	0

BIT NUMBER	Name	Type Description
7 – 0	B3_Error_Count[7:0]	RUR B3 Error Count – LSB:
	HUS	This RESET-upon-READ register, along with "Receive STS-3c Path – B3 Error Count Register – Bytes 3 through 1; function as a 32 bit counter, which is incremented anytime the Receive STS-3c POH Processor block detects a B3 byte error.
	3000	Note:
	Theoris	If the B3 Error Type is configured to be "bit errors", then the Receive STS-3c POH Processor block will increment this 32 bit counter by the number of bits, within the B3 value that are in error.
	o and	If the B3 Error Type is configured to be "frame errors", then the Receive STS-3c POH Processor block will increment this 32 bit counter by the number of frames that contain erred B3 bytes.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 723: Receive STS-3c Path – REI-P Error Count Register – Byte 3 (Address Location= 0x119C)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0					
	REI_P_Error_Count[31:24]											
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR					
0	0	0	0	0	0	0	0					

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	REI_P_Error_Count[31:24]	RUR	REI-P Error Count – MSB:
			This RESET-upon-READ register, along with "Receive STS-3c Path – REI-P Error Count Register – Bytes 2 through 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3c POH Processor block detects a Path – Remote Error Indicator. Note: If the REI-P Error Type is configured to be "bit errors", then the Receive STS-3c POH Processor block will increment this 32 bit counter by the nibble-value within the REI-P field of the incoming G1 byte. If the REI-P Error Type is configured to be "frame errors", then the Receive STS-3c POH Processor block will increment this 32 bit counter by the number of frames that contain non-zero REI-P values:

Table 724: Receive STS-3c Path – REI_P Error Count Register – Byte 2 (Address Location= 0x119D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
			REI_P_Error_	Count[23:16]							
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR				
0	0	0 🜔	0 0	0	0	0	0				
	100										

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	REI_P_Error_Count[23:16]	RUR	REI-P Error Count (Bits 23 through 16):
	the plata driad		This RESET-upon-READ register, along with "Receive STS-3c Path – REI-P Error Count Register – Bytes 3, 1 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3c POH Processor block detects a Path – Remote Error Indicator.
	all		Note:
			If the REI-P Error Type is configured to be "bit errors", then the Receive STS-3c POH Processor block will increment this 32 bit counter by the nibble-value within the REI-P field of the incoming G1 byte.
			If the REI-P Error Type is configured to be "frame errors", then the Receive STS-3c POH Processor block will increment this 32 bit counter by the number of frames that contain non-zero REI-P values.

Table 725: Receive STS-3c Path – REI_P Error Count Register – Byte 1 (Address Location=0x119E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0					
	REI_P_Error_Count[15:8]											
RUR	RUR RUR RUR RUR RUR RUR RUR											

XRT94L33



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

ſ	Λ	0	0	0	Λ	0	0	0
	U	O	U	U	0	U	0	O

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	REI_P_Error_Count[15:8]	RUR	REI-P Error Count – (Bits 15 through 8)
			This RESET-upon-READ register, along with "Receive STS-3c Path – REI-P Error Count Register – Bytes 3, 2 and 0; function as a 32 bit counter, which is incremented anytime the Receive STS-3c POH Processor block detects a Path –Remote Error Indicator.
			Note:
			 If the REI-P Error Type is configured to be "bit errors", then the Receive STS-3c POH Processor block will increment this 32 bit counter by the nibble-value within the REI-P field of the incoming G1 byte. If the REI-P Error Type is configured to be "frame errors", then the Receive STS-3c POH Processor block will increment this 32 bit counter by the number of frames that contain non-zero REI-P values.

Table 726: Receive STS-3c Path – REI_P Error Count Register —Byte 0 (Address Location= 0x119F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			REI_P_Erro	r_Count[7:0]	3 1		
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER N	AME TYPE	DESCRIPTION
	ame Type or_Count[7:0] RUR	

Table 727: Receive STS-3c Path – Receive J1 Control Register (Address Location=0x11A3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused		New Message Ready	Receive J1 Message Buffer Read Select	Accept Threshold	Message Type	Message l	_ength[1:0]
R/O	R/O	R/O	R/W	R/W	R/W	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 5	Unused	R/O	
5	New Message	R/O	New Message Ready:
	Ready		This READ/WRITE bit-field indicates whether or not the J1 trace buffer has received a new expected value.
			0 – Indicates "NO" new expected value has been downloaded into the receive J1 trace buffer.
			1 – Indicates a new expected value has been downloaded into the receive J1 trace buffer.
4	Received J1	R/W	J1 Buffer Read Selection:
	Message Buffer Read Select		This READ/WRITE bit-field permits a user to specify which of the following buffer segments to read.
			a. Valid Message Buffer
			b Expected Message Buffer
			0 - Executing a READ to the Receive J1 Trace Buffer, will return contents within the "Valid Message" buffer.
		, ch	1 – Executing a READ to the Receive J1 Trace Buffer, will return contents within the Expected Message Buffer".
	ď	odule	Note: In the case of the Receive STS-3c POH Processor block, the "Receive J1 Trace Buffer" is located at Address Location = 0x1500 through 0x153F
3	Accept 🕜	R/W	Message Accept Threshold:
	Threshold	300	This READ/WRITE bit-field permits a user to select the number of consecutive times that the Receive STS-3c POH Processor block must receive a given J1 Trace Message, before it is accepted, as described below.
			0 – The Receive STS-3c POH Processor block accepts the J1 Message after it has received it the third time in succession.
			1 – The Receive STS-3c POH Processor block accepts the J1 Message after it has received in the fifth time in succession.
2	Message Type	R/O	Message Alignment Type:
			This READ/WRITE bit-field permits a user to specify have the Receive STS-3c POH Processor block will locate the boundary of the J1 Trace Message, as indicated below.
			0 – Message boundary is indicated by "Line Feed".
			1- Message boundary is indicated by the presence of a "1" in the MSB of a the first byte (within the J1 Trace Message).

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

1 – 0	Message	R/W	J1 Message Length[1:0]:							
	Length[1:0]		These READ/WRITE bit-fields permit the user to specify the length of the Trace Message, that the Receive STS-3c POH Processor block will receive The relationship between the content of these bit-fields and the corresponding J1 Trace Message Length is presented below.							
			MSG LENGTH Resulting J1 Trace Message Length							
			00	1 Byte						
			01	16 Bytes						
			10/11	64 Bytes						

The product are no ordered (OBS)

The product are no ordered (OBS)

The product are no ordered (OBS)

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 728: Receive STS-3c Path - Pointer Value - Byte 1 (Address Location= 0x11A6)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unused					Current_Pointer	Value MSB[9:8]
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 2	Unused	R/O	
1 – 0	Current_Pointer_Value_MSB[1:0]	R/O	Current Pointer Value – MSB:
			These READ-ONLY bit-fields, along with that from the "Receive STS-3c Path – Pointer Value – Byte 0" Register combine to reflect the current value of the pointer that the "Receive STS-3c POH Processor" block is using to locate the SPE within the incoming SONET data stream. Note: These register bits comprise the two-most significant bits of the Pointer Value.

Table 729: Receive STS-3c Path – Pointer Value – Byte 0 (Address Location=0x11A7)

Віт 7	Віт 6	Віт 5	Віт 4	⊘Віт.3	Віт 2	Віт 1	Віт 0
		C	Current_Pointer_	Value_LSB[7:0)]		
R/O	R/O	R/O	R/O C	R/O	R/O	R/O	R/O
0	0	0	000	0	0	0	0

BIT NUMBER	NAME TYP	DESCRIPTION
7 – 0	Current_Pointer_Value_LSB[7:0] R/C	Current Pointer Value – LSB: These READ-ONLY bit-fields, along with that from the "Receive STS-3c Path – Pointer Value – Byte 1" Register combine to reflect the current value of the pointer that the "Receive STS-3c POH Processor" block is using to locate the SPE within the incoming SONET data stream. Note: These register bits comprise the Lower Byte value
	o alle	of the Pointer Value.



3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 730: Receive STS-3c Path – LOP-C Status Register (Address Location=0x11AB)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
		Unused			LOP-C Status STS-1 # 3	LOP-C Status STS-1 # 2	Unused
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 3	Unused	R/O	
2	LOP-C Status - STS-1 # 3	R/O	Loss of Pointer – Concatenation Status – STS-1 # 3
			This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is declaring the LOP-C (Loss of Pointer – Concatenation) defect with STS-1 # 3 (within an STS-3c signal).
			The Receive STS-3c POH Processor block will declare the LOP-C condition, with STS-1 # 3; if it does not receive the "Concatenation Indicator" value of "0x93FF" in the H1, H2 bytes (associated with STS-1#3) for 8 consecutive SONET frames.
			0 – Indicates that the Receive STS-3c POH Processor block is NOT currently declaring the LOP-C condition with STS-1 # 3.
			1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-C condition with STS-1 # 3.
		~ C	Note: This bit-field is only valid if the XRT94L33 is receiving an STS-3 signal that contains one or more STS-3c signals.
1	LOP-C Status – STS-1 # 2	R/O	Loss of Pointer – Concatenation Status – STS-1 # 2
	dus	et ale	This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is declaring the LOP-C (Loss of Pointer – Concatenation) condition with STS-1 # 2 (within an STS-3c signal).
	The production of the producti	naynu	The Receive STS-3c POH Processor block will declare the LOP-C condition, with STS-1 # 2; if it does not receive the "Concatenation Indicator" value of "0x93FF" in the H1, H2 bytes (associated with STS-1 # 2) for 8 consecutive SONET frames.
	, go sho		0 – Indicates that the Receive STS-3c POH Processor block is NOT currently declaring the LOP-C condition with STS-1 # 2.
			1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the LOP-C condition with STS-1 # 2.
			Note: This bit-field is only valid if the XRT94L33 is receiving an STS-3 signal that contains one or more STS-3c signals.
0	Unused	R/O	

Table 731: Receive STS-3c Path – AIS-C Status Register (Address Location=0x11B3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused				AIS-C Status STS-1 # 3	AIS-C Status STS-1 # 2	Unused	
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 3	Unused	R/O	
2	AIS-C Status – STS-1 # 3	R/O	AIS – Concatenation Status – STS-1 # 3
			This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is declaring the LOP-C (AIS – Concatenation) condition with STS-1 # 3 (within an STS-3c signal).
			The Receive STS-3c POH Processor block will declare the AIS-C condition, with STS-1 # 3; if it receives an "All Ones" string; in the H1, H2 bytes (associated with STS-1 # 3) for 3 consecutive SONET trames.
			0 – Indicates that the Receive STS-3c POH Processor block is NOT currently declaring the AIS-C condition with STS-1 # 3.
			1 Indicates that the Receive STS-3c POH Processor block is currently declaring the AIS-C condition with STS-1 # 3.
		orodu	Note: This bit-field is only valid if the XRT94L33 is receiving an STS-3 signal that contains one or more STS-3c signals.
1	AIS-C Status – STS-1 # 2	R/O	AIS - Concatenation Status - STS-1 # 2
	duct	ale be	This READ-ONLY bit-field indicates whether or not the Receive STS-3c POH Processor block is declaring the AIS-C (Loss of Pointer – Concatenation) condition with STS-1 # 2 (within an STS-3c signal).
	AIS-C Status – STS-1 # 2	And	The Receive STS-3c POH Processor block will declare the AIS-C condition, with STS-1 # 2; if it receives an "All Ones" string in the H1, H2 bytes (associated with STS-1 # 2) for 3 consecutive SONET frames.
	, da and		0 – Indicates that the Receive STS-3c POH Processor block is NOT currently declaring the AIS-C condition with STS-1 # 2.
			1 – Indicates that the Receive STS-3c POH Processor block is currently declaring the AIS-C condition with STS-1 # 2.
			Note: This bit-field is only valid if the XRT94L33 is receiving an STS-3 signal that contains one or more STS-3c signals.
0	Unused	R/O	

perience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 732: Receive STS-3c Path – AUTO AIS Control Register (Address Location= 0x11BB)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused	Transmit AIS-P (Down- stream) Upon C2 Byte Unstable	Transmit AIS-P (Down- stream) Upon UNEQ-P	Transmit AIS-P (Down- stream) Upon PLM- P	Transmit AIS-P (Down- stream) Upon J1 Message Unstable	Transmit AIS-P (Down- stream) Upon TIM-P	Transmit AIS-P (Down- stream) upon LOP-P	Transmit AIS-P (Down- stream) Enable
R/O	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	Description
7	Unused	R/O	thille
6	Transmit AIS-P	R/W	Transmit Path AIS upon Detection of Unstable C2 Byte:
	(Downstream) upon C2 Byte Unstable		This READ/WRITE bit-field permits the user to configure the Receive STS-3c POH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive STS-3/STM-1 Telecom Bus Interface), anytime it detects an Unstable C2 Byte condition in the "incoming" STS-3c data-stream. 0 – Does not configure the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects an "Unstable C2 Byte" condition.
			1 – Configures the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects an "Unstable C2 Byte" condition.
		ct of	Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
5	Transmit AIS-P (Downstream) upon UNEQ-P	R/W	Transmit Path AIS upon Detection of Path-Unequipped Defect (UNEQ-P):
	UNEQ-P OF	dnay	This READ/WRITE bit-field permits the user to configure the Receive STS-3c POH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive STS-3/STM-1 Telecom Bus Interface), anytime it declares an UNEQ-P condition.
	*		0 – Does not configure the Receive STS-3c POH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the UNEQ-P defect.
			1 – Configures the Receive STS-3c POH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the UNEQ-P defect.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
4	Transmit AIS-P (Downstream) upon	R/W	Transmit Path AIS upon Detection of Path-Payload Label Mismatch Defect (PLM-P):
	PLM-P		This READ/WRITE bit-field permits the user to configure the Receive STS-3c POH Processor block to automatically transmit a Path AIS

			(AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive STS-3/STM-1 Telecom Bus Interface), anytime it declares an PLM-P condition.
			0-Does not configure the Receive STS-3c POH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the PLM-P defect.
			1 – Configures the Receive STS-3c POH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the PLM-P defect.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
3	Transmit AIS-P	R/W	Transmit Path AIS upon Detection of Unstable 1 Message:
	(Downstream) upon J1 Message Unstable		This READ/WRITE bit-field permits the user to configure the Receive STS-3c POH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive STS-3/STM-1 Telecom Bus Interface), anytime it detects an Unstable J1 Message condition in the "incoming" STS-3c datastream.
			0 – Does not configure the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects an "Unstable J1 Message" condition.
			1 - Configures the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) whenever it detects an "Unstable J1 Message" condition.
		, pro	Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
2	Transmit AIS-P (Downstream) upon	R/W	Transmit Path AIS upon Detection of Path-Trace Identification Message Mismatch Defect (TIM-P):
	TIM-P Production	8,40	This READ/WRITE bit-field permits the user to configure the Receive STS-3c POH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive STS-3/STM-1 Telecom Bus Interface), anytime it declares an TIM-P condition.
	The bata and t		0-Does not configure the Receive STS-3c POH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the TIM-P defect.
			1 – Configures the Receive STS-3c POH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the TIM-P defect.
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.
1	Transmit AIS-P	R/W	Transmit Path AIS upon Detection of Loss of Pointer (LOP-P):
	(Downstream) upon LOP-P		This READ/WRITE bit-field permits the user to configure the Receive STS-3c POH Processor block to automatically transmit a Path AIS (AIS-P) Indicator via the "downstream" traffic (e.g., towards the Receive STS-3/STM-1 Telecom Bus Interface), anytime it declares an LOP-P condition.
L			

EXARExperience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

			0 – Does not configure the Receive STS-3c POH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the LOP-P defect.				
			1 – Configures the Receive STS-3c POH Processor block to transmit the AIS-P indicator (via the "downstream" traffic) upon declaration of the LOP-P defect.				
			Note: The user must also set Bit 0 (Transmit AIS-P Enable) to "1" to configure the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator, in response to this defect condition.				
0	Transmit AIS-P	R/W	Automatic Transmission of AIS-P Enable:				
	(Downstream) Enable		This READ/WRITE bit-field permits the user to configure the Receive STS-3c POH Processor block to automatically transmit the Path AIS indicator, via the down-stream traffic (e.g., towards the Receive STS-3/STM-1 Telecom Bus Interface), upon detection of an AIS-P, UNEQ-P, PLM-P, TIM-P, LOP-P, Trace Identification Message Mismatch or J1 Message Unstable conditions.				
			0 – Configures the Receive STS-3c POH Processor block to NOT automatically transmit the AlS-P indicator (via the "downstream" traffic) upon detection of any of the "above-mentioned" conditions.				
			1 – Configures the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator (via the "downstream" traffic) upon detection of any of the "above-mentioned" condition.				
			Note: The user must also set the corresponding bit-fields (within this register) to "1" in order to configure the Receive STS-3c POH Processor block to automatically transmit the AIS-P indicator upon detection of a given alarm/defect condition.				
		روا	bio lo de la				
3c POH Processor block to automatically transmit the AIS-Poindicator upon detection of a given alarm/defect condition.							

Table 733: Receive STS-3c Path - Serial Port Control Register (Address Location= 0x11BF)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unu	sed		RxPOH_CLOCK_SPEED[7:0]			
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 4	Unused	R/O	
3 - 0	RxPOH_CLOCK_SPEED[7:0]	R/W	RxPOHCIk Output Clock Signal Speed:
			These READ/WRITE bit-fields permit the user to specify the frequency of the "RxPOHCIk output clock signal.
			The formula that relates the contents of these register bits to the "RxPOHCIk" frequency is presented below.
			FREQ = 19.44/J2 * (RXPOH_CLOCK_SPEED)
			Note: For STS-3/STM-1 applications, the frequency of the BxPOHClk output signal must be in the range of 0.304MHz to 9.72MHz
	The product of and may	ot be	indered (O'



Table 734: Receive STS-3c Path – SONET Receive Auto Alarm Register – Byte 0 (Address Location= 0x11C3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit AIS-P (via Downstream STS-3c) upon LOP-P	Unused	Transmit AIS-P (via Downstream STS-3cs) upon PLM-P	Unused	Transmit AIS-P (via Downstream STS-3c) upon UNEQ-P	Transmit AIS-P (via Downstream STS-3c) upon TIM-P	Transmit AIS-P (via Downstream STS-3c) upon AIS-P	Unused
R/W	R/O	R/W	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Transmit AIS-P (via Downstream STS-3c) upon LOP-P	R/W	Transmit AlS-P (via Downstream STS-3c) upon LOP-P This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH Processor block (within the corresponding channel) to automatically transmit the AlS-P (Path AlS) Indicator via the "downstream" STS-3c signal, anytime the Receive STS-3c POH Processor block declares the LOP-P defect. 0 – Does not configure the corresponding Transmit STS-1 POH Processor block to automatically transmit the AlS-P Indicator via the "downstream" STS-3c signals, anytime the Receive STS-3c POH Processor block declares the LOP-P defect. 1 – Configures the corresponding Transmit STS-3c POH Processor block to automatically transmit the AlS-P Indicator via the "downstream" STS-3c signals, anytime the Receive STS-3c POH Processor block declares the LOP-P defect.
6	Unused	CR/O	
5	Unused Transmit AIS-P (via Downstream STS-1s) upon PLM-P	RW	Transmit AIS-P (via Downstream STS-1s) upon PLM-P: This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal, anytime the Receive STS-3c POH Processor block declares the PLM-P defect. 0 – Does not configure the corresponding Transmit STS-1 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3c POH Processor block declares the PLM-P defect. 1 – Configures the corresponding Transmit STS-1 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3c POH Processor block declares the PLM-P defect.
4	Unused	R/O	
3	Transmit AIS-P (via Downstream STS-1s) upon UNEQ-P	R/W	Transmit AIS-P (via Downstream STS-1s) upon UNEQ-P: This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal, anytime the Receive STS-3c POH Processor block declares the UNEQ-P defect.

			0 – Does not configure the corresponding Transmit STS-1 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3c POH Processor block declares the UNEQ-P defect.
			1 – Configures the corresponding Transmit STS-1 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3c POH Processor block declares the UNEQ-P defect.
2	Transmit AIS-P (via Downstream STS-1s) upon TIM-P	R/W	Transmit AIS-P (via Downstream STS-1s) upon TIM-P: This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal, anytime the Receive STS-3c POH Processor block declares the TIM-P defect.
			0 – Does not configure the corresponding Transmit STS-1 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3c POH Processor block declares the TIM-P defect.
			1 - Configures the corresponding Transmit STS-1 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3c POH Processor block declares the TIM-P defect.
1	Transmit AIS-P (via	R/W	Transmit AIS-P (via Downstream STS-1s) upon AIS-P:
	Downstream STS-1s) upon AIS-P	duc	This READ/WRITE bit-field permits the user to configure the Transmit STS-1 POH Processor block (within the corresponding channel) to automatically transmit the AIS-P (Path AIS) Indicator via the "downstream" STS-1 signal, anytime the Receive STS-3c POH Processor block declares the AIS-P defect.
	, lot	pros la	0 – Does not configure the corresponding Transmit STS-1 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signals, anytime the Receive STS-3c POH Processor block declares the AIS-P defect.
	Upused State	othe	1 — Configures the corresponding Transmit STS-1 POH Processor block to automatically transmit the AIS-P Indicator via the "downstream" STS-1 signal, anytime the Receive STS-3c POH Processor block declares the AIS-P defect.
0	Unused	R/O	

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 735: Receive STS-3c Path – Receive J1 Capture Register (Address Location= 0x11D3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
J1_Byte_Captured_Value[7:0]									
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	J1_Byte_Captured_Value[7:0]	R/O	J1 Byte Captured Value[7:0]
			These READ-ONLY bit-fields contain the value of the J1 byte, within the most recently received SONET frame.
			This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new J1 byte value.

Table 736: Receive STS-3c Path – Receive B3 Capture Register (Address Location= 0x11D7)

Віт 7	Віт 6	Віт 5	Віт 4	ВітіЗ	Віт 2	Віт 1	Віт 0		
B3_Byte_Captured_Value[7:0]									
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
0	0	0	0	8 8 B	0	0	0		

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	B3_Byte_Captured_Value[7:0]	R/O	B3 Byte Captured Value[7:0]
	, ct		These READ-ONLY bit-fields contain the value of the B3 byte, within the most recently received SONET frame. This particular value is stored in this register for one SONET
	, odle	Cot	frame period. During the next SONET frame period, this value will be overridden with a new B3 byte value.
	The prairie and ma	148	

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 737: Receive STS-3c Path – Receive C2 Capture Register (Address Location= 0x11DB)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
C2_Byte_Captured_Value[7:0]									
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	C2_Byte_Captured_Value[7:0]	R/O	C2 Byte Captured Value[7:0]
			These READ-ONLY bit-fields contain the value of the C2 byte, within the most recently received SONET frame.
			This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new C2 byte value.

Table 738: Receive STS-3c Path - Receive G1 Byte Capture Register (Address Location= 0x11DF)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			G1_Byte_Captu	ured_Value[7:0]			
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0 6	8	0	0	0

BIT NUMBER	Name	TYPE	DESCRIPTION	
7 – 0	G1_Byte_Captured_Value[7:0]	R/O	G1 Byte Captured Value[7:0]	
	, or	100	These READ-ONLY bit-fields contain the value of the C within the most recently received SONET frame.	G1 byte,
	oduct of	othe	This particular value is stored in this register for one frame period. During the next SONET frame period, the will be overridden with a new G1 byte value.	

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 739: Receive STS-3c Path – Receive F2 Byte Capture Register (Address Location=0x11E3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	F2_Byte_Captured_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	F2_Byte_Captured_Value[7:0]	R/O	G1 Byte Captured Value[7:0]
			These READ-ONLY bit-fields contain the value of the F2 byte, within the most recently received SONET frame. This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new F2 byte value.

Table 740: Receive STS-3c Path – Receive H4 Capture Register (Address Location=0x11E7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	H4_Byte_Captured_Value[7:0]									
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O			
0	0	0	0	6,00	0	0	0			

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	H4_Byte_Captured_Value[7:0]	R/O	H4 Byte Captured Value[7:0]
		or you	These READ-ONLY bit-fields contain the value of the H4 byte, within the most recently received SONET frame.
	oduct	arot	This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new H4 byte value.

The prosing y

Table 741: Receive STS-3c Path - Receive Z3 Capture Register (Address Location=0x11EB)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
	Z3_Byte_Captured_Value[7:0]								
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
0	0	0	0	0	0	0	0		

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Z3_Byte_Captured_Value[7:0]	R/O	Z3 Byte Captured Value[7:0]
			These READ-ONLY bit-fields contain the value of the Z3 byte, within the most recently received SONET frame.
			This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new Z3 byte value.

Table 742: Receive STS-3c Path - Receive Z4 (K3) Capture Register (Address Location= 0x11EF)

Віт 7	Віт 6	Віт 5	Віт 4	Вп 3	Віт 2	Віт 1	Віт 0			
	Z4(K3)_Byte_Captured_Value[7:0]									
R/O	R/O	R/O	R/O 《	R/O	R/O	R/O	R/O			
0	0	0	0	0,000,	0	0	0			

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 0	Z4(K3)_Byte_Captured_Value[7:0]	R/O	Z4 (K3) Byte Captured Value[7:0]
	Col Pr	o do	These READ-ONLY bit-fields contain the value of the Z4 (K3) byte, within the most recently received SONET frame.
	oduct are	o _©	This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new Z4 (K3) byte value.
	The preshed may		

EXAR Experience Our Connectivity.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 743: Receive STS-3c Path – Receive Z5 Capture Register (Address Location= 0x11F3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	Z5_Byte_Captured_Value[7:0]									
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O			
0	0	0	0	0	0	0	0			

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 0	Z5_Byte_Captured_Value[7:0]	R/O	Z5 Byte Captured Value[7:0]
			These READ-ONLY bit-fields contain the value of the Z5 byte, within the most recently received SONET frame.
			This particular value is stored in this register for one SONET frame period. During the next SONET frame period, this value will be overridden with a new Z5 byte value.
	The product	or prot	frame period. During the next SONET frame period, this value will be overridden with a new Z5 byte value.



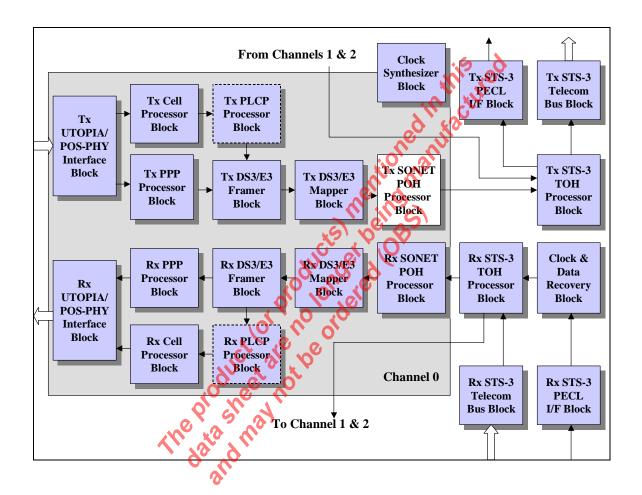
1.13.3 TRANSMIT STS-3c POH PROCESSOR BLOCK

The register map for the Transmit STS-3c POH Processor Block is presented in the Table below. Additionally, a detailed description of each of the "Transmit STS-3c POH Processor" block registers is presented below.

In order to provide some orientation for the reader, an illustration of the Functional Block Diagram for the XRT94L33, with the "Transmit STS-3c POH Processor Block "highlighted" is presented below in Figure 15.

Figure 15: Illustration of the Functional Blo

ck Diagram of the XRT94L33, with the Transmit STS-3c POH Processor Block "High-lighted".



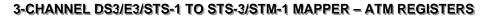


1.13.4 TRANSMIT STS-3c POH PROCESSOR BLOCK REGISTER

Table 744: Transmit STS-3c POH Processor Block - Register Address Map

Individual Register Address	Address Location	REGISTER NAME	DEFAULT VALUES
0x00 – 0x81	0x1900 – 0x1981	Reserved	0x00
0x82	0x1982	Transmit STS-3c Path – SONET Control Register – Byte 1	0x00
0x83	0x1983	Transmit STS-3c Path – SONET Control Register – Byte 0	0x00
0x84- 0x92	0x1984 – 0x1992	Reserved	0x00
0x93	0x1993	Transmit STS-3c Path – Transmit J1 Byte Value Register	0x00
0x94 – 0x96	0x1994 – 0x1996	Reserved	0x00
0x97	0x1997	Transmit STS-3c Path – B3 Byte Mask Register	0x00
0x98 – 0x9A	0x1998 – 0x199A	Reserved	0x00
0x9B	0x199B	Transmit STS-3c Path – Transmit C2 Byte Value Register	0x00
0x9C - 0x9E	0x199C – 0x199E	Reserved	0x00
0x9F	0x199F	Transmit STS-3c Path – Transmit G1 Byte Value Register	0x00
0xA0 - 0xA2	0x19A0 – 0x19A2	Reserved	0x00
0xA3	0x19A3	Transmit \$13-3c Path Transmit F2 Byte Value Register	0x00
0xA4 - 0xA6	0x19A4 – 0x19A6	Reserved	0x00
0xA7	0x19A7	Transmit STS-3c Path – Transmit H4 Byte Value Register	0x00
0xA8 – 0xAA	0x19A8 – 0x19AA	Reserved	0x00
0xAB	0x19AB	Transmit STS-3c Path – Transmit Z3 Byte Value Register	0x00
0xAC – 0xAE	0x19AC – 0x19AE	Reserved	0x00
0xAF	0x19AF	Transmit STS-3c Path – Transmit Z4 Byte Value Register	0x00
0xB0 - 0xB2	0x19B0 – 0x19B2	Reserved	0x00
0xB3	0x19B3	Transmit STS-3c Path – Transmit Z5 Byte Value Register	0x00
0xB4 - 0xB6	0x19B4 – 0x19B6	Reserved	0x00
0xB7	0x19B7	Transmit STS-3c Path – Transmit Path Control Register – Byte 0	0x00
0xB8 - 0xBA	0x19B8 – 0x19BA	Reserved	0x00
0xBB	0x19BB	Transmit STS-3c Path – Transmit J1 Control Register	0x00

INDIVIDUAL REGISTER ADDRESS	Address Location	REGISTER NAME	DEFAULT VALUES
0xBC - 0xBE	0x19BC – 0x19BE	Reserved	0x00
0xBF	0x19BF	Transmit STS-3c Path - Transmit Arbitrary H1 Byte Pointer Register	0x94
0xC0 - 0xC2	0x19C0 - 0x19C2	Reserved	0x00
0xC3	0x19C3	Transmit STS-3c Path - Transmit Arbitrary H2 Byte Pointer Register	0x00
0xC4, 0xC5	0x19C4 – 0x19C5	Reserved	0x00
0xC6	0x19C6	Transmit STS-3c Path – Transmit Pointer Byte Register – Byte 1	0x02
0xC7	0x19C7	Transmit STS-3c Path – Transmit Pointer Byte Register – Byte 0	0x0A
0xC8	0x19C8	Reserved	0x00
0xC9	0x19C9	Transmit STS-3c Path – RDI-P Control Register – Byte 2	0x40
0xCA	0x19CA	Transmit STS-3c Path – RDI-P Control Register – Byte 1	0xC0
0xCB	0x19CB	Transmit STS-3c Path - RDI-P Control Register - Byte 0	0xA0
0xCC - 0xCE	0x19CC - 0x19CE	Reserved	0x00
0xCF	0x19CF	Transmit STS-3c Path - Transmit Path Serial Port Control Register	0x00
0xD0 – 0xFF	0x19D0 – 0x19FF	Reserved	0x00
	Thep	Transmit STS-3c Path — Transmit Path Serial Port Control Register Reserved	





1.13.5 TRANSMIT STS-3c POH PROCESSOR BLOCK REGISTER DESCRIPTION

Table 745: Transmit STS-3c Path – SONET Control Register – Byte 1 (Address Location= 0x1982)

Віт 7	BIT 7 BIT 6 BIT 5 BIT 4		Віт 3	Віт 2	Віт 1	Віт 0	
	Unu	ised		Z5 Insertion Type	Z4 Insertion Type	Z3 Insertion Type	H4 Insertion Type
R/W	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 4	Unused	R/O	
3	Z5 Insertion Type	R/W	Z5 Insertion Type:
	1,450		This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH Processor block to use either the "Transmit STS-3c Path – Transmit Z5 Byte Value" Register or the TPOH input pin as the source for the Z5 byte, in the outbound STS-3c SPE.
			0 - Configures the Transmit STS-3c POH Processor block to use the "Transmit STS-3c Path - Transmit Z5 Byte Value" Register.
			1 - Configures the Transmit STS-3c POH Processor block to use the "TPOH" input as the source for the Z5 byte, in the outbound STS-3c SPE.
			Note: The Address Location of the Transmit Z5 Byte Value Register is 0x19B3
2	Z4 Insertion	R/W	Z4 Insertion Type:
	Type		This READ/WRITE bit field permits the user to configure the Transmit STS-3c POH Processor block to use either the "Transmit STS-3c Path – Transmit Z4 Byte Value" Register or the TxPOH input pin as the source for the Z4 byte in the outbound STS-3c SPE.
			0 - Configures the Transmit STS-3c POH Processor block to use the "Transmit STS-3c Path - Transmit Z4 Byte Value" Register.
		1001	17- Configures the Transmit STS-3c POH Processor block to use the TxPOH" input as the source for the Z4 byte, in the outbound STS-3c SPE.
	~	O O	Note: The address location of the Transmit Z4 Byte Value Register is 0x19AF
1	Z3 Insertion	R/W	Z3 Insertion Type:
	Туре	3	This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH Processor block to use either the "Transmit STS-3c Path – Transmit Z3 Byte Value" Register or the TxPOH input pin as the source for the Z3 byte, in the outbound STS-3c SPE.
			0 - Configures the Transmit STS-3c POH Processor block to use the "Transmit STS-3c Path - Transmit Z3 Byte Value" Register.
			1 - Configures the Transmit STS-3c POH Processor block to use the "TxPOH" input as the source for the Z3 byte, in the outbound STS-3c SPE.
			Note: The Address Location of the Transmit Z3 Byte Value Register is 0x19AB
0	H4 Insertion	R/W	H4 Insertion Type:
	Туре		This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH Processor block to use either the "Transmit STS-3c Path – Transmit H4 Byte Value" Register or the TxPOH input pin as the source for the H4

Rev		

byte, in the outbound STS-3c SPE.
0 – Configures the Transmit STS-3c POH Processor block to use the "Transmit STS-3c Path – Transmit H4 Byte Value" Register.
1 – Configures the Transmit STS-3c POH Processor block to use the "TPOH" input as the source for the H4 byte, in the outbound STS-3c SPE.
Note: The Address Location of the Transmit H4 Byte Value Register is 0x19A7

The product of products in an infactured of the product of products in a product of the ordered (OBS).

The product of product are no ordered (OBS).



Rev 2.0.0

Table 746: Transmit STS-3c Path – SONET Control Register – Byte 0 (Address Location= 0x1983)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
F2 Insertion Type		nsertion [1:0]		nsertion e[1:0]	C2 Byte Insertion Type	Unused	Transmit AIS- P Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/O	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7	F2 Insertion	R/W	F2 Insertion Type:
	Туре		This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH Processor block to use either the "Transmit STS-3c Path – Transmit F2 Byte Value" Register or the TxPOH input pin as the source for the F2 byte, in the outbound STS-3c SPE.
			0 – Configures the Transmit STS-3c POH Processor block to use the "Transmit STS-3c Path – Transmit F2 Value" Register
			1 – Configures the Transmit STS-3c POH Processor block to use the "TPOH" input as the source for the F2 byte, in the outbound STS-3c SPE.
			Note: The Address Location of the Transmit F2 Byte Value Register is 0x19A3
6 - 5	REI-P Insertion	R/W	REI-P Insertion Type[1:0]:
	Type[1:0]		These two READ/WRITE bit-fields permit the user to configure the Transmit STS-3c POH Processor block to use one of the three following sources for the REI-P bit-fields (e.g., bits 1 through 4, within the G1 byte of the outbound STS-3c SPE).
			• From the corresponding Receive STS-3c POH Processor block (e.g., when it detects B3 bytes in its incoming SPE data).
			From the "Transmit G1 Byte Value" Register.
			From the "TPOH" input pin.
		PIO	00/th — Configures the Transmit STS-3c POH Processor block to set Bits 1 through 4 (in the G1 byte of the outbound SPE) based upon "receive conditions" as detected by the corresponding Receive STS-3c POH Processor block.
	*	data	O1 Configures the Transmit STS-3c POH Processor block to set Bits 1 through 4 (in the G1 byte of the outbound SPE) based upon the contents within the "Transmit G1 Byte Value" register.
			10 – Configures the Transmit STS-3c POH Processor block to use the TPOH input pin as the source of Bits 1 through 4 (in the G1 byte of the outbound SPE).
			Note: The address location of the Transmit G1 Byte Value Register is 0x199F
4 - 3	RDI-P	R/W	RDI-P Insertion Type[1:0]:
	Insertion Type[1:0]		These two READ/WRITE bit-fields permit the user to configure the Transmit STS-3c POH Processor block to use one of the three following sources for the RDI-P bit-fields (e.g., bits 5 through 7, within the G1 byte of the outbound STS-3c SPE).
			• From the corresponding Receive STS-3c POH Processor block (e.g., when it detects various alarm conditions within its incoming STS-3c SPE data).
			From the "Transmit G1 Byte Value" Register.

			From the "TPOH" input pin.
			00/11 - Configures the Transmit STS-3c POH Processor block to set Bits 5 through 7 (in the G1 byte of the outbound SPE) based upon "receive conditions" as detected by the corresponding Receive STS-3c POH Processor block.
			01 - Configures the Transmit STS-3c POH Processor block to set Bits 5 through 7 (in the G1 byte of the outbound SPE) based upon the contents within the "Transmit G1 Byte Value" register.
			10 – Configures the Transmit STS-3c POH Processor block to use the TPOH input pin as the source of Bits 5 through 7 (in the G1 byte of the outbound SPE).
			Note: The address location of the Transmit G1 Byte Value Register is 0x199F
2	C2 Byte	R/W	C2 Insertion Type:
	Insertion Type		This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH Processor block to use either the "Transmit STS-3c Path – Transmit C2 Byte Value" Register or the TPOH input pin as the source for the C2 byte, in the outbound STS-3c SPE.
			0 – Configures the Transmit STS-3c POH Processor block to use the "Transmit STS-3c Path – Transmit C2 Byte Value" Register.
			1 – Configures the Transmit STS-3c POH Processor block to use the "TPOH" input as the source for the C2 byte, in the outbound STS-3c SPE.
			Note: The address location of the Transmit C2 Byte Value Register is 0x199B
1	Unused	R/O	is be by
0	Transmit	R/W	Transmit AIS-P Enable:
	AIS-P Enable		This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH Processor block to (via software control) transmit an AIS-P indicator to the remote PTE.
			If this feature is enabled, then the Transmit STS-3c POH Processor block will automatically set the H1, H2, H3 and all the "outbound" STS-3c SPE bytes to an "All Ones" pattern, prior to routing this data to the Transmit STS-3 TOH Processor block.
	•	log's	O – Configures the Transmit STS-3c POH Processor block to NOT transmit the AIS-P indicator to the remote PTE.
	The	10	Configures the Transmit STS-3c POH Processor block to transmit the AIS-P indicator to the remote PTE.
		, 7	



Rev 2.0.0

Table 747: Transmit STS-3c Path – Transmitter J1 Byte Value Register (Address Location= 0x1993)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
			Transmit_J	1_Byte[7:0]			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

	smit J1 Byte 'alue[7:0]	R/W	Transmit J1 Byte Value: These READ/WRITE bit-fields permit the user to have software control over
Va	alue[7:0]		
			the value of the J1 byte, within each outbound STS-3c SPE.
			If the user configures the Transmit STS-3c POH Processor block to this register as the source of the J1 byte then it will automatically write the contents of this register into the J1 byte location, within each "outbound" STS-3c SPE. This feature is enabled whenever the user writes the value "[1, 0]" into Bits 1 and 0 (Insertion Method) within the "Transmit STS-3c Path – SONET Path J1 Byte Control Register" register. Note: The Address Location of the Transmit STS-3c Path – SONET J1 Byte Control Register is 0x19BB

Table 748: Transmit STS-3c Path – Transmitter B3 Error Mask Register (Address Location= 0x1997)

Віт 7	Віт 6	Віт 5	Віт 4	Bit 3	Віт 2	Віт 1	Віт 0
Transmit_B3_Byte_Mask[7:0]							
R/W	R/W	R/W	O R/W	R/W	R/W	R/W	R/W
0	0	0	600	0	0	0	0

BIT NUMBER	Name	TYPE (DESCRIPTION
7 - 0	Transmit B3 Byte Mask[7:0]	RAY	Transmit B3 Byte Mask[7:0]: This READ/WRITE bit-field permits the user to insert errors into the B3 byte, within the "outbound" STS-3c SPE, prior to transmission to the Transmit STS-3 TOH Processor block. The Transmit STS-3c POH Processor block will perform an XOR operation with the contents of this register, and the B3 byte value. The results of this operation will be written back into the B3 byte of the "outbound" STS-3c SPE. If the user sets a particular bit-field, within this register, to "1", then that corresponding bit, within the "outbound" B3 byte will be in error. Note: For normal operation, the user should set this register to 0x00.

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Table 749: Transmit STS-3c Path – Transmit C2 Byte Value Register (Address Location= 0x199B)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit_C2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	Transmit C2 Byte R/W		Transmit C2 Byte Value:
	Value[7:0]		These READ/WRITE bit-fields permit the user to have software control over the value of the C2 byte, within each outbound STS-3c SPE.
			If the user configures the Transmit STS-3c POH Processor block to this register as the source of the C2 byte, then it will automatically write the contents of this register into the C2 byte location, within each "outbound" STS-3c SPE.
		This feature is enabled whenever the user writes a "0" into Bit 2 (C2 Insertion Type) within the "Transmit STS-3c Path – SONET Control Register – Byte 0" register.	
			Note: The Address Location of the Transmit STS-3c Path – SONET Control Register - Byte 0" Register is 0x1983

Table 750: Transmit STS-3c Path – Transmit G1 Byte Value Register (Address Location= 0x199F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Transmit_G1_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	6. %	0	0	0	0

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit G1 Byte Value[7:0]	and man	Transmit G1 Byte Value: These READ/WRITE bit-fields permit the user to have software control over the contents of the RDI-P and REI-P bit-fields, within each G1 byte in the "outbound" STS-3c SPE. If the users sets "REI-P_Insertion_Type[1:0]" and "RDI-P_Insertion_Type[1:0]" bits to the value [0, 1], then contents of the REI-P and the RDI-P bit-fields (within each G1 byte of the "outbound" STS-3c SPE) will be dictated by the contents of this register. Note: 1. The "REI-P_Insertion_Type[1:0]" and "RDI-P_Insertion_Type[1:0]" bit-fields are located in the "Transmit STS-3c Path — SONET Control Register — Byte 0" Register. 2. The Address Location of the Transmit STS-3c Path — SONET Control Register — Byte 0" Register is 0x1983

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 751: Transmit STS-3c Path – Transmit F2 Byte Value Register (Address Location= 0x19A3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit_F2_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	Name	Түре	DESCRIPTION
7 - 0	Transmit F2 Byte	R/W	Transmit F2 Byte Value:
	Value[7:0]	These READ/WRITE bit-fields permit the user to have software control over the value of the F2 byte, within each outbound STS-3c SPE.	
			If the user configures the Transmit STS-3c POH Processor block to this register as the source of the F2 byte, then it will automatically write the contents of this register into the F2 byte location, within each "outbound" STS-3c SPE. This feature is enabled whenever the user writes a "0" into Bit 7 (F2 Insertion Type) within the "Transmit STS-3c Path – SONET Control Register – Byte 0" register. Note: The Address Location of the Transmit STS-3c Path – SONET Control Register is 0x1983

Table 752: Transmit STS-3c Path – Transmit H4 Byte Value Register (Address Location= 0x19A7)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 2	Віт 1	Віт 0	
Transmit_H4_Byte_Value[7:0]							
R/W	R/W	R/W	R/W R/W	R/W	R/W	R/W	
0	0	0	0 00 0	0	0	0	

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 - 0	Transmit H4 Byte Value[7:0]	Para da anti	Transmit H4 Byte Value: These READ/WRITE bit-fields permit the user to have software control over the value of the H4 byte, within each outbound STS-3c SPE. If the user configures the Transmit STS-3c POH Processor block to this register as the source of the H4 byte, then it will automatically write the contents of this register into the H4 byte location, within each "outbound" STS-3c SPE. This feature is enabled whenever the user writes a "0" into Bit 0 (H4 Insertion Type) within the "Transmit STS-3c Path – SONET Control Register – Byte 1" register. Note: The Address Location for the "Transmit STS-3c Path – SONET Control Register – Byte 1" register is 0x1982

Table 753: Transmit STS-3c Path – Transmit Z3 Byte Value Register (Address Location= 0x19AB)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Transmit_Z3_Byte_Value[7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	Transmit Z3 Byte	R/W	Transmit Z3 Byte Value:
	Value[7:0]	These READ/WRITE bit-fields permit the user to have software control over the value of the Z3 byte, within each outbound STS-3c SPE.	
			If the user configures the Transmit STS-3c POH Processor block to this register as the source of the Z3 byte, then it will automatically write the contents of this register into the Z3 byte location, within each "outbound" STS-3c SPE. This feature is enabled whenever the user writes a "0" into Bit 1 (Z3 Insertion Type) within the "Transmit STS-3c Path – SONET Control Register – Byte 1" register.
			Note: The Address Location for the "Transmit STS-3c Path – SONET Control Register – Byte 1" register is 0x1982

Table 754: Transmit STS-3c Path – Transmit ZA Byte Value Register (Address Location= 0x19AF)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0				
Transmit_Z4_Byte_Value[7:0]											
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W				
0	0	0 0	0	0	0	0	0				
			10,00								

BIT NUMBER	Name	TYPE	DESCRIPTION
7 - 0	Transmit Z4 Byte Value[7:0]	RY HI	Transmit Z4 Byte Value: These READ/WRITE bit-fields permit the user to have software control over the value of the Z4 byte, within each outbound STS-3c SPE. If the user configures the Transmit STS-3c POH Processor block to this register as the source of the Z4 byte, then it will automatically write the contents of this register into the Z4 byte location, within each "outbound" STS-3c SPE. This feature is enabled whenever the user writes a "0" into Bit 2 (Z4 Insertion Type) within the "Transmit STS-3c Path – SONET Control Register – Byte 0" register. Note: The Address Location of the Transmit STS-3c Path – SONET Control Register – Byte 0" Register is 0x1982



Rev 2.0.0

Table 755: Transmit STS-3c Path – Transmit Z5 Byte Value Register (Address Location= 0x19B3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
Transmit_Z5_Byte_Value[7:0]										
R/W	R/W R/W R/W R/W R/W R/W						R/W			
0	0	0	0	0	0	0	0			

BIT NUMBER	NAME	Түре	DESCRIPTION				
7 - 0	Transmit Z5 Byte	R/W	Transmit Z5 Byte Value:				
	Value[7:0]		These READ/WRITE bit-fields permit the user to have software control over the value of the Z5 byte, within each outbound STS-3c SPE.				
			If the user configures the Transmit STS-3c POH Processor block to this register as the source of the Z5 byte, then it will automatically write the contents of this register into the Z5 byte location, within each "outbound" STS-3c SPE.				
			This feature is enabled whenever the user writes a "0" into Bit 3 (Z5 Insertion Type) within the "Transmit STS-3c Path – SONET Control Register – Byte 0" register.				
			Note: The Address Location of the Transmit STS-3c Path – SONET Control Register – Byte 0" register is 0x1982				
	The	produ datand	Note: The Address Location of the Transmit STS-3c Path – SONET Control Register – Byte 0" register is 0x1982				

Table 756: Transmit STS-3c Path – Transmit Path Control Register (Address Location= 0x19B7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Unused		Pointer Force	Check Stuff	Insert Negative Stuff	Insert Positive Stuff	Insert Continuous NDF Events	Insert Single NDF Event
R/O	R/O	R/W	R/W	W	W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 6	Unused	R/O	
5	Pointer Force	R/W	Pointer Force: This READ/WRITE bit-field permits the user to load the values contained within the "Transmit STS-3c POH Arbitrary H1 Pointer Byte" and "Transmit STS-3c POH Arbitrary H2 Pointer Byte" registers into the H1 and H2 bytes (within the outbound STS-3c data stream). Note: The actual location of the SPE will NOT be adjusted, per the value of H1 and H2 bytes. Hence, this feature should cause the remote terminal to declare an "Invalid Pointer" condition. 0 - Configures the Transmit STS-3c POH and Transmit STS-3 TOH Processor blocks to transmit STS-3c/STS-3 data with normal and correct H1 and H2 bytes. 1 - Configures the Transmit STS-3c POH and Transmit STS-3 TOH Processor blocks to overwrite the values of the H1 and H2 bytes (in the outbound STS-3c/STS-3 data-stream) with the values in the "Transmit STS-3c POH Arbitrary H1 and H2 Pointer Byte" registers. Note: 1. The Address Location of the Transmit STS-3c Arbitrary H1 Pointer Byte register is 0x19BF 2. The Address Location of the Transmit STS-3c Arbitrary H2 Pointer Byte register is 0x19C3
4	Check Stuff	RAY OF THE PROPERTY OF THE PRO	Check Stuff Monitoring: This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH and Transmit STS-3 TOH Processor blocks to only execute a "Positive", "Negative" or "NDF" event (via the "Insert Positive Stuff", "Insert Negative Stuff", "Insert Continuous or Single NDF" options, via software command) if no pointer adjustment (NDF or otherwise) has occurred during the last 3 SONET frame periods. 0 – Disables this feature. In this mode, the Transmit STS-3c POH and Transmit STS-3 TOH Processor blocks will execute a "software-commanded" pointer adjustment event, independent of whether a pointer adjustment event has occurred in the last 3 SONET frame periods. 1 – Enables this feature. In this mode, the Transmit STS-3c POH and Transmit STS-3 TOH Processor blocks will ONLY execute a "software-commanded" pointer adjustment event, if no pointer adjustment event has occurred during the last 3 SONET frame periods.
3	Insert Negative Stuff	R/W	Insert Negative Stuff: This READ/WRITE bit-field permits the user to configure the Transmit STS-3c

Rev 2.0.0

			POH and Transmit STS-3 TOH Processor blocks to insert a negative-stuff into
			the outbound STS-3c/STS-3 data stream. This command, in-turn will cause a "Pointer Decrementing" event at the remote terminal.
			Writing a "0" to "1" transition into this bit-field causes the following to happen.
			• A negative-stuff will occur (e.g., a single payload byte will be inserted into the H3 byte position within the outbound STS-1/STS-3 data stream).
			• The "D" bits, within the H1 and H2 bytes will be inverted (to denote a "Decrementing" Pointer Adjustment event).
			• The contents of the H1 and H2 bytes will be decremented by "1", and will be used as the new pointer from this point on.
			Note: Once the user writes a "1" into this bit-field, the XRT94L33 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to "0".
2	Insert Positive	R/W	Insert Positive Stuff:
	Stuff		This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH and Transmit STS-3 TOH Processor blocks to insert a positive-stuff into the outbound STS-3c/STS-3 data stream. This command, in-turn will cause a "Pointer Incrementing" event at the remote terminal.
			Writing a "0" to "1" transition into this bit-field causes the following to happen.
			• A positive-stuff will occur (e.g., a single stuff-byte will be inserted into the STS-3c/STS-3 data-stream, immediately after the H3 byte position within the outbound STS-3c/STS-3 data stream).
			The "I" bits, within the H1 and H2 bytes will be inverted (to denote a "Incrementing" Pointer Adjustment event).
			 The contents of the H1 and H2 bytes will be incremented by "1", and will be used as the new pointer from this point on.
			Note: Once the user writes a "1" into this bit-field, the XRT94L33 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to "0".
1	Insert	R/W	Insert Continuous NDF Events:
	Continuous NDF Events	eprod	This READ/WRITE bit-field permits the user configure the Transmit STS-3c POH and Transmit STS-3 TOH Processor blocks to continuously insert a New Data Flag (NDF) pointer adjustment into the outbound STS-3c/STS-3 data stream.
	N. C.	data	As the Transmit STS-3c POH and Transmit STS-3 TOH Processor blocks insert the NDF event into the STS-1/STS-3 data stream, it will proceed to load in the contents of the "Transmit STS-3c POH Arbitrary H1 Pointer" and "Transmit STS-3c POH Arbitrary H2 Pointer" registers into the H1 and H2 bytes (within the outbound STS-3c/STS-3 data stream).
			0 - Configures the "Transmit STS-3c TOH and Transmit STS-3 POH Processor" blocks to not continuously insert NDF events into the "outbound" STS-3c/STS-3 data stream.
			1- Configures the "Transmit STS-3c TOH and Transmit STS-3 POH Processor" blocks to continuously insert NDF events into the "outbound" STS-3c/STS-3 data stream.
0	Insert Single	R/W	Insert Single NDF Event:
	NDF Event		This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH and Transmit STS-3 TOH Processor blocks to insert a New Data Flag (NDF) pointer adjustment into the outbound STS-3c/STS-3 data stream.
	I.	I	

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Writing a "0" to "1" transition into this bit-field causes the following to happen. • The "N" bits, within the H1 byte will set to the value "1001" • The ten pointer-value bits (within the H1 and H2 bytes) will be set to new pointer value per the contents within the "Transmit STS-3c POH – Arbitrary H1 Pointer" and "Transmit STS-3c POH Arbitrary H2 Pointer" registers (Address Location= 0xN9BF and 0xN9C3). • Afterwards, the "N" bits will resume their normal value of "0110"; and this new pointer value will be used as the new pointer from this point on. Note: Once the user writes a "1" into this bit-field, the XRT94L33 will automatically clear this bit-field. Hence, there is no need to subsequently reset this bit-field to "0". 2. The Address Location of the Transmit STS-3c Arbitrary H1 Pointer Byte of the Transcription of the Transcription of the Transcription of the Indian of the ordered of t register is 0x19BF 3. The Address Location of the Transmit STS-3c Arbitrary H2 Pointer Byte



Rev 2.0.0

Table 757: Transmit STS-3c Path – SONET Path J1 Byte Control Register (Address Location= 0x19BB)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0	
	Unused			Message_l	Length[1:0]	Insertion_Method[1:0]		
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W	
0	0	0	0	0	0	0	0	

BIT NUMBER	NAME	Түре	DESCRIPTION				
7 – 4	Unused	R/O					
3 - 2	Message_Length[1:0]	R/W	J1 Message Length[1:0]:				
			These READ/WRITE bit-fields permit the user to specify the length of the J1 Trace Message, that the Transmit STS-3c POH Processor block will transmit. The relationship between the content of these bit-fields and the corresponding J1 Trace Message Length is presented below.				
			MSG LENGTH Resulting J1 Trace Message Length				
			00 1 Byte 1				
			01 16 Bytes				
			10/11 64 Bytes				
1 - 0	Insertion_Method[1:0]	R/W	J1 Insertion_Method[1:0]:				
			These READ/WRITE bit-fields permit the user to specify the method that he/she will use to insert the J1 byte into the outbound STS-3c SPE. The relationship between the contents of these bit-fields and the corresponding J1 Insertion Method is presented below.				
		المن	Insertion Resulting Insertion Method Method[1:0]				
		911	00 Insert the value "0x00"				
	ar ar	Divor	01 Insert from the J1 Trace Buffer				
	Thebri	SAM	Insert from the "Transmit STS-3c Path – Transmit J1 Byte Value Register.				
		9,	11 Insert via the "TxPOH_n" input port				

Table 758: Transmit STS-3c Path – Transmit Arbitrary H1 Pointer Register (Address Location= 0x19BF)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	NDF Bits			SS	Bits	H1 Point	ter Value
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 4	NDF Bits	R/W	NDF (New Data Flag) Bits:
			These READ/WRITE bit-fields permit the user provide the value that will be loaded into the "NDF" bit-field (of the H1 byte), whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the "Transmit STS-3c Path – Transmit Path Control" Register.
			Note: The Address Location of the Transmit STS-3c Path – Transmit Path Control register is 0x19B7
3 - 2	SS Bits	R/W	SS Bits
			These READ/WRITE bit-fields permits the user to provide the value that will be loaded into the "SS" bit-fields (of the H1 byte) whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the "Transmit STS-3c Path – Transmit Path Control" Register.
			Note:
			1. The "SS" bits have no functional value, within the H1 byte.
			2. The Address Location of the Transmit STS-3c Path – Transmit Path Control register is 0x19B7
1 - 0	H1 Pointer	R/W	H1 Pointer Value[1:0]:
	Value[1:0]		These two READ/WRITE bit-fields, along with the constants of the "Transmit STS 3c Path – Transmit Arbitrary H2 Pointer" Register (Address Location= 0xN9C3) permit the user to provide the contents of the Pointer Word.
		6000	These two READ/WRITE bit-fields permit the user to define the value of the two most significant bits within the Pointer word.
	The	ato de	Whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the Transmit STS-3c Path – Transmit Path Control" Register, the values of these two bits will be loaded into the two most significant bits within the Pointer Word.
		91	Note: The Address Location of the Transmit STS-3c Path – Transmit Path Control register is 0x19B7



Rev 2.0.0

Table 759: Transmit STS-3c Path - Transmit Arbitrary H2 Pointer Register (Address Location= 0x19C3)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0			
	H2 Pointer Value[7:0]									
R/W R/W R/W R/W R/W R/W R/W							R/W			
0	0	0	0	0	0	0	0			

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 0	H2 Pointer	R/W	H2 Pointer Value[1:0]:
	Value[7:0]		These eight READ/WRITE bit-fields, along with the constants of bits 1 and 0 within the "Transmit STS-3c Path – Transmit Arbitrary H1 Pointer" Register permit the user to provide the contents of the Pointer Word.
			These two READ/WRITE bit-fields permit the user to define the value of the eight least significant bits within the Pointer word. Whenever a "0 to 1" transition occurs in Bit 5 (Pointer Force) within the Transmit STS-3c Path – Transmit Path Control" Register, the values of these
			eight bits will be loaded into the H2 byte, within the outbound STS-3c/STS-3 data stream. Note:
			1. The Address Location of the Transmit STS-3c Path – Transmit Arbitrary H1 Pointer" register is 0x19C3
			2. The Address Location of the Transmit STS-3c Path – Transmit Path Control register is 0x19B7

Table 760: Transmit STS-3c Path - Transmit current Pointer Byte Register - Byte 1 (Address Location= 0x19C6)

Віт 7	Віт 6	Віт 5	Bit 4	Віт 3	Віт 2	Віт 1	Віт 0			
		Tx_Pointer	r_High[1:0]							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O			
0	0	0 0	600	0	0	1	0			
	0, 4, 1									

BIT NUMBER	NAME	TYPE	DESCRIPTION
7 – 2	Unused	R/O	
1 - 0	Tx_Pointer_Hi gh[1:0]	R/O	Transmit Pointer Word – High[1:0]: These two READ-ONLY bits, along with the contents of the "Transmit STS-3c Path – Transmit Current Pointer Byte Register – Byte 0" reflect the current value of the pointer (or offset of SPE within the STS-3c frame).
			These two bits contain the two most significant bits within the "10-bit pointer" word.
			Note: The Address Location of the Transmit STS-3c Path – Transmit Current Pointer Byte – Byte 0 register is 0x19C7

Table 761: Transmit STS-3c Path - Transmit Current Pointer Byte Register - Byte 0 (Address Location= 0x19C7)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0				
	Tx_Pointer_Low[7:0]										
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O				
0	0	0	0	1	0	1	0				

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 0	Tx_Pointer_Lo	R/O	Transmit Pointer Word – Low[7:0]:
	w[7:0]		These two READ-ONLY bits, along with the contents of the "Transmit STS-3c Path – Transmit Current Pointer Byte Register – Byte 1" reflect the current value of the pointer (or offset of SPE within the STS-3c frame).
			These two bits contain the eight least significant bits within the "10-bit pointer" word.
			Note: The Address Location of the Transmit STS-3c Path – Transmit Current Pointer Byte – Byte 0 register is 0x19C6
	the	ata dict	Corproducts Indered (OBS) Let are ho ordered (OBS) Analytic to the corporation of the c

EXAR Experience Our Connectivity

3-CHANNEL DS3/E3/STS-1 TO STS-3/STM-1 MAPPER - ATM REGISTERS

Rev 2.0.0

Table 762: Transmit STS-3c Path – RDI-P Control Register – Byte 2 (Address Location= 0x19C9)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unu	ised		PLM-P RDI-P Code[2:0]			Transmit RDI-P upon PLM-P
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 – 4	Unused	R/O	
3 - 1	PLM-P RDI-P Code[2:0]	R/W	PLM-P (Path – Payload Mismatch) – RDI-P Code: These three READ/WRITE bit-fields permit the user to specify the value that the Transmit STS-3c POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within the "outbound" STS-3c SPE), whenever the corresponding Receive STS-3c POH Processor block detects and declares a PLM-P condition. Note: In order to enable this feature, the user must set Bit 0 (RDI-P upon PLM-P) within this register to "1".
0	Transmit RDI-P upon PLM-P	R/W	Transmit RDI-P upon PLM-P: This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH Processor block to automatically transmit the RDI-P Code (as configured in Bits 3 through 1 – within this register) whenever the corresponding Receive STS-3c POH Processor block declares a PLM-P condition. 0 – Disables the automatic transmission of RDI-P upon detection of PLM-P. 1 – Enables the automatic transmission of RDI-P upon detection of PLM-P.
	Thepro	duct sheet s	not be

Table 763: Transmit STS-3c Path – RDI-P Control Register – Byte 1 (Address Location= 0x19CA)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
TIM-F	P RDI-P Cod	e[2:0]	Transmit RDI-P upon TIM-P	UNEQ-P RDI-P Code[2:0]		Transmit RDI-P upon UNEQ-P	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 5	TIM-P RDI-P	R/W	TIM-P (Path – Trace Identification Mismatch) – RDI-P Code:
	Code[2:0]		These three READ/WRITE bit-fields permit the user to specify the value that the Transmit STS-3c PQH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within the "outbound" STS-3c SPE), whenever the corresponding Receive STS-3c POH Processor block detects and declares a TIM-P condition.
			Note: In order to enable this feature, the user must set Bit 4 (RDI-P upon TIM-P) within this register to "1".
4	Transmit RDI-P upon	R/W	Transmit RDI-P upon TIM-P:
	TIM-P		This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH Processor block to automatically transmit the RDI-P Code (as configured in Bits 7 through 5 – within this register) whenever the corresponding Receive STS-3c POH Processor block declares a TIM-P condition.
		ي د	O Disables the automatic transmission of RDI-P upon detection of TIM-P. 1 Enables the automatic transmission of RDI-P upon detection of
		, 6,	TIM-P
3 - 1	UNEQ-P RDI-P	R/W	UNEQ-P (Path – Unequipped) – RDI-P Code:
	UNEQ-P RDI-P Code[2:0] Transmit RDI-P upon	ectno	These three READ/WRITE bit-fields permit the user to specify the value that the Transmit STS-3c POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within the "outbound" STS-3c SPE), whenever the corresponding Receive STS-3c POH Processor block detects and declares a UNEQ-P condition.
	Theata	Wa,	Note: In order to enable this feature, the user must set Bit 4 (RDI-P upon UNEQ-P) within this register to "1".
0	Transmit RDI-P upon UNEQ-P	R/W	Transmit RDI-P upon UNEQ-P:
	UNEQ-P		This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH Processor block to automatically transmit the RDI-P Code (as configured in Bits 7 through 5 — within this register) whenever the corresponding Receive STS-3c POH Processor block declares a UNEQ-P condition.
			0 – Disables the automatic transmission of RDI-P upon detection of UNEQ-P.
		_	1 – Enables the automatic transmission of RDI-P upon detection of UNEQ-P.



Rev 2.0.0

Table 764: Transmit STS-3c Path – RDI-P Control Register – Byte 1 (Address Location= 0x19CB)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
LOP	-P RDI-P Code	e[2:0]	Transmit RDI-P upon LOP-P	AIS-P RDI-P Code[2:0]			Transmit RDI- P upon AIS-P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	0	0	0	0	0	0

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 5	LOP-P RDI-P	R/W	LOP-P (Path – Loss of Pointer) – RDI-P Code:
	Code[2:0]		These three READ/WRITE bit-fields permit the user to specify the value that the Transmit STS-3c POH Rrocessor block will transmit, within the RDI-P bit-fields of the G1 byte (within the "outbound" STS-3c SPE), whenever the corresponding Receive STS-3c POH Processor block detects and declares a LOP-P condition.
			Note: In order to enable this feature, the user must set Bit 4 (RDI-P upon LOP-P) within this register to "1".
4	Transmit RDI-P upon	R/W	Transmit RDI-P upon LOP-P:
	LOP-P		This READ/WRITE bit field permits the user to configure the Transmit STS-3c POH Processor block to automatically transmit the RDI-P Code (as configured in Bits 7 through 5 – within this register) whenever the corresponding Receive STS-3c POH Processor block declares a LOP-P condition.
			0 – Disables the automatic transmission of RDI-P upon detection of LOP-P.
		, ०	1 – Enables the automatic transmission of RDI-P upon detection of LOP-P.
3 - 1	AIS-P RDI-P Code[2:0]	RW duceta	AlS-P (Path – AlS) – RDI-P Code: These three READ/WRITE bit-fields permit the user to specify the value that the Transmit STS-3c POH Processor block will transmit, within the RDI-P bit-fields of the G1 byte (within the "outbound" STS-3c SPE), whenever the corresponding Receive STS-3c POH Processor block detects and declares an AIS-P condition.
	Theat	nd m	Note: In order to enable this feature, the user must set Bit 4 (RDI-P upon AIS-P) within this register to "1".
0	Halisilik Kul-r upon	R/W	Transmit RDI-P upon AIS-P:
	AIS-P		This READ/WRITE bit-field permits the user to configure the Transmit STS-3c POH Processor block to automatically transmit the RDI-P Code (as configured in Bits 7 through 5 – within this register) whenever the corresponding Receive STS-3c POH Processor block declares a AIS-P condition.
			0 – Disables the automatic transmission of RDI-P upon detection of AIS-P.
			1 – Enables the automatic transmission of RDI-P upon detection of AIS-P.

Table 765: Transmit STS-3c Path – Serial Port Control Register (Address Location= 0x19CF)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Unu	ised			TxPOH Clock	k Speed [3:0]	
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	Name	Түре	DESCRIPTION
7 – 4	Unused	R/O	
3 – 0	TxPOH Clock Speed	R/W	TxPOHCIk Output Clock Signal Speed:
	[3:0]		These READ/WRITE bit-fields permit the user to specify the frequency of the "TxPOHCIk output clock signal. The formula that relates the contents of these register bits to the "TxPOHCIk" frequency is presented below.
			FREQ = 19.44/[2 * (TxPOH_CLOCK_SPEED + 1)
			Note: For STS-3/STM-1 applications, the frequency of the RxPOHCIk output signal must be in the range of 0.304MHz to 9.72MHz
to 9.72MHz. To 9.72MHz. The product are not longered to 1.354miles and the large of 0.354miles are not longered to 1.354miles and the large of 0.354miles are not longered to 1.354miles			



NOTES:

Rev. 2.0.0 – Added description of bits 4, 5, 6 of register 0x011B.

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or teliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein conveys and irrepse under any patent or other right, and makes no representation.

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained here in are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

Copyright 2007 EXAR Corporation

DataSheet March 2007

Reproduction in part or whole, without prior written consent of EXAR Corporation is prohibited