40V 1.5A Synchronous Step-Down COT Regulator

Description

The XR76201 is a synchronous step-down regulator combining the controller, drivers, bootstrap diode and MOSFETs in a single package for point-of-load supplies. The XR76201 is capable of supplying steady state loads of 1.5A. A wide 5V to 40V input voltage range allows for single supply operation from 12V battery systems required to withstand load dump, industry standard 24V ±10%, 18V to 36V, and rectified 18VAC and 24VAC rails.

With a proprietary emulated current mode Constant On-Time (COT) control scheme, the XR76201 provides extremely fast line and load transient response using ceramic output capacitors. They require no loop compensation, simplifying circuit implementation and reducing overall component count. The control loop also provides 0.05% load and 0.15% line regulation and maintains constant operating frequency. A selectable power saving mode allows the user to operate in Discontinuous Conduction Mode (DCM) at light current loads, thereby significantly increasing the converter efficiency.

A host of protection features, including overcurrent, over temperature, short-circuit and UVLO, helps achieve safe operation under abnormal operating conditions.

The XR76201 is available in a RoHS-compliant, green / halogen-free, space-saving 5mm x 5mm QFN package.

FEATURES

- Controller, drivers, bootstrap diode and MOSFETs integrated in one package
- 1.5A step-down regulator
  - Wide 5V to 40V input voltage range
  - >0.6V adjustable output voltage
- Proprietary constant on-time control
  - No loop compensation required
  - Stable ceramic output capacitor operation
  - Programmable 100ns to 1µs on-time
  - Constant 400kHz to 800kHz frequency
- Selectable CCM or CCM / DCM
  - CCM / DCM for high efficiency at light-load
  - CCM for constant frequency at light-load
- Programmable hiccup current limit with thermal compensation
- Precision enable and Power Good flag
- Programmable soft-start
- 30-pin 5mm x 5mm QFN package

APPLICATIONS

- Automotive systems
- Industrial
- Military

Ordering Information – back page

Typical Application

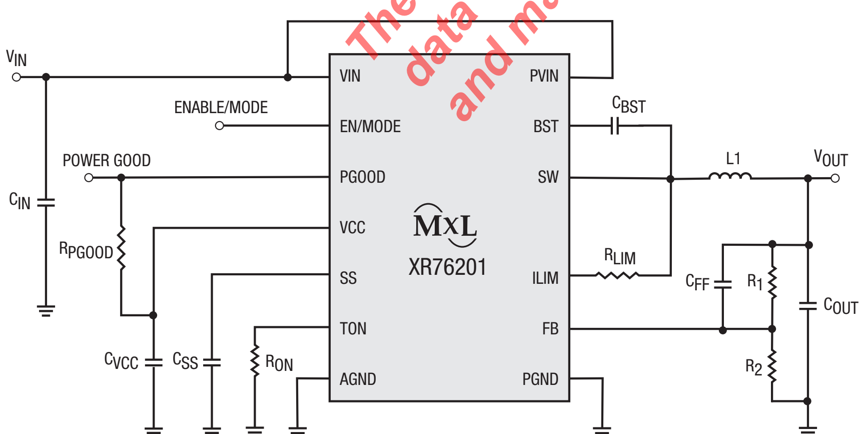


Figure 1. Typical Application

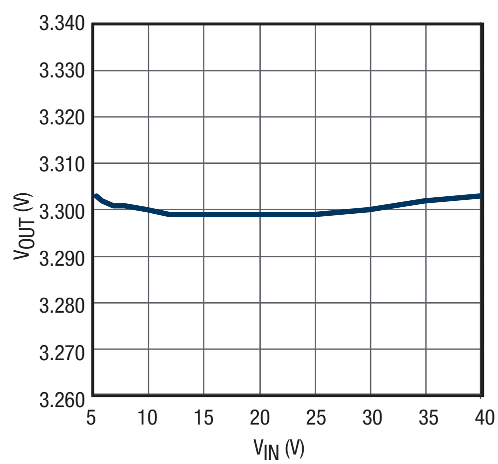


Figure 2. Line Regulation

Absolute Maximum Ratings

Stresses beyond the limits listed below may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

PV_{IN}, V_{IN} .... -0.3V to 43V

V_{CC} .... -0.3V to 6.0V

BST .... -0.3V to 48V(1)

BST-SW .... -0.3V to 6V

SW, ILIM .... -1V to 43V(1)(2)

ALL other pins .... -0.3V to VCC + 0.3V

Storage temperature .... -65°C to 150°C

Junction temperature .... 150°C

Power dissipation .... Internally limited

Lead temperature (soldering, 10 sec) .... 300°C

ESD rating (HBM - Human Body Model) 2kV

NOTES:

1. No external voltage applied.
2. SW pin's minimum DC range is -1V, transient is -5V for less than 50ns.
3. Recommended frequency for optimum performance.

Operating Conditions

PV_{IN} .... 5V to 40V

V_{IN} .... 5V to 40V

SW, ILIM .... -1V to 40V(1)

PGOOD, VCC, TON, SS, EN, FB .... -0.3V to 5.5V

Switching frequency .... 400kHz to 800kHz(3)

Junction temperature range .... -40°C to 125°C

JEDEC51 package thermal resistance, θ_{JA} .... 28°C/W

Package power dissipation at 25°C 3.6W

Electrical Characteristics

Unless otherwise noted: T_J = 25°C, V_{IN} = 24V, BST = V_{CC}, SW = AGND = PGND = 0V, C_{VCC} = 4.7µF. Limits applying over the full operating temperature range are denoted by a •.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
Power Supply Characteristics							
V_{IN}	Input voltage range	V_{CC} regulating	•	5.5		40	V
I_{VIN}	V_{IN} input supply current	Not switching, V_{IN} = 24V, V_{FB} = 0.7V	•		0.7	2	mA
I_{VIN}	V_{IN} input supply current	f = 300kHz, R_{ON} = 215kΩ, V_{FB} = 0.58V			12		mA
I_{OFF}	Shutdown current	Enable = 0V, V_{IN} = 12V			1		µA
Enable and Under-Voltage Lock-Out UVLO							
$V_{IH\_EN\_1}$	EN pin rising threshold		•	1.8	1.9	2.0	V
$V_{EN\_H\_1}$	EN pin hysteresis				70		mV
$V_{IH\_EN\_2}$	EN pin rising threshold for DCM/CCM operation		•	2.8	3.0	3.1	V
$V_{EN\_H\_2}$	EN pin hysteresis				100		mV
	V_{CC} UVLO start threshold, rising edge		•	4.00	4.25	4.40	V
	V_{CC} UVLO hysteresis				230		mV

Electrical Characteristics (Continued)

Unless otherwise noted: T_J = 25°C, V_{IN} = 24V, BST = V_{CC}, SW = AGND = PGND = 0V, C_{VCC} = 4.7μF. Limits applying over the full operating temperature range are denoted by a •.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
Reference Voltage							
V_{REF}	Reference voltage	V_{IN} = 5.5V to 40V, V_{CC} regulating		0.596	0.600	0.604	V
			•	0.594	0.600	0.606	V
	DC line regulation	CCM, closed loop, V_{IN} = 5.5V to 40V, applies to any C_{OUT}			±0.15		%
	DC load regulation	CCM, closed loop, applies to any C_{OUT}			±0.05		%
Programmable Constant On-Time							
t_{ON1}	On-time 1	R_{ON} = 6.04kΩ, V_{IN} = 24V	•	85	100	117	ns
	f corresponding to on-time 1	V_{OUT} = 1.8V, V_{IN} = 24V, R_{ON} = 6.04kΩ, I_{OUT} = 1.5A	•	710	830	980	kHz
$t_{ON(MIN)}$	Minimum programmable on-time	R_{ON} = 6.04kΩ, V_{IN} = 24V		85	100	117	ns
t_{ON2}	On-time 2	R_{ON} = 14kΩ, V_{IN} = 24V	•	174	205	236	ns
t_{ON3}	On-time 3	R_{ON} = 35.7kΩ, V_{IN} = 24V	•	407	479	550	ns
	f corresponding to on-time 2	V_{OUT} = 1.8V, V_{IN} = 24V, R_{ON} = 14kΩ, I_{OUT} = 1.5A	•	345	400	470	kHz
	Minimum off-time		•		250	350	ns
Diode Emulation Mode							
	Zero crossing threshold	DC value measured during test			-2		mV
Soft-Start							
	SS charge current		•	-14	-10	-6	μA
	SS discharge current	Fault present	•	1			mA
V_{CC} Linear Regulator							
	V_{CC} output voltage	V_{IN} = 6V to 40V, I_{LOAD} = 0 to 30mA	•	4.8	5.0	5.2	V
		V_{IN} = 5V, I_{LOAD} = 0 to 20mA	•	4.51	4.7		V
Power Good Output							
	Power good threshold			-10	-6.9	-5	%
	Power good hysteresis				1.6	4	%
	Power good sink current			1			mA

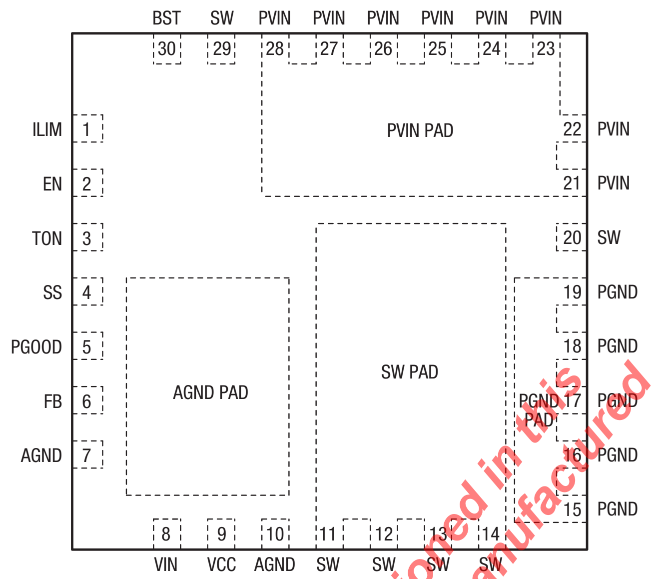
Electrical Characteristics (Continued)

Unless otherwise noted: T_J = 25°C, V_{IN} = 24V, BST = V_{CC}, SW = AGND = PGND = 0V, C_{VCC} = 4.7μF. Limits applying over the full operating temperature range are denoted by a •.

Symbol	Parameter	Conditions	•	Min	Typ	Max	Units
Protection: OCP, OTP, Short-Circuit							
	Hiccup timeout				110		ms
	I_{LIM} pin source current			45	50	55	μA
	I_{LIM} current temperature coefficient				0.4		%/°C
	OCP comparator offset		•	-8	0	8	mV
	Current limit blanking	GL rising > 1V			100		ns
	Thermal shutdown threshold[1]	Rising temperature			150		°C
	Thermal hysteresis[1]				15		°C
	VSCTH feedback pin short-circuit threshold	Percent of V_{REF}, short-circuit is active after PGOOD is asserted	•	50	60	70	%
Output Power Stage							
R_{DSON}	High-side MOSFET R_{DSON}	I_{DS} = 1A			115	160	mΩ
	Low-side MOSFET R_{DSON}				40	59	mΩ
I_{OUT}	Maximum output current		•	1.5A			A
	Maximum ambient temperature at continuous load	V_{IN} = 24V, V_{OUT} = 5V, I_{OUT} = 1.5A, f = 700kHz				100	°C
		V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 1.5A, f = 600kHz				110	°C

NOTE:
1. Guaranteed by design.

Pin Configuration, Top View



Pin Functions

Pin Number	Pin Name	Type	Description
1	ILIM	A	Overcurrent protection programming. Connect with a resistor to SW.
2	EN/MODE	I	Precision enable pin. Pulling this pin above 1.9V will turn the regulator on and it will operate in CCM. If the voltage is raised above 3.0V, then the regulator will operate in DCM / CCM depending on load.
3	TON	A	Constant on-time programming pin. Connect with a resistor to AGND.
4	SS	A	Soft-start pin. Connect an external capacitor between SS and AGND to program the soft-start rate based on the 10μA internal source current.
5	PGOOD	O, OD	Power-good output. This open-drain output is pulled low when V_{OUT} is outside the regulation.
6	FB	A	Feedback input to feedback comparator. Connect with a set of resistors to VOUT and AGND in order to program V_{OUT}.
7, 10, AGND Pad	AGND	A	Signal ground for control circuitry. Connect AGND Pad with a short trace to pins 7 and 10.
8	VIN	A	Supply input for the regulator's LDO. Normally it is connected to PVIN.
9	VCC	A	The output of regulator's LDO. For operation using a 5V rail, VCC should be shorted to VIN.
11-14, 20, 29, SW Pad	SW	PWR	Switch node. The drain of the low-side N-channel MOSFET. The source of the high-side MOSFET is wire-bonded to the SW Pad. Pins 20 and 29 are internally connected to SW pad.
15-19, PGND Pad	PGND	PWR	Ground of the power stage. Should be connected to the system's power ground plane. The source of the low-side MOSFET is wire-bonded to PGND Pad.
21-28, PVIN Pad	PVIN	PWR	Input voltage for power stage. The drain of the high-side N-channel MOSFET.
30	BST	A	High-side driver supply pin. Connect a bootstrap capacitor between BST and pin 29.

NOTE:
A = Analog, I = Input, O = Output, OD = Open Drain, PWR = Power.

Typical Performance Characteristics

Unless otherwise noted: V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 1.5A, f = 600kHz, T_A = 25°C. The application circuit is from the Application Information section.

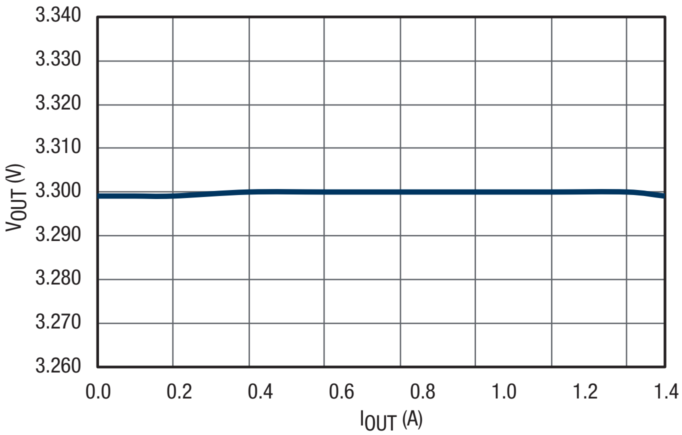


Figure 3.
Load Regulation

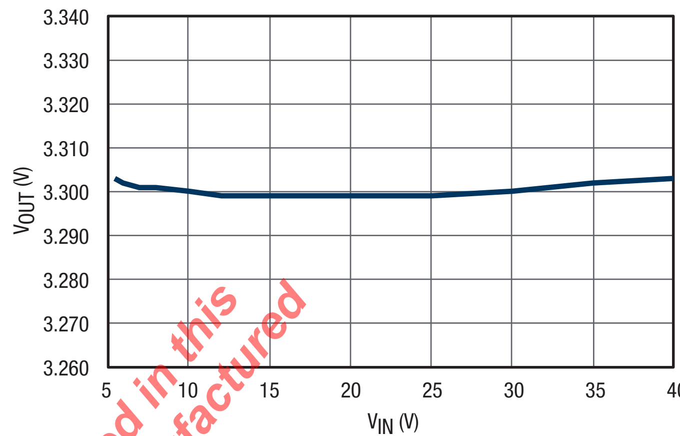


Figure 4.
Line Regulation

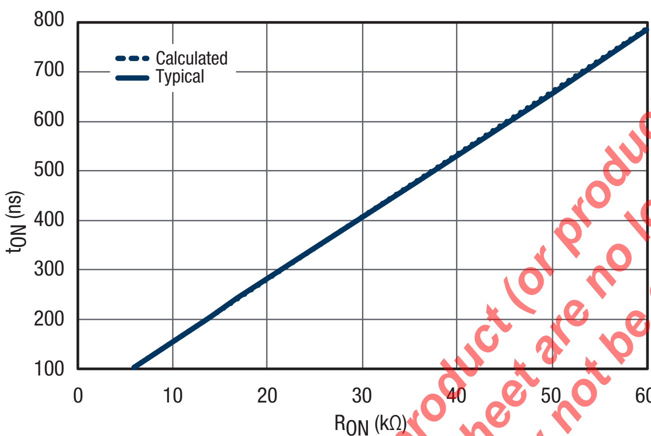


Figure 5.
t_{ON} vs. R_{ON}

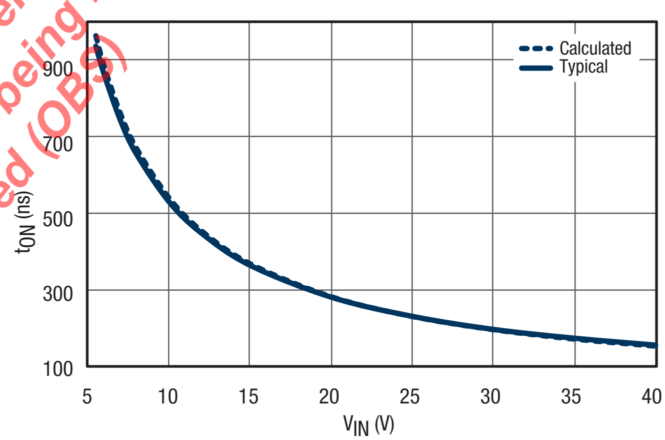


Figure 6.
t_{ON} vs. V_{IN}, R_{ON} = 16.9kΩ

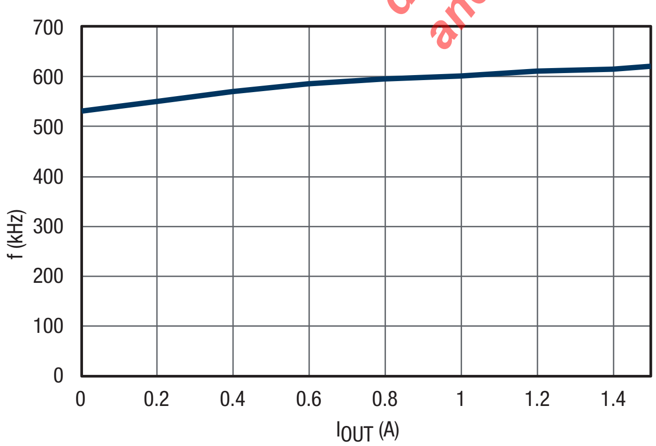


Figure 7.
Frequency vs. I_{OUT}

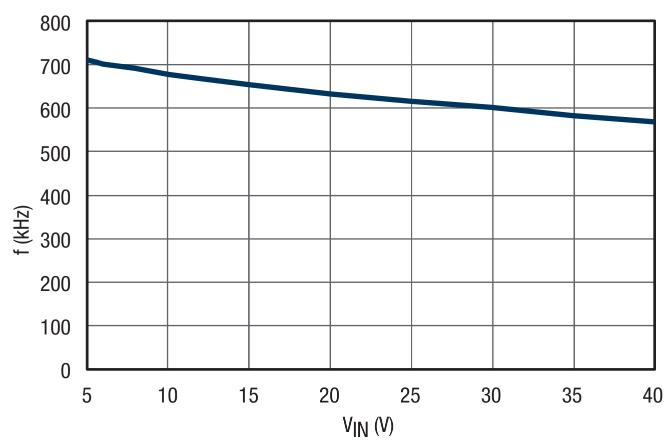


Figure 8.
Frequency vs. V_{IN}

Typical Performance Characteristics (Continued)

Unless otherwise noted: V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 1.5A, f = 600kHz, T_A = 25°C. The application circuit is from the Application Information section.

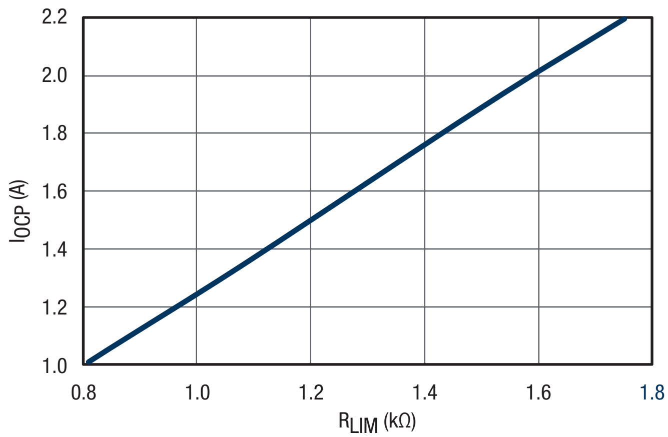


Figure 9.
I_{OCP} vs. R_{LIM}

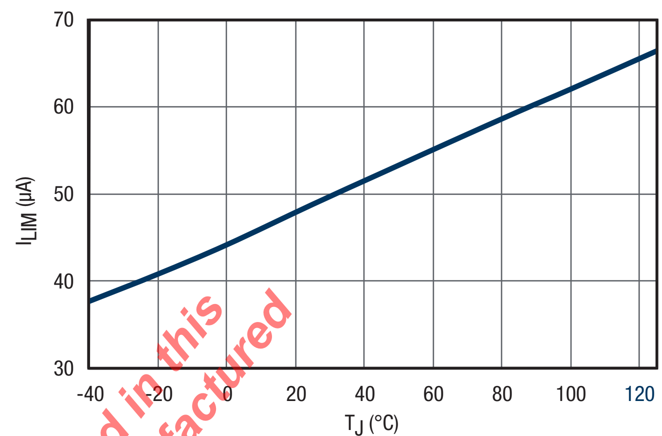


Figure 10.
I_{LIM} vs. Temperature

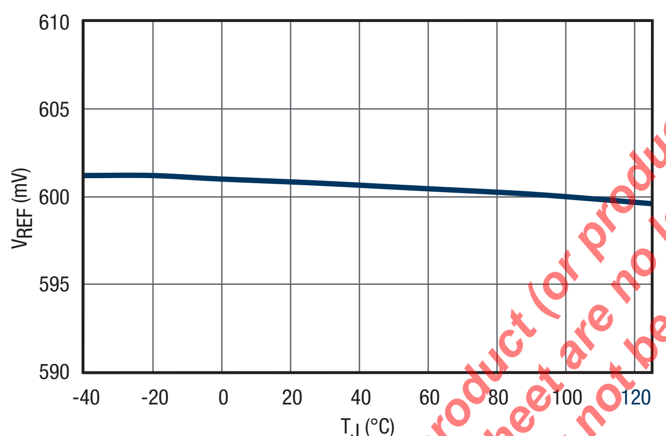


Figure 11.
V_{REF} vs. Temperature

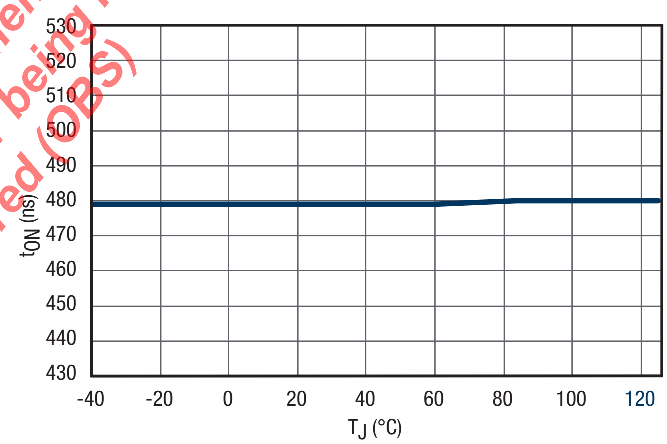


Figure 12.
t_{ON} vs. Temperature, R_{ON} = 35.7kΩ

Typical Performance Characteristics (Continued)

Unless otherwise noted: V_{IN} = 24V, V_{OUT} = 3.3V, I_{OUT} = 1.5A, f = 600kHz, T_A = 25°C. The application circuit is from the Application Information section.

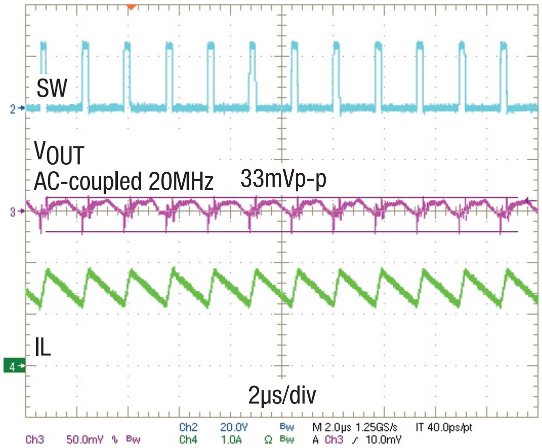


Figure 13.
Steady State, I_{OUT} = 1.5A

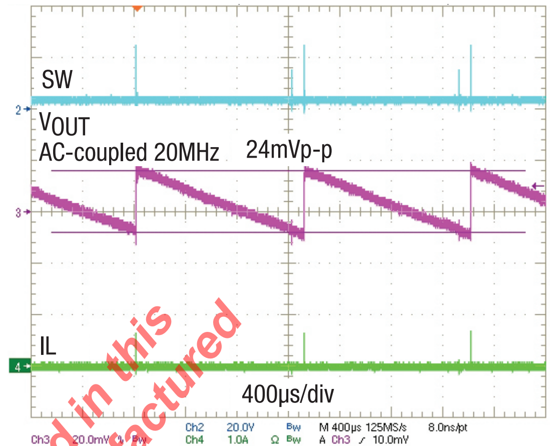


Figure 14.
Steady State, DCM, I_{OUT} = 0A

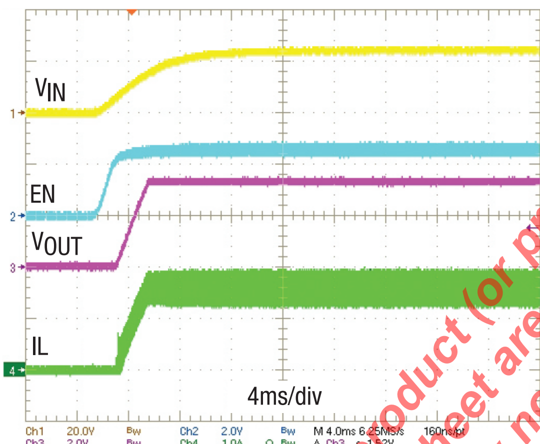


Figure 15.
Power Up, Forced CCM

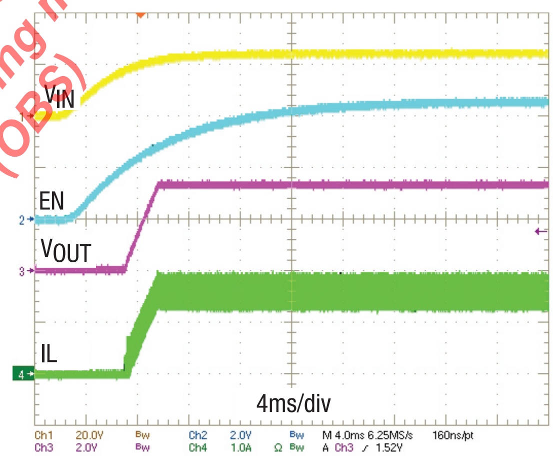


Figure 16.
Power Up, DCM / CCM

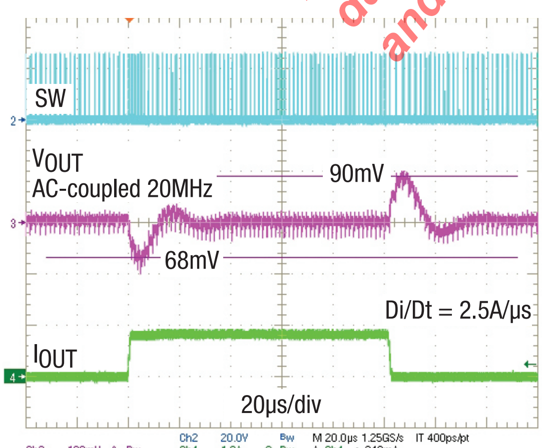


Figure 17.
Load Step, Forced CCM, 0A - 0.8A

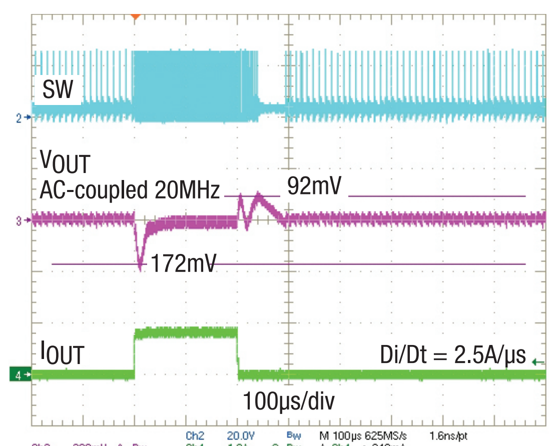


Figure 18.
Load Step, DCM / CCM, 0.05A - 0.85A

Typical Performance Characteristics (Continued)

Efficiency

Unless otherwise noted: $T_{AMBIENT}$ = 25°C, no air flow, L = 6.8μH, inductor losses are included, application circuit is from the Application Information section.

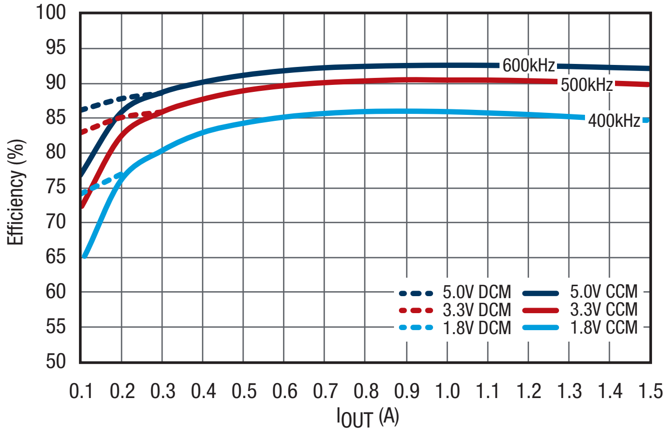


Figure 19.
Efficiency, V_{IN} = 12V

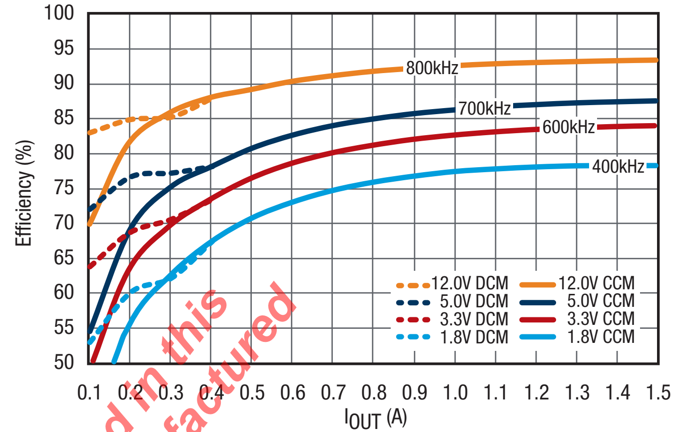


Figure 20.
Efficiency, V_{IN} = 24V

Functional Block Diagram

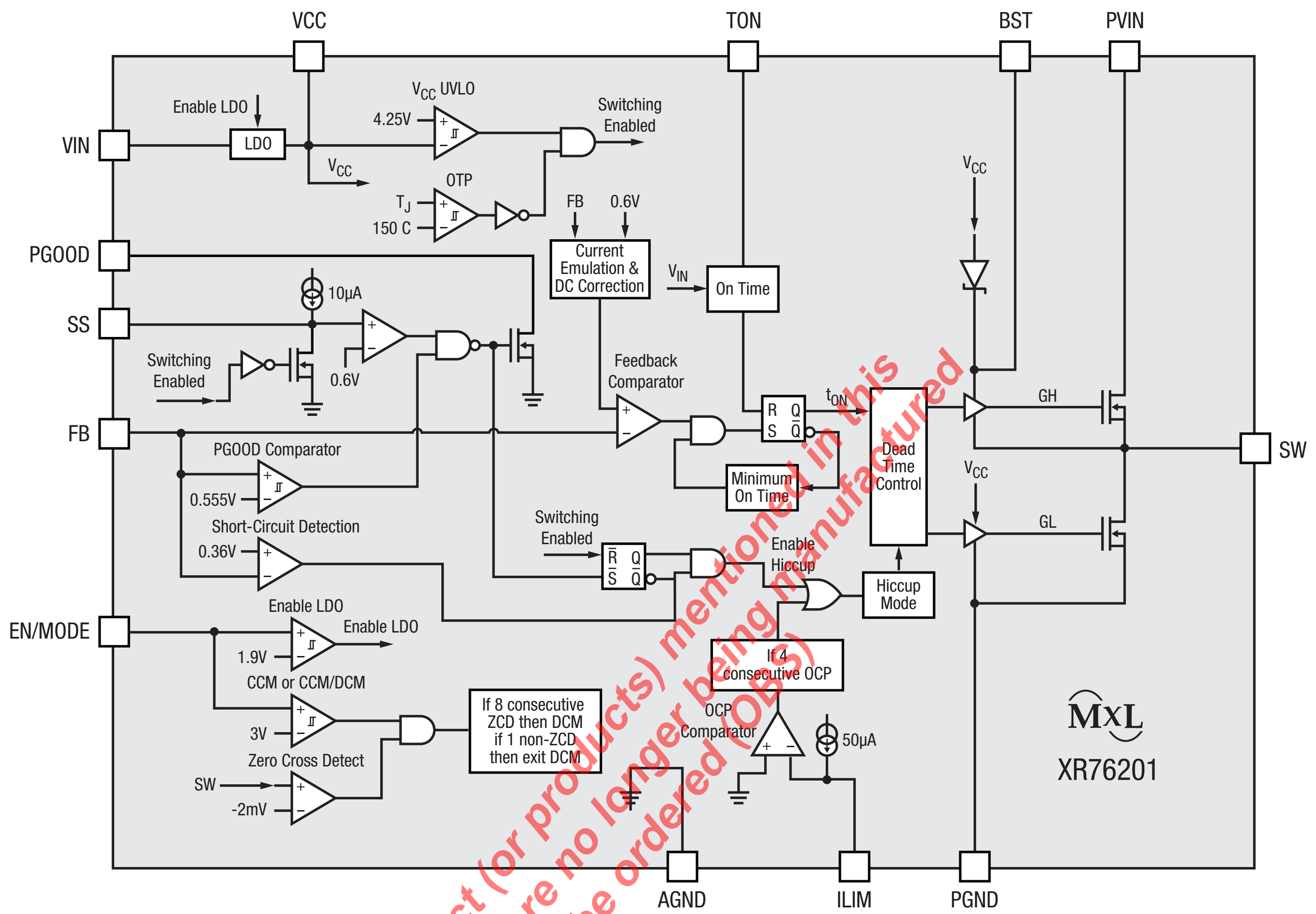


Figure 21. Functional Block Diagram

Applications Information

Functional Description

XR76201 is a synchronous step-down, proprietary emulated current-mode Constant On-Time (COT) regulator. The on-time, which is programmed via R_{ON}, is inversely proportional to V_{IN} and maintains a nearly constant frequency. The emulated current-mode control is stable with ceramic output capacitors.

Each switching cycle begins with GH signal turning on the high-side (control) FET for a preprogrammed time. At the end of the on-time, the high-side FET is turned off and the low-side (synchronous) FET is turned on for a preset minimum time (250ns nominal). This parameter is termed Minimum Off-Time. After the Minimum Off-Time, the voltage at the feedback pin FB is compared to an internal voltage ramp at the feedback comparator. When V_{FB} drops below the ramp voltage, the high-side FET is turned on and the cycle repeats. This voltage ramp constitutes an emulated current ramp and makes possible the use of ceramic capacitors, in addition to other capacitor types, for output filtering.

Enable/Mode Input (EN/MODE)

EN/MODE pin accepts a tri-level signal that is used to control turn on / off. It also selects between two modes of operation: ‘Forced CCM’ and ‘DCM / CCM’. If EN/MODE is pulled below 1.8V, the regulator shuts down. A voltage between 2.0V and 2.8V selects the Forced CCM mode, which will run the regulator in continuous conduction at all times. A voltage higher than 3.1V selects the DCM / CCM mode, which will run the regulator in discontinuous conduction at light loads.

Selecting the Forced CCM Mode

In order to set the regulator to operate in Forced CCM, a voltage between 2.0V and 2.8V must be applied to EN/MODE. This can be achieved with an external control signal that meets the above voltage requirement. Where an external control is not available, the EN/MODE can be derived from V_{IN}. If V_{IN} is well regulated, use a resistor divider and set the voltage to 2.5V. If V_{IN} varies over a wide range, the circuit shown in Figure 22 can be used to generate the required voltage. Note that at V_{IN} of 5.5V and 40V, the nominal Zever voltage is 4.0V and 5.0V respectively. Therefore for V_{IN} in the range of 5.5V to 40V, the circuit shown in Figure 22 will generate the V_{EN} required for Forced CCM.

Selecting the DCM / CCM Mode

In order to set the regulator operation to DCM / CCM, a voltage between 3.1V and 5.5V must be applied to the EN/MODE pin. If an external control signal is available, it can be directly connected to EN/MODE. In applications where an external control is not available, the EN/MODE input can be derived from V_{IN}. If V_{IN} is well regulated, use a resistor divider and set the voltage to 4V. If V_{IN} varies over a wide range, the circuit shown in Figure 23 can be used to generate the required voltage.

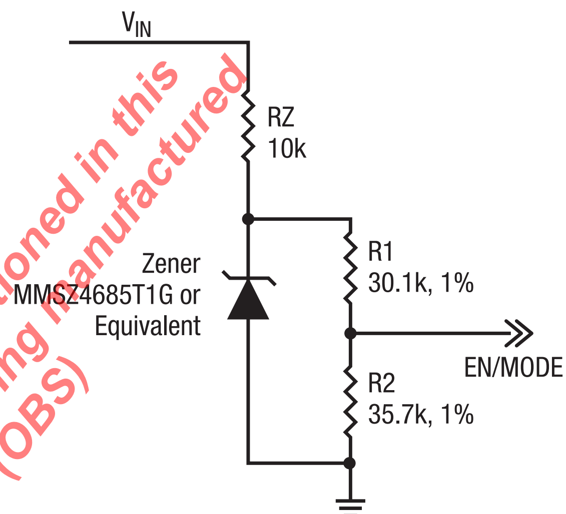


Figure 22.
Selecting Forced CCM by Deriving EN/MODE from V_{IN}

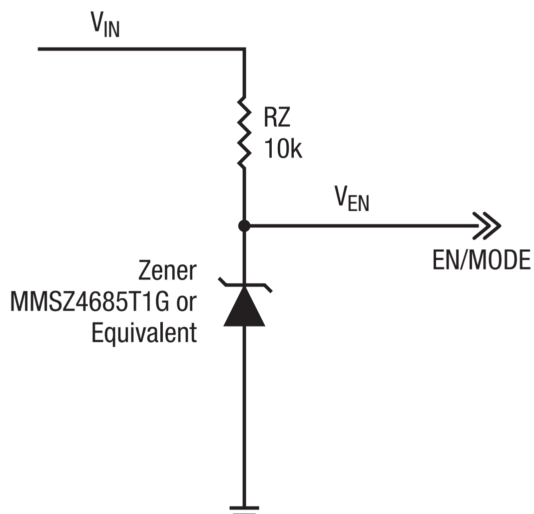


Figure 23.
Selecting DCM/CCM by Deriving EN/MODE from V_{IN}

Applications Information (Continued)

Programming the On-Time

The on-time t_{ON} is programmed via resistor R_{ON} according to following equation:

$$R_{ON} = \frac{V_{IN} \times [t_{ON} - (2.5 \times 10^{-8})]}{3.05 \text{ x } 10^{-10}}$$

A graph of t_{ON} vs. R_{ON}, using the above equation, is compared to typical test data in Figure 5. The graph shows that calculated data matches typical test data within 3%.

The t_{ON} corresponding to a particular set of operating conditions can be calculated based on empirical data from:

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times 0.97 \text{ x } f}$$

Where:

- f is the desired switching frequency at 1.5A

Substituting for t_{ON} in the first equation we get:

$$R_{ON} = \frac{\left(\frac{V_{OUT}}{0.97 \text{ x } f}\right) - [(2.5 \times 10^{-8}) \times V_{IN}]}{(3.05 \times 10^{-10})}$$

Now R_{ON} can be calculated in terms of operating conditions V_{IN}, V_{OUT}, and f using the above equation. At V_{IN} = 24V, I_{OUT} = 1.5A we get the following R_{ON}:

V_{OUT} (V)	f (kHZ)	R_{ON} (kΩ)
12	800	48.7
5	700	22.2
3.3	600	16.6
1.8	400	13.2

Overcurrent Protection (OCP)

If load current exceeds the programmed overcurrent I_{OCP} for four consecutive switching cycles, the module enters the hiccup mode of operation. In hiccup, the MOSFET gates are turned off for 110ms (hiccup timeout). Following the hiccup timeout, a soft-start is attempted. If OCP persists, the hiccup timeout will repeat. The module will remain in hiccup mode until load current is reduced below the programmed I_{OCP}. In order to program the overcurrent protection, use the following equation:

$$R_{LIM} = \frac{(I_{OCP} \times 59m\Omega) + 8mV}{I_{LIM}}$$

where:

- R_{LIM} is resistor value for programming I_{OCP}
- I_{OCP} is the overcurrent threshold to be programmed
- 8mV is the OCP comparator maximum offset
- I_{LIM} is the internal current that generates the necessary OCP comparator threshold (use 45µA).

Note that I_{LIM} has a positive temperature coefficient of 0.4%/°C, Figure 10. This is meant to roughly match and compensate for positive temperature coefficient of the synchronous FET. The above equation is for worst-case analysis and safeguards against premature OCP. Typical value of I_{OCP}, for a given R_{LIM}, will be higher than that predicted by the above equation. A graph of calculated I_{OCP} vs. R_{LIM} is compared to typical I_{OCP} in Figure 9.

Short-Circuit Protection (SCP)

If the output voltage drops below 60% of its programmed value, the module will enter hiccup mode. Hiccup will persist until short-circuit is removed. The SCP circuit becomes active after PGOOD asserts high.

Over-Temperature (OTP)

OTP triggers at a nominal die temperature of 150°C. The gate of switching FET and synchronous FET are turned off. When die temperature cools down to 135°C, soft-start is initiated and operation resumes.

Programming the Output Voltage

Use an external voltage divider as shown in the Application Circuit to program the output voltage V_{OUT}.

$$R_1 = R_2 \times \left(\frac{V_{OUT}}{0.6V} - 1\right)$$

where: R2 has a nominal value of 2kΩ

Programming the Soft-Start

Place a capacitor C_{SS} between the SS and AGND pins to program the soft-start. In order to program a soft-start time of t_{SS}, calculate the required capacitance C_{SS} from the following equation:

$$C_{SS} = t_{SS} \times \frac{10\mu A}{0.6V}$$

Applications Information (Continued)

Feed-Forward Capacitor (C_{FF})

A feed-forward capacitor (C_{FF}) may be necessary depending on the Equivalent Series Resistance (ESR) of C_{OUT}. If only ceramic output capacitors are used for C_{OUT}, then a C_{FF} is necessary. Calculate C_{FF} from:

$$C_{FF} = \frac{1}{2 \times \pi \times R_1 \times 7 \times f_{LC}}$$

where:

- R1 is the resistor that is parallel with C_{FF}
- f_{LC} is calculated by the equation below:

$$f_{LC} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}}$$

The f_{LC} frequency must be less than 11kHz when using ceramic C_{OUT}. If necessary, increase L and / or C_{OUT} in order to meet this constraint.

When using capacitors with higher ESR such as the PANASONIC TPE series, a C_{FF} is not required provided following conditions are met:

1. The frequency of output filter LC double-pole f_{LC} should be less than 11kHz
2. The frequency of ESR Zero $f_{ZERO,ESR}$ should be at least five times larger than f_{LC}

Note that if $f_{ZERO,ESR}$ is less than 5 x f_{LC}, then it is recommended to set the f_{LC} at less than 2kHz. C_{FF} is still not required.

Maximum Allowable Voltage Ripple at FB Pin

Note that the steady-state voltage ripple at feedback pin FB ($V_{FB,RIPPLE}$) must not exceed 50mV in order for the regulator to function correctly. If $V_{FB,RIPPLE}$ is larger than 50mV, then C_{OUT} should be increased as necessary in order to keep the $V_{FB,RIPPLE}$ below 50mV.

Feed-Forward Resistor (R_{FF})

FET switching noise may couple to V_{OUT} through the parasitic capacitance across the inductor and to the FB pin via C_{FF}. Excessive noise at FB will cause poor load regulation. To solve this problem, place a resistor R_{FF} in series with C_{FF}. An R_{FF} value up to 2% of R1 is acceptable.

Applications Information (Continued)

Application Circuit

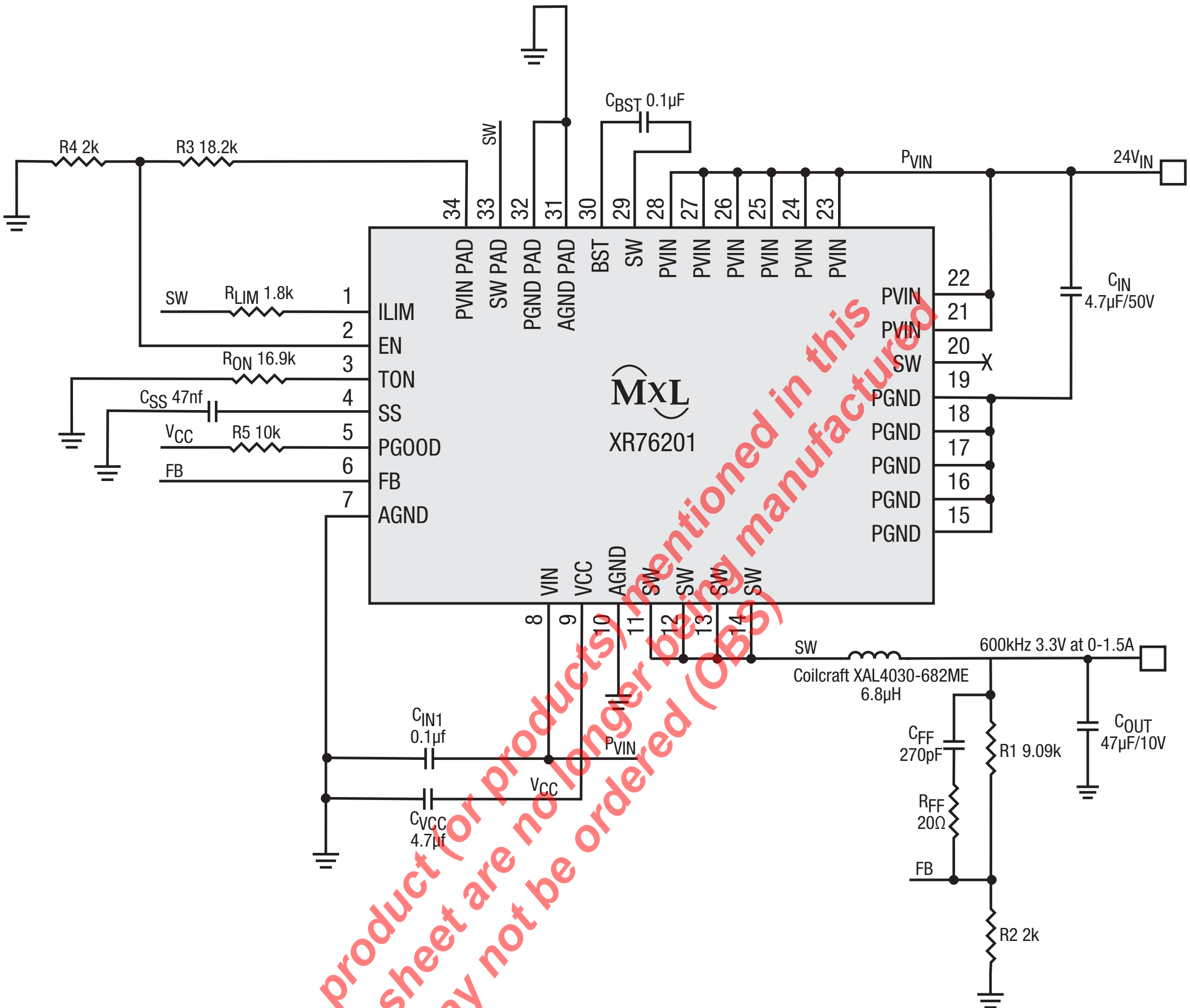
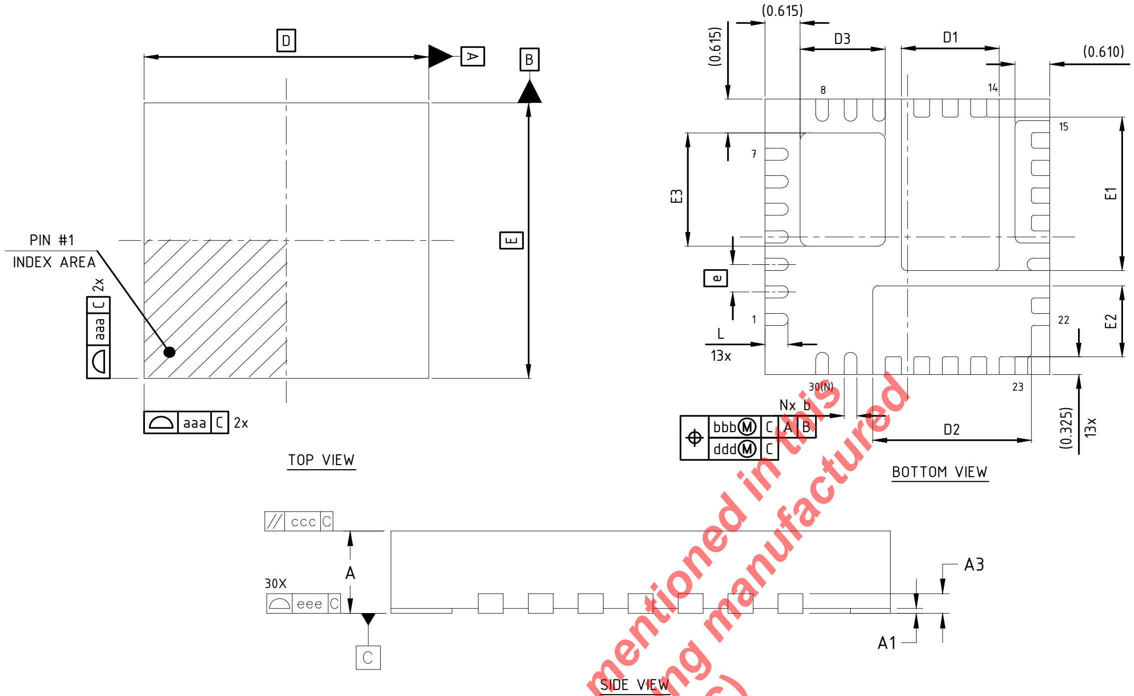


Figure 24. Application Circuit

Mechanical Dimensions



Dimension Table			
Symbol \ Thickness	MINIMUM	NOMINAL	MAXIMUM
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 Ref.	
b	0.18	0.25	0.30
D		5.00 BSC	
E		5.00 BSC	
e		0.50 BSC	
D1	1.570	1.720	1.820
E1	2.635	2.785	2.885
D2	2.635	2.785	2.885
E2	1.135	1.285	1.385
D3	1.345	1.495	1.595
E3	1.903	2.053	2.153
L	0.30	0.40	0.50
aaa		0.05	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
N		30	

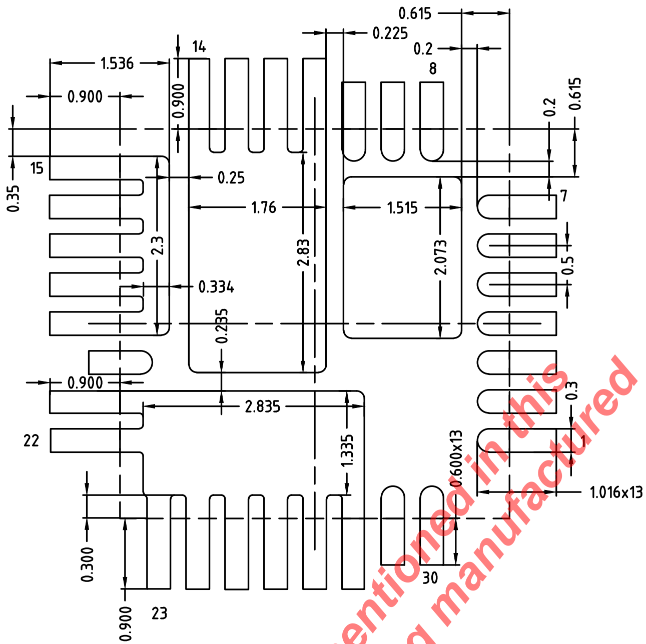
TERMINAL DETAIL

NOTE : ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.

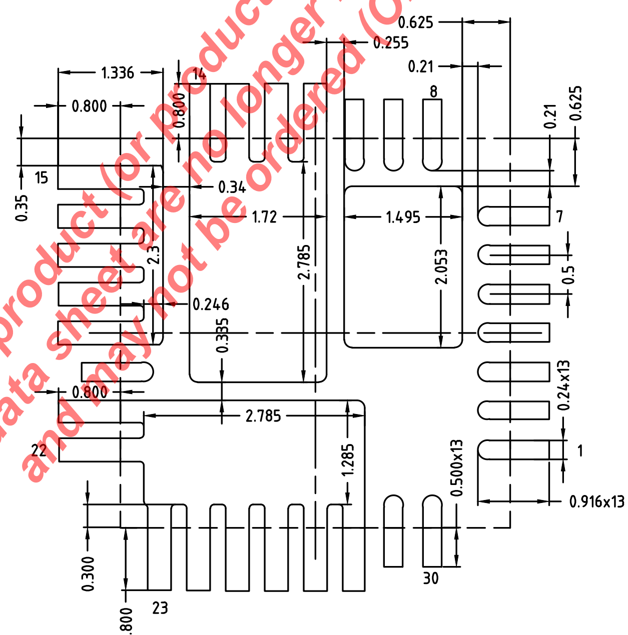
Drawing No.: POD-00000018

Revision: B

Recommended Land Pattern and Stencil



TYPICAL RECOMMENDED LAND PATTERN



TYPICAL RECOMMENDED STENCIL

NOTE : ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.

Drawing No.: POD-00000018

Revision: B

Ordering Information[1]

Part Number	Operating Temperature Range	Package	Packaging Method	Lead-Free
XR76201ELTR	-40°C ≤ T_J ≤ 125°C	QFN 5x5	Tape and Reel	Yes[2]
XR76201EVB	XR76201 Evaluation Board			

NOTE:
1. Refer to www.maxlinear.com/XR76201 for most up-to-date Ordering Information.
2. Visit www.maxlinear.com for additional information on Environmental Rating.

Revision History

Revision	Date	Description
1A	Sept 2016	Initial Release
1B	June 2018	Update to MaxLinear logo. Update format and Ordering Information.
1C	October 2019	Correct block diagram by changing the input gate into the Hiccup Mode from an AND gate to an OR gate. Update ordering information. Add recommended land pattern and stencil.

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