OCTOBER 2007 REV. 1.0.4

GENERAL DESCRIPTION

The XRT75R12 is a twelve channel fully integrated Line Interface Unit (LIU) featuring EXAR's R³ Technology (Reconfigurable, Relayless Redundancy) for E3/DS3/STS-1 applications. The LIU incorporates 12 independent Receivers, Transmitters and Jitter Attenuators in a single 420 Lead TBGA package.

Each channel of the XRT75R12 can be independently configured to operate in E3 (34.368 MHz), DS3 (44.736 MHz) or STS-1 (51.84 MHz). Each transmitter can be turned off and tri-stated for redundancy support or for conserving power.

The XRT75R12's differential receiver provides high noise interference margin and is able to receive data over 1000 feet of cable or with up to 12 dB of cable attenuation.

The XRT75R12 incorporates an advanced crystalless jitter attenuator per channel that can be selected either in the transmit or receive path. The jitter attenuator performance meets the ETSI TBR-24 and Bellcore GR-499 specifications.

The XRT75R12 provides a Parallel Microprocessor Interface for programming and control.

The XRT75R12 supports analog, remote and digital loop-backs. The device also has a built-in Pseudo Random Binary Sequence (PRBS) generator and detector with the ability to insert and detect single bit error for diagnostic purposes.

APPLICATIONS

- E3/DS3 Access Equipment
- DSLAMs
- Digital Cross Connect Systems
- CSU/DSU Equipment
- Routers
- Fiber Optic Terminals

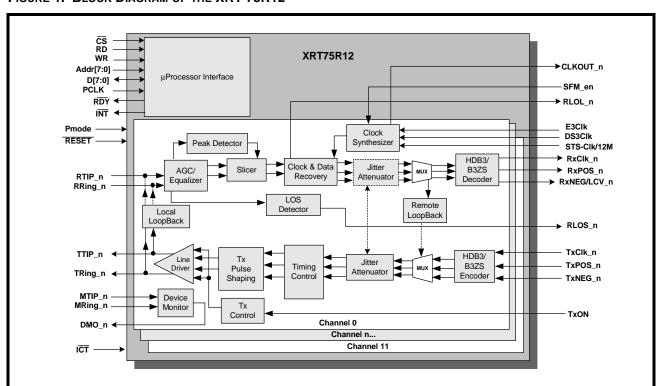


FIGURE 1. BLOCK DIAGRAM OF THE XRT 75R12

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT75R12IB	420 Lead TBGA	-40°C to +85°C

XRT75R12



TWELVE CHANNEL E3/DS3/STS-1 LINE INTERFACE UNIT WITH JITTER ATTENUATOR

REV. 1.0.4

FEATURES

RECEIVER

- R³ Technology (Reconfigurable, Relayless Redundancy)
- On chip Clock and Data Recovery circuit for high input jitter tolerance
- Meets E3/DS3/STS-1 Jitter Tolerance Requirement
- Detects and Clears LOS as per G.775
- Receiver Monitor mode handles up to 20 dB flat loss with 6 dB cable attenuation
- On chip B3ZS/HDB3 encoder and decoder that can be either enabled or disabled
- On-chip clock synthesizer provides the appropriate rate clock from a single 12.288 MHz Clock
- Provides low jitter output clock

TRANSMITTER

- R³ Technology (Reconfigurable, Relayless Redundancy)
- Compliant with Bellcore GR-499, GR-253 and ANSI T1.102 Specification for transmit pulse
- Tri-state Transmit output capability for redundancy applications
- Each Transmitter can be independently turned on or off
- Transmitters provide Voltage Output Drive

JITTER ATTENUATOR

- On chip advanced crystal-less Jitter Attenuator for each channel
- Jitter Attenuator can be selected in Receive, Transmit path, or disabled
- Meets ETSI TBR 24 Jitter Transfer Requirements
- Compliant with jitter transfer template outlined in ITU G.751, G.752, G.755 and GR-499-CORE,1995 standards
- 16 or 32 bits selectable FIFO size

CONTROL AND DIAGNOSTICS

- Parallel Microprocessor Interface for control and configuration
- Supports optional internal Transmit driver monitoring

- Each channel supports Analog, Remote and Digital Loop-backs
- Single 3.3 V ± 5% power supply
- 5 V Tolerant digital inputs
- Available in 420 pin TBGA Thermally enhanced Package
- - 40℃ to 85℃ Industrial Temperature Range

TRANSMIT INTERFACE CHARACTERISTICS

- Accepts either Single-Rail or Dual-Rail data from Terminal Equipment and generates a bipolar signal to the line
- Integrated Pulse Shaping Circuit
- Built-in B3ZS/HDB3 Encoder (which can be disabled)
- Accepts Transmit Clock with duty cycle of 30%-70%
- Generates pulses that comply with the ITU-T G.703 pulse template for E3 applications
- Generates pulses that comply with the DSX-3 pulse template, as specified in Bellcore GR-499-CORE and ANSI T1.102_1993
- Generates pulses that comply with the STSX-1 pulse template, as specified in Bellcore GR-253-CORE
- Transmitter can be turned off in order to support redundancy designs

RECEIVE INTERFACE CHARACTERISTICS

- Integrated Adaptive Receive Equalization (optional) for optimal Clock and Data Recovery
- Declares and Clears the LOS defect per ITU-T G.775 requirements for E3 and DS3 applications
- Meets Jitter Tolerance Requirements, as specified in ITU-T G.823_1993 for E3 Applications
- Meets Jitter Tolerance Requirements, as specified in Bellcore GR-499-CORE for DS3 Applications
- Declares Loss of Lock (LOL) Alarm
- Built-in B3ZS/HDB3 Decoder (which can be disabled)
- Recovered Data can be muted while the LOS Condition is declared
- Outputs either Single-Rail or Dual-Rail data to the Terminal Equipment



TABLE OF CONTENTS

GENERAL DESCRIPTION	
APPLICATIONS	
FIGURE 1. BLOCK DIAGRAM OF THE XRT 75R12	
ORDERING INFORMATION	
FEATURES	2
Transmit Interface Characteristics	
Receive Interface Characteristics	
TABLE OF CONTENTS	1
PIN DESCRIPTIONS (BY FUNCTION)	3
SYSTEM-SIDE TRANSMIT INPUT AND TRANSMIT CONTROL PINS	
System-Side Receive Output and Receive Control Pins	
RECEIVE LINE SIDE PINS	
CLOCK INTERFACE.	_
GENERAL CONTROL PINS	
Power Supply Pins	
GROUND PINS	
TABLE 1: PIN LIST BY PIN NUMBER	
FUNCTIONAL DESCRIPTION	18
1.0 R3 TECHNOLOGY (RECONFIGURABLE, RELAYLESS REDUNDANCY)	. 18
1.1 NETWORK ARCHITECTURE	
FIGURE 2. NETWORK REDUNDANCY ARCHITECTURE	
2.0 CLOCK SYNTHESIZER	.19
FIGURE 3. SIMPLIFIED BLOCK DIAGRAM OF THE INPUT CLOCK CIRCUITRY DRIVING THE MICROPROCESSOR	
Table 2: Reference Clock Performance Specifications	
2.1 CLOCK DISTRIBUTION	
FIGURE 4. CLOCK DISTRIBUTION CONGIFURED IN E3 MODE WITHOUT USING SFM	
3.0 THE RECEIVER SECTION	
FIGURE 5. RECEIVE PATH BLOCK DIAGRAM	
3.1 RECEIVE LINE INTERFACE	
3.2 ADAPTIVE GAIN CONTROL (AGC)	
3.3 RECEIVE EQUALIZER	
FIGURE 7. ACG/EQUALIZER BLOCK DIAGRAM	
3.3.1 RECOMMENDATIONS FOR EQUALIZER SETTINGS	
3.4 CLOCK AND DATA RECOVERY	22
3.4.1 DATA/CLOCK RECOVERY MODE	22
3.4.2 TRAINING MODE	
3.5 LOS (LOSS OF SIGNAL) DETECTOR	
3.5.1 DS3/STS-1 LOS CONDITION	
TABLE 3: THE ALOS (ANALOG LOS) DECLARATION AND CLEARANCE THRESHOLDS FOR A GIVEN SETTING OF REQEN (DS3 AND STS- PLICATIONS)	
3.5.2 DISABLING ALOS/DLOS DETECTION	
3.5.3 E3 LOS CONDITION:	
FIGURE 8. LOSS OF SIGNAL DEFINITION FOR E3 AS PER ITU-T G.775	23
Figure 9. Loss of Signal Definition for E3 as per ITU-T G.775	. 24
3.5.4 INTERFERENCE TOLERANCE	
FIGURE 10. INTERFERENCE MARGIN TEST SET UP FOR DS3/STS-1	
Figure 11. Interference Margin Test Set up for E3	
3.5.5 MUTING THE RECOVERED DATA WITH LOS CONDITION:	
Figure 12. Receiver Data output and code violation timing	
3.6 B3ZS/HDB3 DECODER	
4.0 THE TRANSMITTER SECTION	
FIGURE 13. TRANSMIT PATH BLOCK DIAGRAM	
4.1 TRANSMIT DIGITAL INPUT INTERFACE	
FIGURE 14. TYPICAL INTERFACE BETWEEN TERMINAL EQUIPMENT AND THE XRT75R12 (DUAL-RAIL DATA)	
FIGURE 15. TRANSMITTER TERMINAL INPUT TIMING	
FIGURE 16. SINGLE-RAIL OR NRZ DATA FORMAT (ENCODER AND DECODER ARE ENABLED)	
4.2 TRANSMIT CLOCK	29



TWELVE CHANNEL E3/DS3/STS-1 LINE INTERFACE UNIT WITH JITTER ATTENUATOR 5.0 JITTER37 6.0 DIAGNOSTIC FEATURES41 Figure 29. PRBS MODE 41 7.0 MICROPROCESSOR INTERFACE BLOCK45 FIGURE 35. ASYNCHRONOUS µP INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS.......47 FIGURE 36. SYNCHRONOUS µP INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS.......48 Table 17. Command Register Address Map, within the XRT75R12. THE GLOBAL/CHIP-LEVEL REGISTERS57 REGISTER DESCRIPTION - GLOBAL REGISTERS58 Table 20: APS/Redundancy Recieve Control Register - CR8 (Address Location = 0x08) 58





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REV. 1.0.4 TWELVE CHANNEL E3/DS3/STS-1 LINE INTERFACE UNIT WITH JITTER ATTENUATOR

	TABLE 21: APS/REDUNDANCY TRANSMIT CONTROL REGISTER - CR128 (ADDRESS LOCATION = 0x80)	59
	TABLE 22: APS/REDUNDANCY RECIEVE CONTROL REGISTER - CR136 (ADDRESS LOCATION = 0x88)	59
	TABLE 23: CHANNEL LEVEL INTERRUPT ENABLE REGISTER - CR96 (ADDRESS LOCATION = 0x60)	60
	TABLE 24: CHANNEL LEVEL INTERRUPT STATUS REGISTER - CR97 (ADDRESS LOCATION = 0x61)	
	TABLE 25: CHANNEL LEVEL INTERRUPT ENABLE REGISTER - CR224 (ADDRESS LOCATION = 0xE0)	
	TABLE 26: CHANNEL LEVEL INTERRUPT STATUS REGISTER - CR225 (ADDRESS LOCATION = 0xE1)	63
	Table 27: Device/Part Number Register - CR110 (Address Location = 0x6E)	
	TABLE 28: CHIP REVISION NUMBER REGISTER - CR111 (ADDRESS LOCATION = 0x6F)	64
	THE PER-CHANNEL REGISTERS	
	REGISTER DESCRIPTION - PER CHANNEL REGISTERS	65
	TABLE 29: XRT75R12 REGISTER MAP SHOWING INTERRUPT ENABLE REGISTERS (IER_N)	65
	TABLE 30: SOURCE LEVEL INTERRUPT ENABLE REGISTER - CHANNEL N ADDRESS LOCATION = 0XM1	66
	TABLE 31: XRT75R12 REGISTER MAP SHOWING INTERRUPT STATUS REGISTERS (ISR_N)	67
	TABLE 32: SOURCE LEVEL INTERRUPT STATUS REGISTER - CHANNEL N ADDRESS LOCATION = 0XM2	68
	TABLE 33: XRT75R12 REGISTER MAP SHOWING ALARM STATUS REGISTERS (AS_N)	69
	TABLE 34: ALARM STATUS REGISTER - CHANNEL N ADDRESS LOCATION = 0XM3	69
	TABLE 35: XRT75R12 REGISTER MAP SHOWING TRANSMIT CONTROL REGISTERS (TC_N)	
	TABLE 36: TRANSMIT CONTROL REGISTER - CHANNEL N ADDRESS LOCATION = 0xM4	_
	TABLE 37: XRT75R12 REGISTER MAP SHOWING RECEIVE CONTROL REGISTERS (RC_N)	75
	Table 38: Receive Control Register - Channel in Address Location = 0xm5	
	TABLE 39: XRT75R12 REGISTER MAP SHOWING CHANNEL CONTROL REGISTERS (CC_N)	
	TABLE 40: CHANNEL CONTROL REGISTER - CHANNEL N ADDRESS LOCATION = 0XM6	
	TABLE 41: XRT75R12 REGISTER MAP SHOWING JITTER ATTENUATOR CONTROL REGISTERS (JA_N)	
	TABLE 42: JITTER ATTENUATOR CONTROL REGISTER - CHANNEL N ADDRESS LOCATION = 0XM7	
	TABLE 43: XRT75R12 REGISTER MAP SHOWING ERROR COUNTER MSBYTE REGISTERS (EM_n)	
	TABLE 44: ERROR COUNTER MSBYTE REGISTER - CHANNEL N ADDRESS LOCATION = 0XMA	
	TABLE 45: XRT75R12 REGISTER MAP SHOWING ERROR COUNTER LSBYTE REGISTERS (EL_N)	
	TABLE 46: ERROR COUNTER LSBYTE REGISTER - CHANNEL N ADDRESS LOCATION = 0xmB	
	TABLE 47: XRT75R12 REGISTER MAP SHOWING ERROR COUNTER HOLDING REGISTERS (EH_N)	
	TABLE 48: ERROR COUNTER HOLDING REGISTER - CHANNEL N ADDRESS LOCATION = 0XMC	
8.0	.0 ELECTRICAL CHARACTERISTICS	84
	TABLE 49: ABSOLUTE MAXIMUM RATINGS	_
	TABLE 50: DC ELECTRICAL CHARACTERISTICS:	_
	ORDERING INFORMATION	86
	FIGURE 37. PACKAGE DIMENSIONS	86
	REVISION HISTORY	87

REV. 1.0.4

PIN DESCRIPTIONS (BY FUNCTION)

SYSTEM-SIDE TRANSMIT INPUT AND TRANSMIT CONTROL PINS

Pin#	SIGNAL NAME	Түре	DESCRIPTION
P4	TxON	-	Transmit On/Off Input Upon power up, the transmitters are powered on. Turning the transmitters On or Off is selected through the microprocessor interface by programming the appropriate channel register if this pin is pulled "High". If the TxON pin is pulled "Low", all 12 transmitters are powered off. Note: TxON is ideal for redundancy applications. See the R³ Technology section of this datasheet for more details. Internally pulled "High".
F22 AA22 H22 Y23 G26 AA25 G1 AA2 H5 Y4 F5 AA5	TxCLK0 TxCLK1 TxCLK2 TxCLK3 TxCLK4 TxCLK5 TxCLK6 TxCLK6 TxCLK7 TxCLK8 TxCLK8 TxCLK9 TxCLK10 TxCLK11	ı	 Transmit Clock Input These input pins have three functions: They function as the timing source for the Transmit Section of the corresponding channel within the XRT75R12. They are used by the Transmit Section of the LIU IC to sample the corresponding TxPOS_n and TxNEG_n input pins. They are used to clock the PRBS generator Note: The user is expected to supply a 44.736MHz ± 20ppm clock signal (for DS3 applications), 34.368MHz ± 20 ppm clock signal (for E3 applications) or a 51.84MHz ± 4.6ppm clock signal (for STS-1, Stratum 3E or better applications).
E23 AB24 J22 AA23 G25 AA26 G2 AA1 J5 AA4 E4 AB3	TxPOS0 TxPOS1 TxPOS2 TxPOS3 TxPOS4 TxPOS5 TxPOS6 TxPOS7 TxPOS8 TxPOS9 TxPOS10 TxPOS11		Transmit Positive Data Input The function of these digitial input pins depends upon whether the corresponding channel has been configured to operate in the Single-Rail or Dual-Rail Mode. Single Rail Mode - Transmit Data Input Operating in the Single-Rail Mode; all transmit input data will be serially applied to this input pin. This signal will be latched into the Transmit Section circuitry on the active edge of the TxCLK_n signal. The Transmit Section of the LIU IC will then encode this data into either the B3ZS line code (for DS3 and STS-1 applications) or the HDB3 line code (for E3 applications). Dual Rail Mode - Transmit Positive Data Input In the Dual-Rail Mode, the user should apply a pulse to this input pin when a positive-polarity pulse is to be transmitted onto the line. This signal will be latched into the Transmit Section circuitry upon the active edge of the TxCLK_n signal,. The Transmit Section of the LIU IC will NOT encode this data into either the B3ZS or HDB3 line codes. If the user configures the LIU IC to operate in the Dual-Rail Mode, B3ZS/HDB3 encoding must have already been done prior to this input.

SYSTEM-SIDE TRANSMIT INPUT AND TRANSMIT CONTROL PINS

Pin#	SIGNAL NAME	Түре	DESCRIPTION
C25	TxNEG0	I	Transmit Negative Data Input
AB25	TxNEG1		When a Channel has been configured to operate in the Dual-Rail Mode,
H23	TxNEG2		the user should apply a pulse to this input pin anytime the Transmit Section
W23	TxNEG3		of the LIU IC to generate a negative-polarity pulse onto the line. This signal
H24	TxNEG4		will be latched into the Transmit Section circuitry upon the active edge of the TxCLK_n signal.
Y26	TxNEG5		
H3	TxNEG6		Note: In the Single-Rail Mode, this input pin has no function, and should be tied to GND.
Y1	TxNEG7		be fied to GIVD.
H4	TxNEG8		
W4	TxNEG9		
C2	TxNEG10		
AB2	TxNEG11		
B24	TTip0	0	Transmit TTIP Output - Positive Polarity Signal
AE24	TTip1		These output pins along with the corresponding TRING_n output pins,
C20	TTip2		function as the Transmit DS3/E3/STS-1 Line output signal drivers for a
AD20	TTip3		given channel of the XRT75R12.
C16	TTip4		Connect this signal and the corresponding TRING_n output signal to a 1:1
AD16	TTip5		transformer.
C11	TTip6		Whenever the Transmit Section of the Channel generates and transmits a positive-polarity pulse onto the line, this output pin will be pulsed to a high
AD11	TTip7		ervoltage than its corresponding TRING_n output pins.
C7	TTip8		Conversely, whenever the Transmit Section of the Channel generates and
AD7	TTip9		transmit a negative-polarity pulse onto the line, this output pin will be
C3	TTip10		pulsed to a lower voltage than its corresponding TRING_n output pin.
AD3	TTip11		Note: This output pin will be tri-stated whenever the TxON input pin or bit-
			field is set to "0".
C24	TRing0	0	Transmit Ring Output - Negative Polarity Signal
AD24	TRing1		These output pins along with the corresponding TTIP_n output pins, func-
B20	TRing2		tion as the Transmit DS3/E3/STS-1 Line output signal drivers for a given
AE20	TRing3		channel, within the XRT75R12.
B16	TRing4		Connect this signal and the corresponding TTIP_n output signal to a 1:1 transformer.
AE16	TRing5		Whenever the Transmit Section of the Channel generates and transmits a
B11	TRing6		positive-polarity pulse onto the line, this output pin will be pulsed to a lower
AE11	TRing7		voltage than its corresponding TTIP_n output pin.
B7	TRing8		Conversely, whenever the Transmit Section of the Channel generates and
AE7	TRing9		transmit a negative-polarity pulse onto the line, this output pin will be
В3	TRing10		pulsed to a higher voltage than its corresponding TTIP_n output pin.
AE3	TRing11		Note: This output pin will be tri-stated whenever the TxON input pin or bit-field is set to "0".

REV. 1.0.4

SYSTEM-SIDE TRANSMIT INPUT AND TRANSMIT CONTROL PINS

Pin#	SIGNAL NAME	Түре	DESCRIPTION
C23	MTip0	I	Monitor Tip Input - Positive Polarity Signal
AD23	MTip1		These input pins along with MRing_n function as the Transmit Drive Moni-
D19	MTip2		tor Output (DMO) input monitoring pins. (1) To monitor the Transmit Out-
AC19	MTip3		put line signal and (2) to perform this monitoring externally, then this pin
D15	MTip4		MUST be connected to the corresponding TTIP_n output pin via a 270Ω series resistor. Similarly, the MRING_n input pin MUST also be connected
AC15	MTip5		to its corresponding TRING_n output pin via a 270Ω series resistor.
E11	MTip6		The MTIP_n and MRING_n input pins will continuously monitor the Trans-
AB11	MTip7		mit Output line signal via the TTIP_n and TRING_n output pins for bipolar
E8	MTip8		activity. If these pins do not detect any bipolar activity for 128 bit periods,
AB8	MTip9		then the Transmit Drive Monitor circuit will drive the corresponding DMO_n
C4	MTip10		output pin "High" in order to denote a possible fault condition in the Transmit Output Line signal path.
AD4	MTip11		Note: These input pins are inactive if the user chooses to internally
			monitor the Transmit Output line signal.
D23	MRing0	1	Monitor Ring Input
AC23	MRing1		These input pins along with MTIP_n function as the Transmit Drive Monitor
E19	MRing2		Output (DMO) input monitoring pins. (1) To monitor the Transmit Output
AB19	MRing3		line signal and (2) to perform this monitoring externally, then this input pin
E16	MRing4		MUST be connected to the corresponding TRING_n output pin via a 270Ω series resistor. Similarly, the MTIP_n input pin MUST be connected to its
AB16	MRing5		corresponding TTIP_n output pin via a 270Ω series resistor.
D10	MRing6		The MTIP_n and MRING_n input pins will continuously monitor the Trans-
AC10	MRing7		mit Output line signal via the TTIP_n and TRING_n output pins for bipolar
D8	MRing8		activity. If these pins do not detect any bipolar activity for 128 bit periods,
AC8	MRing9		then the Transmit Drive Monitor circuit will drive the corresponding DMO_n
D4	MRing10		output pin "High" to indicate a possible fault condition in the Transmit Output Line signal path.
AC4	MRing11		Note: These input pins are inactive if the user chooses to internally
			monitor the Transmit Output line signal.
N3	DMO0	0	Drive Monitor Output
N4	DMO1		These output signals are used to indicate a fault condition within the Trans-
N5	DMO2		mit Output signal path.
N1	DMO3		This output pin will toggle "High" anytime the Transmit Drive Monitor circuitry either, via the corresponding MTIP and MRING input pins or inter-
M1	DMO4		nally, detects no bipolar pulses via the Transmit Output line signal (e.g., via
L2	DMO5		the TTIP_m and TRING_m output pins) for 128 bit-periods.
M2	DMO6		This output pin will be driven "Low" anytime the Transmit Drive Monitor cir-
M3 M4	DMO7 DMO8		cuitry has detected at least one bipolar pulse via the Transmit Output line
M4 M5	DMO8 DMO9		signal within the last 128 bit periods.
M5 K2	DMO9 DMO10		
J1	DMO10 DMO11		
31	DIVIOTI		



SYSTEM-SIDE RECEIVE OUTPUT AND RECEIVE CONTROL PINS

Pin#	SIGNAL NAME	Түре	DESCRIPTION
D25 AD25 G23 AA24 J24 U24 J3 U3 G4 AA3 D2 AD2	RLOS0 RLOS1 RLOS2 RLOS3 RLOS4 RLOS5 RLOS6 RLOS7 RLOS8 RLOS9 RLOS10 RLOS11	0	Receive Loss of Signal Output Indicator This output pin indicates Loss of Signal (LOS) Defect condition for the corresponding channel. "Low" - Indicates that the corresponding Channel is NOT currently declaring the LOS defect condition. "High" - Indicates that the corresponding Channel is currently declaring the LOS defect condition.
G22 AB26 K22 U22 L24 W25 L3 W2 K5 U5 G5 AB1	RLOL0 RLOL1 RLOL2 RLOL3 RLOL4 RLOL5 RLOL6 RLOL7 RLOL8 RLOL9 RLOL10 RLOL11	0	Receive Loss of Lock Output Indicator This output pin indicates Loss of Lock (LOL) condition for the corresponding channel. "Low" - Indicates that the corresponding Channel is NOT declaring the LOL condition. "High" - Indicates that the corresponding Channel is currently declaring the LOL condition. Note: The Receive Section of a given channel will declare the LOL condition anytime the frequency of the Recovered Clock (RCLK) signal differs from that of the reference clock programmed for that channel by 0.5% or more.
E25 AD26 G24 Y24 L22 T22 L5 T5 G3 Y3 E2 AD1	RxPOS0 RxPOS1 RxPOS2 RxPOS3 RxPOS4 RxPOS5 RxPOS6 RxPOS7 RxPOS8 RxPOS9 RxPOS10 RxPOS11	0	Receive Positive Data Output The function of these output pins depends upon whether the channel has been configured to operate in the Single-Rail or Dual-Rail Mode. Dual-Rail Mode - Receive Positive Polarity Data Output If the channel has been configured to operate in the Dual-Rail Mode, then all positive-polarity data will be output via this pin. The negative-polarity data will be output via the corresponding RxNEG_n pin. In other words, the Receive Section of the corresponding Channel will pulse this output pin "High" for one period of RCLK_n anytime it receives a positive-polarity pulse via the RTIP/RRING input pins. The data output via this pin is updated upon the active edge of RxCLK_n output clock signal. Single-Rail Mode - Receive Data Output In the Single-Rail Mode, all Receive (or Recovered) data will be output via this pin. The data output via this pin is updated upon the active edge of RxCLK_n output clock signal.

XRT75R12



TWELVE CHANNEL E3/DS3/STS-1 LINE INTERFACE UNIT WITH JITTER ATTENUATOR

REV. 1.0.4

SYSTEM-SIDE RECEIVE OUTPUT AND RECEIVE CONTROL PINS

Pin#	SIGNAL NAME	Түре	DESCRIPTION
F23	RxNEG/LCV0	0	Receive Negative Data Output/Line Code Violation
AC26	RxNEG/LCV1		The function of these pins depends on whether the XRT75R12 is configured in
F24	RxNEG/LCV2		Single Rail or Dual Rail mode.
U23	RxNEG/LCV3		Dual-Rail Mode - Receive Negative Polarity Data Output
L23	RxNEG/LCV4		In the Dual-Rail Mode, all negative-polarity data will be output via this pin. The
T24	RxNEG/LCV5		positive-polarity data will be output via the corresponding RxPOS_n output pin. In other words, the Receive Section of the corresponding Channel will pulse this
L4	RxNEG/LCV6		output pin "High" for one period of RxCLK_n anytime it receives a negative-
T3	RxNEG/LCV7		polarity pulse via the RTIP/RRING input pins.
F3	RxNEG/LCV8		The data output via this pin is updated upon the active edge of the RCLK_n
U4	RxNEG/LCV9		output clock signal.
F4	RxNEG/LCV10		Single-Rail Mode - Line Code Violation Indicator Output
AC1	RxNEG/LCV11		In the Single-Rail Mode, this output pin will function as the Line Code Violation indicator output.
			In this configuration, the Receive Section of the Channel will pulse this output pin "High" for at least one RCLK period whenever it detects either an LCV (Line Code Violation) or an EXZ (Excessive Zero Event).
			The data that is output via this pin is updated upon the active edge of the RCLK_n output clock signal.
E24	RxCLK0	0	Receive Clock Output
AC25	RxCLK1		This output pin functions as the Receive or recovered clock signal. All Receive
J23	RxCLK2		(or recovered) data will output via the RxPOS_n and RxNEG_n outputs upon
V23	RxCLK3		the active edge of this clock signal.
K24	RxCLK4		Additionally, if the device/channel has been configured to operate in the Single-
T23	RxCLK5		Rail Mode, then the RNEG_n/LCV_n output pins will also be updated upon the active edge of this clock signal.
K3	RxCLK6		dout o dago of the diodit digital.
T4	RxCLK7		
J4	RxCLK8		
V4	RxCLK9		
E3	RxCLK10		
AC2	RxCLK11		



RECEIVE LINE SIDE PINS

Pin#	SIGNAL NAME	Түре	DESCRIPTION
B22	RTip0	I	Receive TIP Input
AE22	RTip1		These input pins along with the corresponding RRing_n input pin function as the
B18	RTip2		Receive DS3/E3/STS-1 Line input signal for a given channel of the XRT75R12.
AE18	RTip3		Cconnect this signal and the corresponding RRING_n input signal to a 1:1
A14	RTip4		transformer.
AF14	RTip5		Whenever the RTIP/RRING input pins are receiving a positive-polarity pulse
D13	RTip6		within the incoming DS3, E3 or STS-1 line signal, this input pin will be pulsed to a higher voltage than its corresponding RRING_n input pin.
AC13	RTip7		Conversely, whenever the RTIP/RRING input pins are receiving a negative-
B9	RTip8		polarity pulse within the incoming DS3, E3 or STS-1 line signal, this input pin
AE9	RTip9		will be pulsed to a lower voltage than its corresponding RRING_n input pin.
B5	RTip10		
AE5	RTip11		
C22	RRing0	I	Receive Ring Input
AD22	RRing1		These input pins along with the corresponding RTIP_n input pin function as the
C18	RRing2		Receive DS3/E3/STS-1 Line input signal for a given channel of the XRT75R12.
AD18	RRing3		Connect this signal and the corresponding RTIP_n input signal to a 1:1 trans-
B14	RRing4		former. (See Figure 6)
AE14	RRing5		Whenever the RTIP/RRING input pins are receiving a positive-polarity pulse within the incoming DS3, E3 or STS-1 line signal, then this input pin will be
C13	RRing6		pulsed to a lower voltage than its corresponding RTIP_n input pin.
AD13	RRing7		Conversely, whenever the RTIP/RRING input pins are receiving a negative-
C9	RRing8		polarity pulse within the incoming DS3, E3 or STS-1 line signal, then this input
AD9	RRing9		pin will be pulsed to a higher voltage than its corresponding RTIP_n input pin.
C5	RRing10		
AD5	RRing11		

REV. 1.0.4

CLOCK INTERFACE

Pin#	SIGNAL NAME	Түре	DESCRIPTION
R5	SFM_EN	I	Single Frequency Mode Enable This input pin is used to configure the XRT75R12 to operate in the SFM (Single Frequency Mode). When this feature is invoked, the SFM Synthesizer will become active. By applying a 12.288MHz clock signal to the STS-1Clk/12M pin, the XRT75R12 will generate all of the appropriate clock signals (e.g., 34.368MHz, 44.736MHz or 51.84). The XRT75R12 internal circuitry will route each of these synthesized clock signals to the appropriate nodes of the corresponding channels in the XRT75R12. "Low" - Disables the Single Frequency Mode. In this setting, the user is required to supply to the E3CLK, DS3CLK or STS-1CLK input pins all of the relevant clock signals that are to be used within the chip. "High" - Enables the Single-Frequency Mode. Note: This input pin is internally pulled low.
R1	E3Clk	I	E3 Clock Input (34.368 MHz ± 20 ppm) If any one of the channels is configured in E3 mode, a reference clock of 34.368 MHz ± 20 ppm is applied to this input pin. If the LIU is used in E3 mode only, this pin must be connected to the DS3Clk input pin to have access to the internal microprocessor. Note: SFM mode negates the need for this clock
T1	DS3Clk	I	DS3 Clock Input (44.736 MHz ± 20 ppm) If any one of the channels is configured in DS3 mode, a reference clock of 44.736 MHz ± 20 ppm is applied to this input pin. Note: SFM mode negates the need for this clock
U1	STS-1Clk/12M	I	STS-1 Clock Input (51.84 MHz ± 20 ppm) If any one of the channels is configured in STS-1 mode, a reference clock of 51.84MHz ± 20 ppm is applied to this input pin. If the LIU is used in STS-1 mode only, this pin must be connected to the DS3Clk input pin to have access to the internal microprocessor. Single Frequency Mode Clock Input (12.288MHz ± 20 ppm) In Single Frequency Mode, a reference clock of 12.288 MHz ± 20 ppm is connected to this pin and the internal clock synthesizer generates the appropriate clock frequencies based on the configuration of the rates (E3, DS3 or STS-1).
C26 W22 K23 W24 J25 V25 J2 V2 K4 W3 C1	CLKOUT0 CLKOUT1 CLKOUT2 CLKOUT3 CLKOUT4 CLKOUT5 CLKOUT6 CLKOUT7 CLKOUT8 CLKOUT9 CLKOUT10 CLKOUT11	0	Reference Clock Out A reference clock pin is provided for each channel that will supply a precise data rate frequency derived from either the Clock input pin (E3Clk, DS3Clk, or STS-1Clk) or the 12.288MHz input in SFM mode. This frequency will be as stable as the original source. It is designed to provide the attached framer with its appropriate reference clock.



GENERAL CONTROL PINS

PIN#	SIGNAL NAME	Түре	DESCRIPTION
P3	TEST	***	Factory Test Mode Input Pin This pin must be connected to GND for normal operation. Note: This input pin is internally pulled "Low".
AE25	TRST	I	Test Reset Test Boundary Scan
AB23	TMS	I	Test Mode Select Test Boundary Scan
AB5	TCK	I	Test Clock Test Boundary Scan
AB4	TDI	I	Test Data Input Test Boundary Scan
AE2	TDO	0	Test Data Output Test Boundary Scan

MICROPROCESSOR PARALLEL INTERFACE -

Pin#	SIGNAL NAME	Түре	DESCRIPTION
J26	Pmode	I	This pin controls the Microprocessor Parallel Interface mode.
			"High" sets a Synchronous clocked interface mode with a clock from the Host.
			"Low" sets an Asynchronous mode where a clock internal to the XRT75R12 will time the operations.
P24	PCLK	I	High speed clock supplied by the Host to provide timing in the Synchronous Interface mode. This signal must be a square-wave.
N24	CS	I	Chip Select Input (active low)
			Initiates a read or write operation. When "High", no parallel communication is active between the LIU and the Host.
N22	WR	I	Write Input (active low)
			Enables the Host to write data D[7:0] into the LIU register space at address Addr[7:0].
N23	RD	1	Read Input (active low)
			Commands the LIU to transfer the contents of a register specified by Addr[7:0] to the Host.
N25	RDY	0	Ready Line Output (active low)
			Provides a handshake between the LIU and the Host that communicates when an operation has been completed.
			Note: This pin must be pulled "High" with a $3k\Omega \pm 1\%$ resistor.

XRT75R12



TWELVE CHANNEL E3/DS3/STS-1 LINE INTERFACE UNIT WITH JITTER ATTENUATOR

REV. 1.0.4

MICROPROCESSOR PARALLEL INTERFACE -

Pin#	SIGNAL NAME	Түре	DESCRIPTION
K25 M22 M23 M24 K26 L26 M26	Addr0 Addr1 Addr2 Addr3 Addr4 Addr5 Addr6 Addr7	I	An eight bit direct address bus that specifies the source/destination register for a Read or Write operation.
P22 R26 T26 U26 R25 R24 R23 R22	D0 D1 D2 D3 D4 D5 D6 D7	I/O	An eight bit bi-directional data bus that provides the data into the LIU for a Write operation or the data out to the Host for a Read operation.
P26	ĪNT	0	Interrupt Active Output (active low) Normally, this output pin will be pulled "High". However, if the user enables interrupts within the LIU, and if those conditions occur, the XRT75R12 will signal an interrupt from the Microprocessor by pulling this output pin "Low". The Host Microprocessor must ascertain the source of the interrupt and service it. Reading the source of the interrupt will clear the flag and the INT pin will go back high unless another interrupt has gone active. **Notes:* 1. This pin will remain "Low" until the Interrupt has been serviced. 2. This pin must be pulled "High" with a 3kΩ ± 1% resistor.
N2	RESET	I	RESET Input Pulsing this input "Low" causes the XRT75R12 to reset the contents of the on- chip Command Registers to their default values. As a consequence, the XRT75R12 will then also be operating in its default condition. For normal operation this input pin should be at a logic "High". Note: This input pin is internally pulled high.



POWER SUPPLY PINS

PIN NAME	PIN NUMBERS	DESCRIPTION
RVDD0	D22	Receive Analog Power Supply (3.3V ±5%)
RVDD1	AC22	RVDD should not be shared with other power supplies. It is recommended
RVDD2	D18	that RVDD be isolated from the digital power supply DVDD and the analog
RVDD3	AC18	power supply TVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used.
RVDD4	E15	Each power supply pin should be bypassed to ground through an external
RVDD5	AB15	0.1μF capacitor.
RVDD6	E12	
RVDD7	AB12	
RVDD8	A9	
RVDD9	AF9	
RVDD10 RVDD11	D5	
RVUUTI	AC5	
TVDD0	B23	Transmit Analog Power Supply (3.3V ±5%)
TVDD1	AE23	TVDD can be shared with DVDD. However, it is recommended that TVDD be
TVDD2	B19	isolated from the analog power supply RVDD. For best results, use an internal power plane for isolation. If an internal power plane is not available, a fer-
TVDD3	AE19	rite bead can be used. Each power supply pin should be bypassed to ground
TVDD4	B15	through an external 0.1μF capacitor.
TVDD5 TVDD6	AE15	
TVDD6	B10	
TVDD7	AE10	
TVDD0	A6	
TVDD10	AF6	
TVDD11	B4	
	AE4	
AVDD	M25, T25, AB21, AB18,	Analog Power Supply (3.3V ±5%)
	AF13, AF12, AB9, AB6, R4, K1, E6, E9, A12, A13, E18, E21,	AVDD should be isolated from the digital power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Each power supply pin should be bypassed to ground through at least one $0.1\mu F$ capacitor.
DVDD	D26, F25, H25, P25, W26, V24, Y22, AF21, AF20, AF17, AF16, AD14, AD12, AF11, AF8, AF7, AF24, AD6, AF3, Y5, V3, W1, P5, P2, H2, F2, D1, C6, A7, A3, A8, A11, C12, C14, A16, A17, A20, A21, A24	Digital Power Supply (3.3V ±5%) DVDD should be isolated from the analog power supplies. For best results, use an internal power plane for isolation. If an internal power plane is not available, a ferrite bead can be used. Every two DVDD power supply pins should be bypassed to ground through at least one 0.1μF capacitor.

REV. 1.0.4

TWELVE CHANNEL E3/DS3/STS-1 LINE INTERFACE UNIT WITH JITTER ATTENUATOR

GROUND PINS

PIN NAME	PIN NUMBERS	DESCRIPTION
RGND0	A22	Receive Analog Ground
RGND1	AF22	It's recommended that all ground pins of this device be tied together.
RGND2	A18	
RGND3	AF18	
RGND4	E14	
RGND5	AB14	
RGND6	E13	
RGND7	AB13	
RGND8	D9	
RGND9		
RGND10	AC9	
RGND11	A5	
	AF5	
TGND0	A23	Transmit Analog Ground
TGND1	AF23	It's recommended that all ground pins of this device be tied together.
TGND2	A19	
TGND3	AF19	
TGND4	A15	
TGND5	AF15	
TGND6	A10	
TGND7	AF10	
TGND8	B6	
TGND9		
TGND10	AE6	
TGND11	A4	
	AF4	
AGND	A1, A2, A25, A26, B1, B2, B25, B26, C8, C10, C17, C19, C21, D17, D21, E5, E22, L25, U25, AB22, AB20, AB17, AB10, AB7, R3, L1, E7, E10, B12, B13, E17, E20, T2, U2, AC17, AC21, AD8, AD10, AD15, AD17, AD19, AD21, AE1, AE26, AE12, AE13, AF1, AF2, AF25, AF26, C15	Analog Ground It's recommended that all ground pins of this device be tied together.
DGND	E26, F26, H26, P23, , V26, Y25, V22, AC24, AC20, AC16, AC14, AC12, AC11, AE8, AE17, AE21, AC7, AC6, AC3, V5, Y2, V1, R2, P1, H1, F1, E1, D3, D7, B8, D6, D11, D12, D14, D16, B17, D20, B21, D24	Digital Ground It's recommended that all ground pins of this device be tied together.

TABLE 1: PIN LIST BY PIN NUMBER

NUMBER		
Pin	PIN NAME	
A1	AGND	
A2	AGND	
А3	DVDD	
A4	TGND10	
A5	RGND10	
A6	TVDD8	
A7	DVDD	
A8	DVDD	
A9	RVDD8	
A10	TGND6	
A11	DVDD	
A12	AVDD	
A13	AVDD	
A14	RTip4	
A15	TGND4	
A16	DVDD	
A17	DVDD	
A18	RGND2	
A19	TGND2	
A20	DVDD	
A21	DVDD	
A22	RGND0	
A23	TGND0	
A24	DVDD	
A25	AGND	
A26	AGND	
B1	AGND	
B2	AGND	
В3	TRing10	
B4	TVDD10	
B5	RTip10	
B6	TGND8	

HANNE	L E3/DS3/STS-1
Pin	PIN NAME
В7	TRing8
B8	DGND
В9	RTip8
B10	TVDD6
B11	TRing6
B12	AGND
B13	AGND
B14	RRing4
B15	TVDD4
B16	TRing4
B17	DGND
B18	RTip2
B19	TVDD2
B20	TRing2
B21	DGND
B22	RTip0
B23	TVDD0
B24	TTip0
B25	AGND
B26	AGND
C1	CLKOUT10
C2	TxNEG10
С3	TTip10
C4	MTip10
C5	RRing10
C6	DVDD
C7	TTip8
C8	AGND
C9	RRing8
C10	AGND
C11	TTip6
C12	DVDD
C13	RRing6
C14	DVDD

PIN	PIN NAME
C15	AGND
C16	TTip4
C17	AGND
C18	RRing2
C19	AGND
C20	TTip2
C21	AGND
C22	RRing0
C23	MTip0
C24	TRing0
C25	TxNEG0
C26	CLKOUT0
D1	DVDD
D2	RLOS10
D3	DGND
D4	MRing10
D5	RVDD10
D6	DGND
D7	DGND
D8	MRing8
D9	RGND8
D10	MRing6
D11	DGND
D12	DGND
D13	RTip6
D14	DGND
D15	MTip4
D16	DGND
D17	AGND
D18	RVDD2
D19	MTip2
D20	DGND
D21	AGND
D22	RVDD0

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Pin	PIN NAME	
D23	MRing0	
D24	DGND	
D25	RLOS0	
D26	DVDD	
E1	DGND	
E2	RxPOS10	
E3	RxCLK10	
E4	TxPOS10	
E5	AGND	
E6	AVDD	
E7	AGND	
E8	MTip8	
E9	AVDD	
E10	AGND	
E11	MTip6	
E12	RVDD6	
E13	RGND6	
E14	RGND4	
E15	RVDD4	
E16	MRing4	
E17	AGND	
E18	AVDD	
E19	MRing2	
E20	AGND	
E21	AVDD	
E22	AGND	
E23	TxPOS0	
E24	RxCLK0	
E25	RxPOS0	
E26	DGND	
F1	DGND	
F2	DVDD	
F3	RxNEG/LCV8	
F4	RxNEG/LCV10	

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TWELVE CHANNEL E3/DS3/STS-1 LINE INTERFACE UNIT WITH JITTER ATTENUATOR

REV. 1.0.4

Pin	PIN NAME
F5	TxCLK10
F22	TxCLK0
F23	RxNEG/LCV0
F24	RxNEG/LCV2
F25	DVDD
F26	DGND
G1	TxCLK6
G2	TxPOS6
G3	RxPOS8
G4	RLOS8
G5	RLOL10
G22	RLOL0
G23	RLOS2
G24	RxPOS2
G25	TxPOS4
G26	TxCLK4
H1	DGND
H2	DVDD
Н3	TxNEG6
H4	TxNEG8
H5	TxCLK8
H22	TxCLK2
H23	TxNEG2
H24	TxNEG4
H25	DVDD
H26	DGND
J1	DMO11
J2	CLKOUT6
J3	RLOS6
J4	RxCLK8
J5	TxPOS8
J22	TxPOS2
J23	RxCLK2
J24	RLOS4

Pin	PIN NAME
J25	CLKOUT4
J26	Pmode
K1	AVDD
K2	DMO10
K3	RxCLK6
K4	CLKOUT8
K5	RLOL8
K22	RLOL2
K23	CLKOUT2
K24	RxCLK4
K25	Addr0
K26	Addr4
L1	AGND
L2	DMO5
L3	RLOL6
L4	RxNEG/LCV6
L5	RxPOS6
L22	RxPOS4
L23	RxNEG/LCV4
L24	RLOL4
L25	AGND
L26	Addr5
M1	DMO4
M2	DMO6
M3	DMO7
M4	DMO8
M5	DMO9
M22	Addr1
M23	Addr2
M24	Addr3
M25	AVDD
M26	Addr6
N1	DMO3
N2	RESET

Pin	PIN NAME
N3	DMO0
N4	DMO1
N5	DMO2
N22	WR
N23	RD
N24	CS
N25	RDY
N26	Addr7
P1	DGND
P2	DVDD
P3	TEST
P4	TxON
P5	DVDD
P22	D0
P23	DGND
P24	PCLK
P25	DVDD
P26	ĪNT
R1	E3Clk
R2	DGND
R3	AGND
R4	AVDD
R5	SFM_EN
R22	D7
R23	D6
R24	D5
R25	D4
R26	D1
T1	DS3Clk
T2	AGND
T3	RxNEG/LCV7
T4	RxCLK7
T5	RxPOS7
T22	RxPOS5

PIN	PIN NAME
T23	RxCLK5
T24	RxNEG/LCV5
T25	AVDD
T26	D2
U1	STS-1Clk/12M
U2	AGND
U3	RLOS7
U4	RxNEG/LCV9
U5	RLOL9
U22	RLOL3
U23	RxNEG/LCV3
U24	RLOS5
U25	AGND
U26	D3
V1	DGND
V2	CLKOUT7
V3	DVDD
V4	RxCLK9
V5	DGND
V22	DGND
V23	RxCLK3
V24	DVDD
V25	CLKOUT5
V26	DGND
W1	DVDD
W2	RLOL7
W3	CLKOUT9
W4	TxNEG9
W5	CLKOUT11
W22	CLKOUT1
W23	TxNEG3
W24	CLKOUT3
W25	RLOL5
W26	DVDD

KEV. 1.0.4	
PIN	PIN NAME
Y1	TxNEG7
Y2	DGND
Y3	RxPOS9
Y4	TxCLK9
Y5	DVDD
Y22	DVDD
Y23	TxCLK3
Y24	RxPOS3
Y25	DGND
Y26	TxNEG5
AA1	TxPOS7
AA2	TxCLK7
AA3	RLOS9
AA4	TxPOS9
AA5	TxCLK11
AA22	TxCLK1
AA23	TxPOS3
AA24	RLOS3
AA25	TxCLK5
AA26	TxPOS5
AB1	RLOL11
AB2	TxNEG11
AB3	TxPOS11
AB4	TDI
AB5	TCK
AB6	AVDD
AB7	AGND
AB8	MTip9
AB9	AVDD
AB10	AGND
AB11	MTip7
AB12	RVDD7
AB13	RGND7
AB14	RGND5

Pin	PIN NAME	
AB15	RVDD5	
AB16	MRing5	
AB17	AGND	
AB18	AVDD	
AB19	MRing3	
AB20	AGND	
AB21	AVDD	
AB22	AGND	
AB23	TMS	
AB24	TxPOS1	
AB25	TxNEG1	
AB26	RLOL1	
AC1	RxNEG/LCV11	
AC2	RxCLK11	
AC3	DGND	
AC4	MRing11	
AC5	RVDD11	
AC6	DGND	
AC7	DGND	
AC8	MRing9	
AC9	RGND9	
AC10	MRing7	
AC11	DGND	
AC12	DGND	
AC13	RTip7	
AC14	DGND	
AC15	MTip5	
AC16	DGND	
AC17	AGND	
AC18	RVDD3	
AC19	MTip3	
AC20	DGND	
AC21	AGND	
AC22	RVDD1	

Pin	PIN NAME
AC23	MRing1
AC24	DGND
AC25	RxCLK1
AC26	RxNEG/LCV1
AD1	RxPOS11
AD2	RLOS11
AD3	TTip11
AD4	MTip11
AD5	RRing11
AD6	DVDD
AD7	TTip9
AD8	AGND
AD9	RRing9
AD10	AGND
AD11	TTip7
AD12	DVDD
AD13	RRing7
AD14	DVDD
AD15	AGND
AD16	TTip5
AD17	AGND
AD18	RRing3
AD19	AGND
AD20	TTip3
AD21	AGND
AD22	RRing1
AD23	MTip1
AD24	TRing1
AD25	RLOS1
AD26	RxPOS1
AE1	AGND
AE2	TDO
AE3	TRing11
AE4	TVDD11

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Pin	PIN NAME		
AE5	RTip11		
AE6	TGND9		
AE7	TRing9		
AE8	DGND		
AE9	RTip9		
AE10	TVDD7		
AE11	TRing7		
AE12	AGND		
AE13	AGND		
AE14	RRing5		
AE15	TVDD5		
AE16	TRing5		
AE17	DGND		
AE18	RTip3		
AE19	TVDD3		
AE20	TRing3		
AE21	DGND		
AE22	RTip1		
AE23	TVDD1		
AE24	TTip1		
AE25	TRST		
AE26	AGND		
AF1	AGND		
AF2	AGND		
AF3	DVDD		
AF4	TGND11		
AF5	RGND11		
AF6	TVDD9		
AF7	DVDD		
AF8	DVDD		
AF9	RVDD9		
AF10	TGND7		
AF11	DVDD		
AF12	AVDD		

XRT75R12



REV. 1.0.4

TWELVE CHANNEL E3/DS3/STS-1 LINE INTERFACE UNIT WITH JITTER ATTENUATOR

Pin	PIN NAME
AF13	AVDD
AF14	RTip5
AF15	TGND5
AF16	DVDD
AF17	DVDD
AF18	RGND3
AF19	TGND3
AF20	DVDD
AF21	DVDD
AF22	RGND1
AF23	TGND1
AF24	DVDD
AF25	AGND
AF26	AGND

FUNCTIONAL DESCRIPTION

The XRT75R12 is a twelve channel fully integrated Line Interface Unit featuring EXAR's R³ Technology (Reconfigurable, Relayless Redundancy) for E3/DS3/STS-1 applications. The LIU incorporates 12 independent Receivers. Transmitters and Jitter Attenuators in a single 420 Lead TBGA package. Each channel can be independently programmed to support E3, DS-3 or STS-1 line rates using one input clock reference of 12.288MHz in Single Frequency Mode (SFM). The LIU is responsible for providing the physical connection between a line interface and an aggregate mapper or framing device. Along with the analog-todigital processing, the LIU offers monitoring and diagnostic features to help optimize network design implementation. A key characteristic within the network topology is Automatic Protection Switching (APS). EXAR's proven expertise in providing redundany solutions has paved the way for R³ Technology.

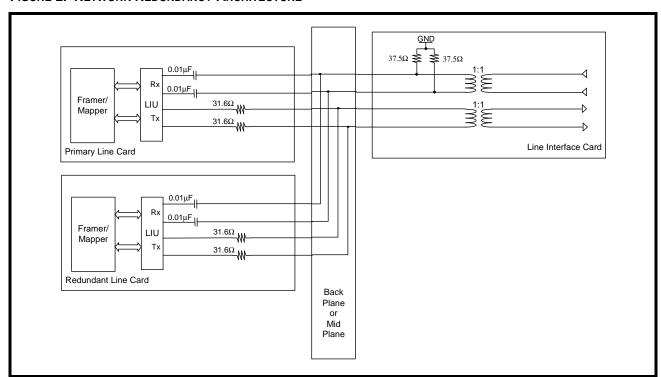
1.0 R³ TECHNOLOGY (RECONFIGURABLE, RELAYLESS REDUNDANCY)

Redundancy is used to introduce reliability and protection into network card design. The redundant card in many cases is an exact replicate of the primary card, such that when a failure occurs the network processor can automatically switch to the backup card. EXAR's R³ technology has re-defined E3/DS-3/STS-1 LIU design for 1:1 and 1+1 redundancy applications. Without relays and one Bill of Materials, EXAR offers multi-port, integrated LIU solutions to assist high density aggregate applications and framing requirements with reliability. The following section can be used as a reference for implementing R³ Technology with EXAR's world leading line interface units.

1.1 **Network Architecture**

A common network design that supports 1:1 or 1+1 redundancy consists of N primary cards along with N backup cards that connect into a mid-plane or back-plane architecture without transformers installed on the network cards. In addition to the network cards, the design has a line interface card with one source of transformers, connectors, and protection components that are common to both network cards. With this design, the bill of materials is reduced to the fewest amount of components. See Figure 2, for a simplified block diagram of a typical redundancy design.

FIGURE 2. NETWORK REDUNDANCY ARCHITECTURE



REV. 1.0.4

2.0 CLOCK SYNTHESIZER

The LIU uses a flexible user interface for accepting clock references to generate the internal master clocks used to drive the LIU. The reference clock used to supply the microprocessor timing is generated from the DS-3 or SFM clock input. Therefore, if the chip is configured for STS-1 only or E3 only, then the DS-3 input pin must be connected to the STS-1 pin or E3 pin respectively. In DS-3 mode or when SFM is used, the STS-1 and E3 input pins can be left unconnected. If SFM is enabled by pulling the SFM_EN pin "High", 12.288MHz is the only clock reference necessary to generate DS-3, E3, or STS-1 line rates and the microprocessor timing. A simplified block diagram of the clock synthesizer is shown in Figure 3. Reference clock performance specifications can be found on Table 2 below.

FIGURE 3. SIMPLIFIED BLOCK DIAGRAM OF THE INPUT CLOCK CIRCUITRY DRIVING THE MICROPROCESSOR

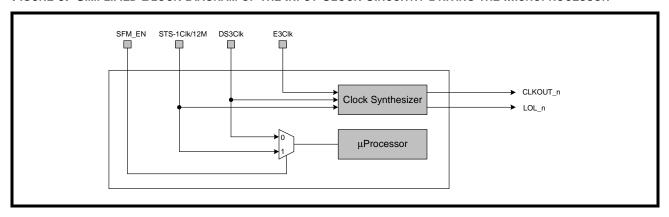


TABLE 2: REFERENCE CLOCK PERFORMANCE SPECIFICATIONS

SYMBOL	PARAMETER	MIN	Түр	MAX	Units
REF _{DUTY}	Reference Clock Duty Cycle	40		60	%
REF _{E3}	E3 Reference Clock Frequency Tolerance ¹	-20		+20	ppm
REF _{DS3}	DS3 Reference Clock Frequency Tolerance ¹	-20		+20	ppm
REF _{STS1}	STS-1 Reference Clock Frequency Tolerance ¹	-20		+20	ppm
REF _{SFM}	SFM Reference Clock Frequency Tolerance ¹	-20		+20	ppm
t _{RISE_REFCLK}	Reference Clock Rise Time (10% to 90%)			5	ns
t _{FALL_REFCLK}	Reference Clock Fall Time (90% to 10%)			5	ns
CLK _{JIT}	Reference Clock Jitter Stability ²			0.005	UI _{p2p}

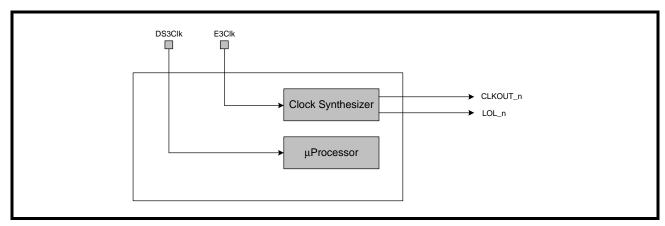
Notes:

- 1. Required to meet Bellcore GR-499 specification on frequency stability requirements. However, the LIU can functionally operate with ±100 ppm without meeting the required specifications.
- 2. Reference clock jitter limits are required for the transmit output to meet ITU-T and Bellcore system level jitter requirements.

2.1 Clock Distribution

Network cards that are designed to support multiple line rates which are not configured for single frequency mode should ensure that a clock is applied to the DS3Clk input pin. For example: If the network card being supplied to an ISP requires E3 only, the DS-3 input clock reference is still necessary to provide read and write access to the internal microprocessor. Therefore, the E3 mode requires two input clock references. If however, multiple line rates will not be supported, i.e. E3 only, then the DS3Clk input pin may be hard wire connected to the E3Clk input pin.

FIGURE 4. CLOCK DISTRIBUTION CONGIFURED IN E3 MODE WITHOUT USING SFM



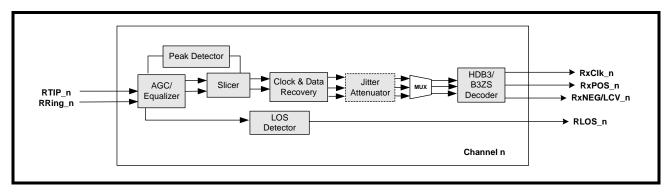
Note: For one input clock reference, the single frequency mode should be used.

REV. 1.0.4

3.0 THE RECEIVER SECTION

The receiver is designed so that the LIU can recover clock and data from an attenuated line signal caused by cable loss or flat loss according to industry specifications. Once data is recovered, it is processed and presented at the receiver outputs according to the format chosen to interface with a Framer/Mapper or ASIC. This section describes the detailed operation of various blocks within the receive path. A simplified block diagram of the receive path is shown in Figure 5.

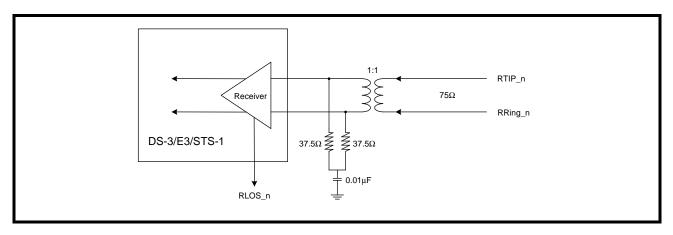
FIGURE 5. RECEIVE PATH BLOCK DIAGRAM



3.1 Receive Line Interface

Physical Layer devices are AC coupled to a line interface through a 1:1 transformer. The transformer provides isolation and a level shift by blocking the DC offset of the incoming data stream. The typical medium for the line interface is a 75Ω coxial cable. Whether using E3, DS-3 or STS-1, the LIU requires the same bill of materials, see Figure 6.

FIGURE 6. RECEIVE LINE INTERFACE CONNECTION



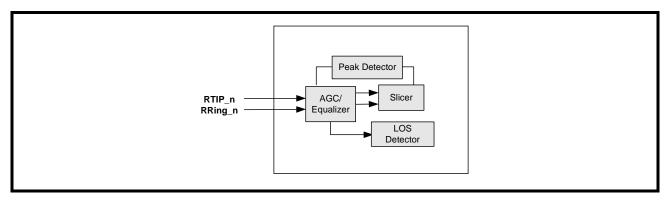
3.2 Adaptive Gain Control (AGC)

The Adaptive Gain Control circuit amplifies the incoming analog signal and compensates for the various flat losses and also for the loss at one-half symbol rate. The AGC has a dynamic range of 30 dB. The peak detector provides feedback to the equalizer before slicing occurs.

3.3 Receive Equalizer

The Equalizer restores the integrity of the signal and compensates for the frequency dependent attenuation of up to 900 feet of coaxial cable (1300 feet for E3). The Equalizer also boosts the high frequency content of the signal to reduce Inter-Symbol Interference (ISI) so that the slicer slices the signal at 50% of peak voltage to generate Positive and Negative data. The equalizer can be disabled by programming the appropriate register.

FIGURE 7. ACG/EQUALIZER BLOCK DIAGRAM



3.3.1 Recommendations for Equalizer Settings

The Equalizer has two gain settings to provide optimum equalization. In the case of normally shaped DS3/STS-1 pulses (pulses that meet the template requirements) that has been driven through 0 to 900 feet of cable, the Equalizer can be enabled. However, for square-shaped pulses such as E3 or for DS3/STS-1 high pulses (that does not meet the pulse template requirements), it is recommended that the Equalizer be disabled for cable length less than 300 feet. This would help to prevent over-equalization of the signal and thus optimize the performance in terms of better jitter transfer characteristics. The Equalizer also contains an additional 20 dB gain stage to provide the line monitoring capability (Receive Monitor Mode) of the resistively attenuated signals which may have 20dB flat loss. The equalizer and the equalizer gain mode can be enabled by programming the appropriate register. However, enabling the equalizer gain mode (Receive Monitor Mode) suppresses the internal LOS circuitry and LOS will never assert nor LOS be declared when operating with Receive Monitor Mode enabled.

Note: The results of extensive testing indicate that even when the Equalizer was enabled, regardless of the cable length, the integrity of the E3 signal was restored properly over 0 to 12 dB cable loss at Industrial Temperature.

3.4 Clock and Data Recovery

The Clock and Data Recovery Circuit extracts the embedded clock, RxClk_n from the sliced digital data stream and provides the retimed data to the B3ZS (HDB3) decoder. The Clock Recovery PLL can be in one of the following two modes:

3.4.1 Data/Clock Recovery Mode

In the presence of input line signals on the RTIP_n and RRing_n input pins and when the frequency difference between the recovered clock signal and the reference clock signal is less than 0.5%, the clock that is output on the RxClk_n out pins is the Recovered Clock signal.

3.4.2 Training Mode

In the absence of input signals at RTIP_n and RRing_n pins, or when the frequency difference between the recovered line clock signal and the reference clock applied on the ExClk_n input pins exceed 0.5%, a Loss of Lock condition is declared by toggling RLOL_n output pin "High" or setting the RLOL_n bit to "1" in the control register. Also, the clock output on the RxClk n pins are the same as the reference channel clock.

3.5 LOS (Loss of Signal) Detector

3.5.1 DS3/STS-1 LOS Condition

A Digital Loss of SIgnal (DLOS) condition occurs when a string of 175 ± 75 consecutive zeros occur on the line. When the DLOS condition occurs, the DLOS_n bit is set to "1" in the status control register. DLOS condition is cleared when the detected average pulse density is greater than 33% for 175 ± 75 pulses. Analog Loss of Signal (ALOS) condition occurs when the amplitude of the incoming line signal is below the threshold as shown in the Table 3. The status of the ALOS condition is reflected in the ALOS_n status control register. RLOS is the logical OR of the DLOS and ALOS states. When the RLOS condition occurs the RLOS_n output pin is toggled "High" and the RLOS_n bit is set to "1" in the status control register.

TABLE 3: THE ALOS (ANALOG LOS) DECLARATION AND CLEARANCE THRESHOLDS FOR A GIVEN SETTING OF REQEN (DS3 and STS-1 Applications)

APPLICATION	REQEN SETTING	SIGNAL LEVEL TO DECLARE ALOS DEFECT	SIGNAL LEVEL TO CLEAR ALOS DEFECT
DS3	0	< 41mVpk	> 102mVpk
	1	< 52mVpk	> 117mVpk
STS-1	0	< 51mVpk	> 114mVpk
	1	< 58mVpk	> 133mVpk

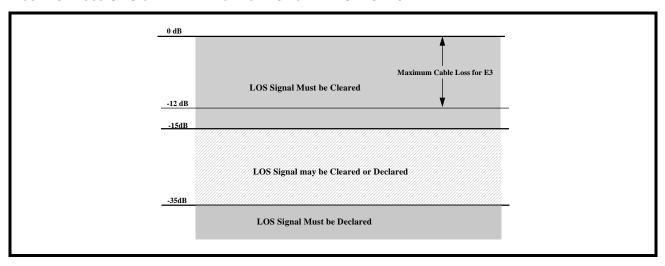
3.5.2 Disabling ALOS/DLOS Detection

For debugging purposes it is useful to disable the ALOS and/or DLOS detection. Writing a "1" to both ALOSDIS_n and DLOSDIS_n bits disables the LOS detection on a per channel basis.

3.5.3 E3 LOS Condition:

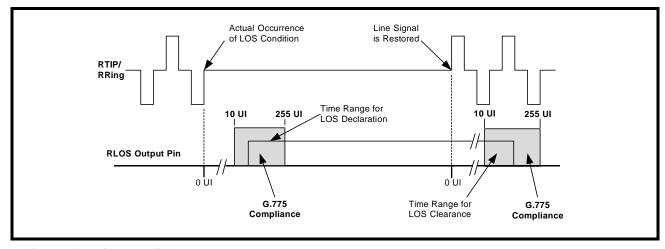
If the level of incoming line signal drops below the threshold as described in the ITU-T G.775 standard, the LOS condition is detected. Loss of signal is defined as no transitions for 10 to 255 consecutive zeros. No transitions is defined as a signal level between 15 and 35 dB below the normal. This is illustrated in Figure 8. The LOS condition is cleared within 10 to 255 UI after restoration of the incoming line signal. Figure 9 shows the LOS declaration and clearance conditions.

FIGURE 8. LOSS OF SIGNAL DEFINITION FOR E3 AS PER ITU-T G.775



REV. 1.0.4

FIGURE 9. LOSS OF SIGNAL DEFINITION FOR E3 AS PER ITU-T G.775.



3.5.4 Interference Tolerance

For E3 mode, ITU-T G.703 Recommendation specifies that the receiver be able to recover error free clock and data in the presence of a sinusoidal interfering tone signal. For DS3 and STS-1 modes, the same recommendation is being used. Figure 10 shows the configuration to test the interference margin for DS3/STS1. Figure 11 shows the set up for E3.

FIGURE 10. INTERFERENCE MARGIN TEST SET UP FOR DS3/STS-1

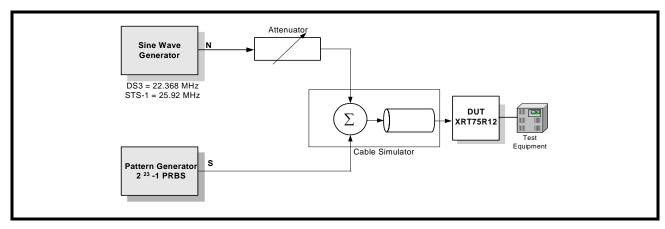


FIGURE 11. INTERFERENCE MARGIN TEST SET UP FOR E3.

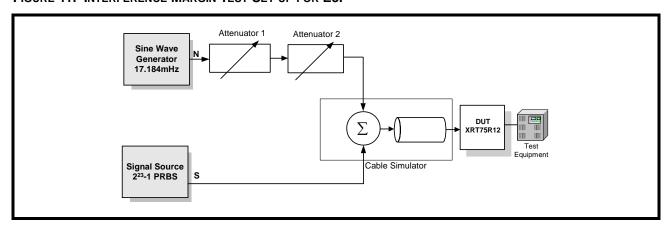




TABLE 4: INTERFERENCE MARGIN TEST RESULTS

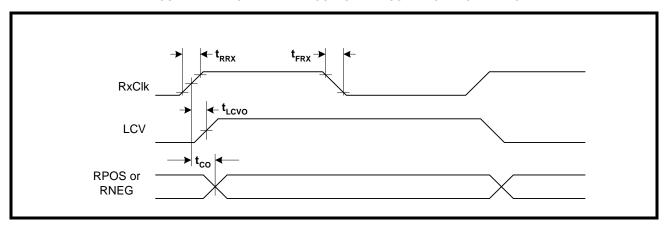
Mode	CABLE LENGTH (ATTENUATION)	INTERFERENCE TOLERANCE
		Equalizer "IN"
E3	0 dB	-17 dB
	12 dB	-14 dB
	0 feet	-15 dB
DS3	225 feet	-15 dB
	450 feet	-14 dB
	0 feet	-15 dB
STS-1	225 feet	-14 dB
	450 feet	-14 dB

3.5.5 Muting the Recovered Data with LOS condition:

When the LOS condition is declared, the clock recovery circuit locks into the reference clock applied to the internal master clock outputs this clock onto the RxClk_n output pin. The data on the RxPOS_n and RxNEG_n pins can be forced to zero by setting the LOSMUT_n bits in the individual channel control register to "1".

Note: When the LOS condition is cleared, the recovered data is output on RxPOS_n and RxNEG_n pins.

FIGURE 12. RECEIVER DATA OUTPUT AND CODE VIOLATION TIMING







REV. 1.0.4

SYMBOL **PARAMETER** MIN TYP MAX UNITS **RxClk Duty Cycle** 45 % 50 55 RxClk Frequency E3 34.368 MHz DS-3 44.736 MHz STS-1 51.84 MHz RxClk rise time (10% o 90%) 2 4 ns t_{RRX} RxClk falling time (10% to 90%) ns t_{FRX} RxClk to RPOS/RNEG delay time 4 t_{CO} ns 2.5 RxClk to rising edge of LCV output delay ns t_{LCVO}

3.6 B3ZS/HDB3 Decoder

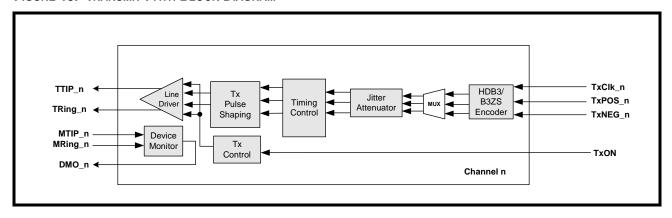
The decoder block takes the output from the clock and data recovery block and decodes the B3ZS (for DS3 or STS-1) or HDB3 (for E3) encoded line signal and detects any coding errors or excessive zeros in the data stream. Whenever the input signal violates the B3ZS or HDB3 coding sequence for bipolar violation or contains three (for B3ZS) or four (for HDB3) or more consecutive zeros, an active "High" pulse is generated on the RLCV_n output pins to indicate line code violation.

REV. 1.0.4

4.0 THE TRANSMITTER SECTION

The transmitter is designed so that the LIU can accept serial data from a local device, encode the data properly, and then output an analog pulse according to the pulse shape chosen in the appropriate registers. This section describes the detailed operation of various blocks within the transmit path. A simplified block diagram of the transmit path is shown in Figure 13.

FIGURE 13. TRANSMIT PATH BLOCK DIAGRAM



4.1 Transmit Digital Input Interface

The method for applying data to the transmit inputs of the LIU is a serial interface consisting of TxClk, TxPOS, and TxNEG. For single rail mode, only TxClk and TxPOS are necessary for providing the local data from a Framer device or ASIC. Data can be sampled on either edge of the input clock signal by programming the appropriate register. A typical interface is shown in Figure 14.

FIGURE 14. TYPICAL INTERFACE BETWEEN TERMINAL EQUIPMENT AND THE XRT75R12 (DUAL-RAIL DATA)

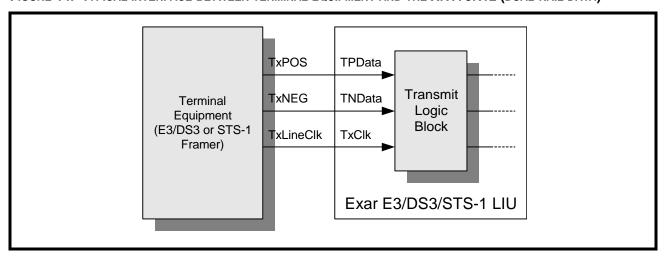
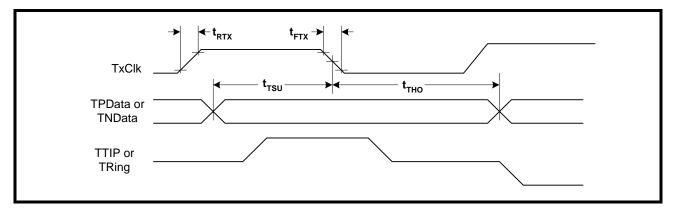


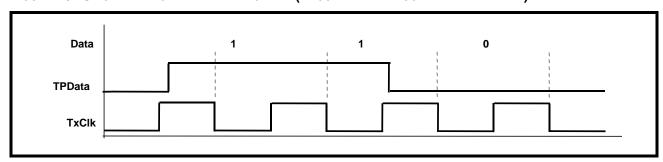


FIGURE 15. TRANSMITTER TERMINAL INPUT TIMING



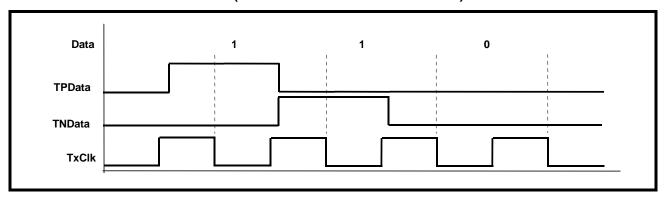
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
TxClk	Duty Cycle	30	50	70	%
	TxClk Frequency				
	E3		34.368		MHz
	DS-3		44.736		MHz
	STS-1		51.84		MHz
t _{RTX}	TxClk Rise Time (10% to 90%)			4	ns
t _{FTX}	TxClk Fall Time (10% to 90%)			4	ns
t _{TSU}	TPData/TNData to TxClk falling set up time	3			ns
t _{THO}	TPData/TNData to TxClk falling hold time	3			ns

FIGURE 16. SINGLE-RAIL OR NRZ DATA FORMAT (ENCODER AND DECODER ARE ENABLED)



REV. 1.0.4

FIGURE 17. DUAL-RAIL DATA FORMAT (ENCODER AND DECODER ARE DISABLED)



4.2 Transmit Clock

The Transmit Clock applied via TxClk_n pins, for the selected data rate (for E3 = 34.368 MHz, DS3 = 44.736 MHz or STS-1 = 51.84 MHz), is duty cycle corrected by the internal PLL circuit to provide a 50% duty cycle clock to the pulse shaping circuit. This allows a 30% to 70% duty cycle Transmit Clock to be supplied.

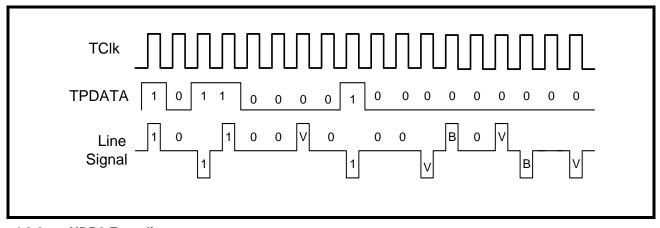
4.3 B3ZS/HDB3 ENCODER

When the Single-Rail (NRZ) data format is selected, the Encoder Block encodes the data into either B3ZS format (for either DS3 or STS-1) or HDB3 format (for E3).

4.3.1 B3ZS Encoding

An example of B3ZS encoding is shown in Figure 18. If the encoder detects an occurrence of three consecutive zeros in the data stream, it is replaced with either B0V or 00V, where 'B' refers to Bipolar pulse that is compliant with the Alternating polarity requirement of the AMI (Alternate Mark Inversion) line code and 'V' refers to a Bipolar Violation (e.g., a bipolar pulse that violates the AMI line code). The substitution of B0V or 00V is made so that an odd number of bipolar pulses exist between any two consecutive violation (V) pulses. This avoids the introduction of a DC component into the line signal.

FIGURE 18. B3ZS ENCODING FORMAT

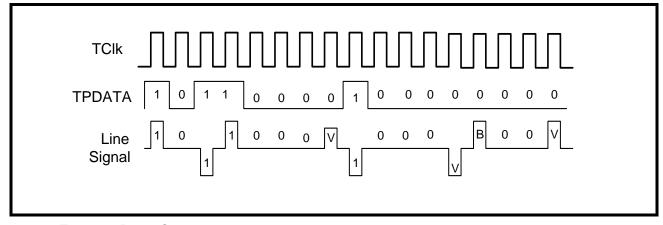


4.3.2 HDB3 Encoding

An example of the HDB3 encoding is shown in Figure 19. If the HDB3 encoder detects an occurrence of four consecutive zeros in the data stream, then the four zeros are substituted with either 000V or B00V pattern. The substitution code is made in such a way that an odd number of pulses exist between any consecutive V pulses. This avoids the introduction of DC component into the analog signal.



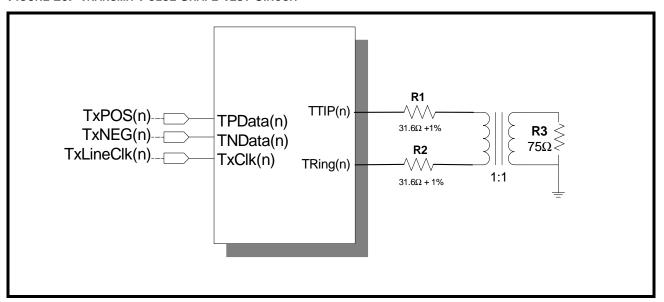
FIGURE 19. HDB3 ENCODING FORMAT



4.4 TRANSMIT PULSE SHAPER

The Transmit Pulse Shaper converts the B3ZS encoded digital pulses into a single analog Alternate Mark Inversion (AMI) pulse that meets the industry standard mask template requirements for STS-1 and DS3. For E3 mode, the pulse shaper converts the HDB3 encoded pulses into a single full amplitude square shaped pulse with very little slope. The Pulse Shaper Block also includes a Transmit Build Out Circuit, which can either be disabled or enabled by setting the TxLEV_n bit to "1" or "0" in the control register. For DS3/STS-1 rates, the Transmit Build Out Circuit is used to shape the transmit waveform that ensures that transmit pulse template requirements are met at the Cross-Connect system. The distance between the transmitter output and the Cross-Connect system can be between 0 to 450 feet. For E3 rate, since the output pulse template is measured at the secondary of the transformer and since there is no Cross-Connect system pulse template requirements, the Transmit Build Out Circuit is always disabled. The differential line driver increases the transmit waveform to appropriate level and drives into the 75 Ω load as shown in Figure 20.

FIGURE 20. TRANSMIT PULSE SHAPE TEST CIRCUIT



4.4.1 Guidelines for using Transmit Build Out Circuit

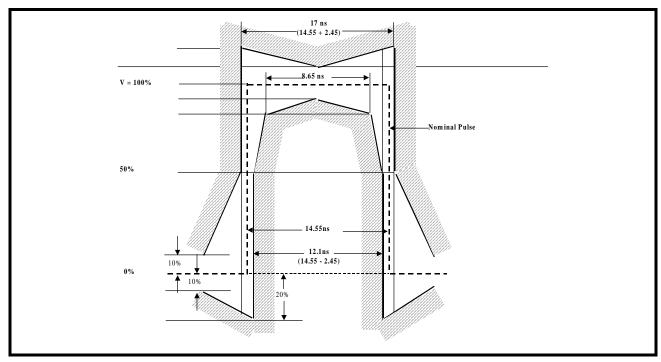
If the distance between the transmitter and the DSX3 or STSX-1, Cross-Connect system, is less than 225 feet, enable the Transmit Build Out Circuit by setting the TxLEV_n control bit to "0". If the distance between the transmitter and the DSX3 or STSX-1 is greater than 225 feet, disable the Transmit Build Out Circuit.

REV. 1.0.4

4.5 E3 line side parameters

The XRT75R12 line output at the transformer output meets the pulse shape specified in ITU-T G.703 for 34.368 Mbits/s operation. The pulse mask as specified in ITU-T G.703 for 34.368 Mbits/s is shown in Figure 21.

FIGURE 21. PULSE MASK FOR E3 (34.368 MBITS/S) INTERFACE AS PER ITU-T G.703



REV. 1.0.4

TABLE 5: E3 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS		
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS						
Transmit Output Pulse Amplitude	0.90	1.00	1.10	V_{pk}		
(Measured at secondary of the transformer)						
Transmit Output Pulse Amplitude Ratio	0.95	1.00	1.05			
Transmit Output Pulse Width	12.5	14.55	16.5	ns		
Transmit Intrinsic Jitter		0.02	0.05	UI _{PP}		
RECEIVER LINE SIDE INPUT CHARACTERISTICS						
Receiver Sensitivity (length of cable)	900	1200		feet		
Interference Margin	-20	-14		dB		
Jitter Tolerance @ Jitter Frequency 800KHz	0.15	0.28		UI _{PP}		
Signal level to Declare Loss of Signal			-35	dB		
Signal Level to Clear Loss of Signal	-15			dB		
Occurence of LOS to LOS Declaration Time	10		255	UI		
Termination of LOS to LOS Clearance Time	10		255	UI		

Note: The above values are at $TA = 25^{\circ}C$ and $V_{DD} = 3.3 \text{ V} \pm 5\%$.



FIGURE 22. BELLCORE GR-253 CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR SONET STS-1 APPLICATIONS

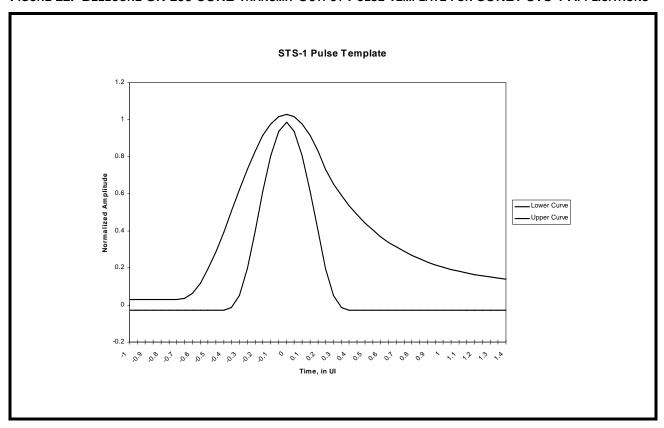


TABLE 6: STS-1 PULSE MASK EQUATIONS

TIME IN UNIT INTERVALS	NORMALIZED AMPLITUDE			
LOWER	CURVE			
-0.85 ≤ T ≤ -0.38	- 0.03			
-0.38 ≤ T ≤ 0.36	$0.5 \left[1 + \sin \left\{ \frac{\pi}{2} \left(1 + \frac{T}{0.18} \right) \right\} \right] - 0.03$			
0.36 ≤ T ≤ 1.4	- 0.03			
UPPER CURVE				
-0.85 ≤ T ≤ -0.68	0.03			
-0.68 ≤ T ≤ 0.26	$0.5 \left[1 + \sin \left\{ \frac{\pi}{2} \left(1 + \frac{T}{0.34} \right) \right\} \right] + 0.03$			
0.26 ≤ T ≤ 1.4	0.1 + 0.61 x e ^{-2.4[T-0.26]}			

TABLE 7: STS-1 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS (GR-253)

PARAMETER	Min	Түр	Max	Units		
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS						
Transmit Output Pulse Amplitude	0.65	0.75	0.90	V_{pk}		
(measured with TxLEV = 0)						
Transmit Output Pulse Amplitude	0.90	1.00	1.10	V_{pk}		
(measured with TxLEV = 1)						
Transmit Output Pulse Width	8.6	9.65	10.6	ns		
Transmit Output Pulse Amplitude Ratio	0.90	1.00	1.10			
Transmit Intrinsic Jitter		0.02	0.05	UI _{pp}		
RECEIVER LINE SIDE INPUT CHARA	ACTERISTICS					
Receiver Sensitivity (length of cable)	900	1100		feet		
Jitter Tolerance @ Jitter Frequency 400 KHz	0.15			Ul _{pp}		
Signal Level to Declare Loss of Signal Refer to Table 3						
Signal Level to Clear Loss of Signal		Refer to Table 3				

NOTE: The above values are at TA = 25° C and $V_{DD} = 3.3 \text{ V} \pm 5\%$.

FIGURE 23. TRANSMIT OUPUT PULSE TEMPLATE FOR DS3 AS PER BELLCORE GR-499

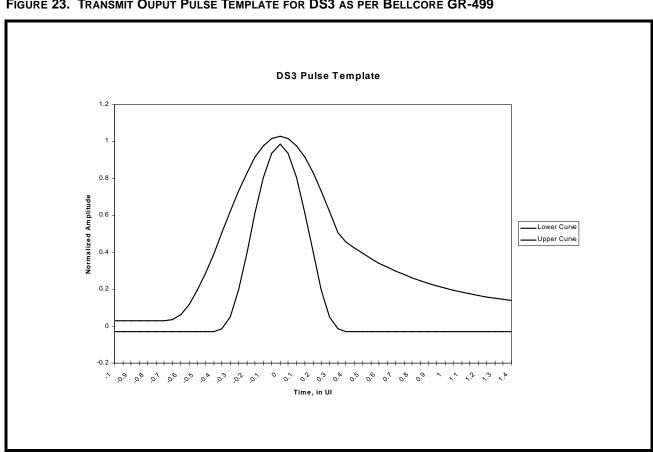


TABLE 8: DS3 PULSE MASK EQUATIONS

TIME IN UNIT INTERVALS	Normalized Amplitude
LOWER	CURVE
-0.85 ≤ T ≤ -0.36	- 0.03
-0.36 ≤ T ≤ 0.36	$0.5 \left[1 + \sin \left\{ \frac{\pi}{2} \left(1 + \frac{T}{0.18} \right) \right\} \right] - 0.03$
0.36 ≤ T ≤ 1.4	- 0.03
UPPER	CURVE
-0.85 ≤ T ≤ -0.68	0.03
-0.68 ≤ T ≤ 0.36	$0.5 \left[1 + \sin \left\{ \frac{\pi}{2} \left(1 + \frac{T}{0.34} \right) \right\} \right] + 0.03$
0.36 ≤ T ≤ 1.4	0.08 + 0.407 x e ^{-1.84[T-0.36]}

TABLE 9: DS3 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS (GR-499)

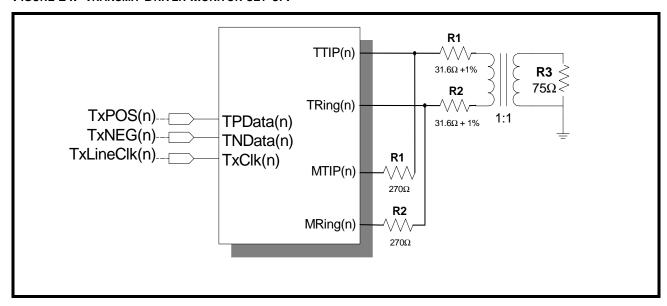
PARAMETER	Min	ТҮР	Max	Units		
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS						
Transmit Output Pulse Amplitude (measured with TxLEV = 0)	0.65	0.75	0.85	V_{pk}		
Transmit Output Pulse Amplitude (measured with TxLEV = 1)	0.90	1.00	1.10	V_{pk}		
Transmit Output Pulse Width	10.10	11.18	12.28	ns		
Transmit Output Pulse Amplitude Ratio	0.90	1.00	1.10			
Transmit Intrinsic Jitter		0.02	0.05	UI _{pp}		
RECEIVER LINE SIDE INPUT CHARACT	TERISTICS					
Receiver Sensitivity (length of cable)	900	1100		feet		
Jitter Tolerance @ 400 KHz (Cat II)	0.15			UI _{pp}		
Signal Level to Declare Loss of Signal Refer to Table 3						
Signal Level to Clear Loss of Signal	Refer to Table 3					

Note: The above values are at TA = 25° C and $V_{DD} = 3.3V \pm 5\%$.

4.6 Transmit Drive Monitor

This feature is used for monitoring the transmit line for occurrence of fault conditions such as a short circuit on the line or a defective line driver. To activate this function, connect MTIP_n pins to the TTIP_n lines via a 270Ω resistor and MRing_n pins to TRing_n lines via 270Ω resistor as shown in Figure 24.

FIGURE 24. TRANSMIT DRIVER MONITOR SET-UP.



When the MTIP_n and MRing_n are connected to the TTIP_n and TRing_n lines, the drive monitor circuit monitors the line for transitions. The DMO_n (Drive Monitor Output) will be asserted "Low" as long as the transitions on the line are detected via MTIP_n and MRing_n. If no transitions on the line are detected for 128 \pm 32 TxClk_n periods, the DMO_n output toggles "High" and when the transitions are detected again, DMO_n toggles "Low".

Note: The Drive Monitor Circuit is only for diagnostic purpose and does not have to be used to operate the transmitter.

4.7 Transmitter Section On/Off

The transmitter section of each channel can either be turned on or off. To turn on the transmitter, set the input pin TxON to "High" and write a "1" to the TxON_n control bit. When the transmitter is turned off, TTIP_n and TRing_n are tri-stated.

Notes:

- 1. This feature provides support for Redundancy.
- 2. If the XRT75R12 is configured in Host mode, to permit a system designed for redundancy to quickly shut-off the defective line card and turn on the back-up line card, writing a "1" to the TxON_n control bits transfers the control to TxON pin.

REV. 1.0.4

5.0 JITTER

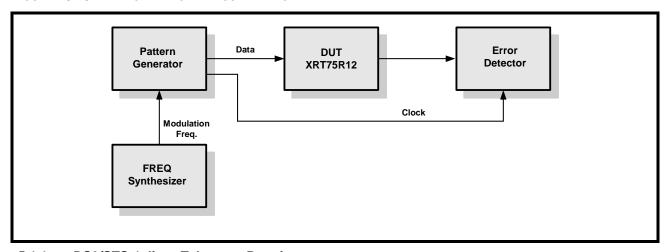
There are three fundamental parameters that describe circuit performance relative to jitter

- Jitter Tolerance
- Jitter Transfer
- Jitter Generation

5.1 JITTER TOLERANCE

Jitter tolerance is a measure of how well a Clock and Data Recovery unit can successfully recover data in the presence of various forms of jitter. It is characterized by the amount of jitter required to produce a specified bit error rate. The tolerance depends on the frequency content of the jitter. Jitter Tolerance is measured as the jitter amplitude over a jitter spectrum for which the clock and data recovery unit achieves a specified bit error rate (BER). To measure the jitter tolerance as shown in Figure 25, jitter is introduced by the sinusoidal modulation of the serial data bit sequence. Input jitter tolerance requirements are specified in terms of compliance with jitter mask which is represented as a combination of points. Each point corresponds to a minimum amplitude of sinusoidal jitter at a given jitter frequency.

FIGURE 25. JITTER TOLERANCE MEASUREMENTS

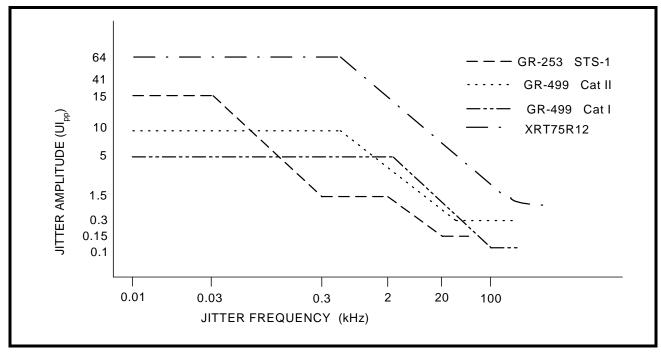


5.1.1 DS3/STS-1 Jitter Tolerance Requirements

Bellcore GR-499 CORE specifies the minimum requirement of jitter tolerance for Category I and Category II. The jitter tolerance requirement for Category II is the most stringent. Figure 26 shows the jitter tolerance curve as per GR-499 specification.



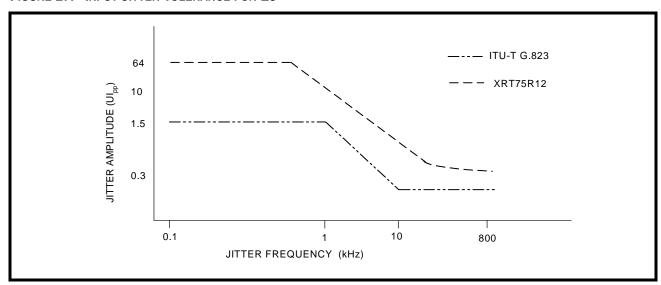
FIGURE 26. INPUT JITTER TOLERANCE FOR DS3/STS-1



5.1.2 E3 Jitter Tolerance Requirements

ITU-T G.823 standard specifies that the clock and data recovery unit must be able to tolerate jitter up to certain specified limits. Figure 27 shows the tolerance curve.

FIGURE 27. INPUT JITTER TOLERANCE FOR E3



As shown in the Figures above, in the jitter tolerance measurement, the dark line indicates the minimum level of jitter that the E3/DS3/STS-1 compliant component must tolerate. Table 10 below shows the jitter amplitude versus the modulation frequency for various standards.

TABLE 10: JITTER AMPLITUDE VERSUS MODULATION FREQUENCY (JITTER TOLERANCE)

BIT RATE	STANDARD		INPUT JITTER AMPLITUDE (UI P-P)			MODULATION FREQUENCY			
(KB/S)	OTANDARD	A1	A2	А3	F1(Hz)	F2(Hz)	F3(KHz)	F4(KHz)	F5(KHZ)
34368	ITU-T G.823	1.5	0.15	-	100	1000	10	800	-
44736	GR-499 CORE Cat I	5	0.1	-	10	2.3k	60	300	ı
44736	GR-499 CORE Cat II	10	0.3	-	10	669	22.3	300	-
51840	GR-253 CORE Cat II	15	1.5	0.15	10	30	300	2	20
	•	•	•	•		•	•	•	

5.2 JITTER TRANSFER

Jitter Transfer function is defined as the ratio of jitter on the output relative to the jitter applied on the input versus frequency. There are two distinct characteristics in jitter transfer, jitter gain (jitter peaking) defined as the highest ratio above 0dB and jitter transfer bandwidth. The overall jitter transfer bandwidth is controlled by a low bandwidth loop, typically using a voltage-controlled crystal oscillator (VCXO).

The jitter transfer function is a ratio between the jitter output and jitter input for a component, or system often expressed in dB. A negative dB jitter transfer indicates the element removed jitter. A positive dB jitter transfer indicates the element added jitter. A zero dB jitter transfer indicates the element had no effect on jitter. Table 11 shows the jitter transfer characteristics and/or jitter attenuation specifications for various data rates:

TABLE 11: JITTER TRANSFER SPECIFICATION/REFERENCES

E3	DS3	STS-1
ETSI TBR-24	GR-499 CORE section 7.3.2 Category I and Category II	GR-253 CORE section 5.6.2.1

Note: The above specifications can be met only with a jitter attenuator that supports E3/DS3/STS-1 rates.

5.3 Jitter Attenuator

An advanced crystal-less jitter attenuator per channel is included in the XRT75R12. The jitter attenuator requires no external crystal nor high-frequency reference clock. By clearing or setting the JATx/Rx_n bits in the channel control registers selects the jitter attenuator either in the Receive or Transmit path on per channel basis. The FIFO size can be either 16-bit or 32-bit. The bits JAO_n and JA1_n can be set to appropriate combination to select the different FIFO sizes or to disable the Jitter Attenuator on a per channel basis. Data is clocked into the FIFO with the associated clock signal (TxClk or RxClk) and clocked out of the FIFO with the dejittered clock. When the FIFO is within two bits of overflowing or underflowing, the FIFO limit status bit, FL n is set to "1" in the Alarm status register. Reading this bit clears the FIFO and resets the bit into default state.

Note: It is recommended to select the 16-bit FIFO for delay-sensitive applications as well as for removing smaller amounts of jitter. Table 12 specifies the jitter transfer mask requirements for various data rates:

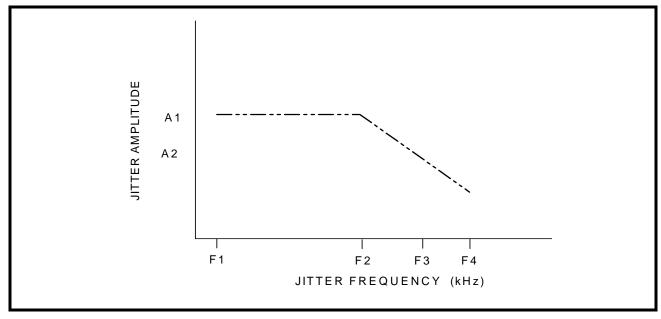


TABLE 12: JITTER TRANSFER PASS MASKS

RATE (KBITS)	Mask	F1 (Hz)	F2 (Hz)	F3 (Hz)	F4 (ĸHz)	A1(dB)	A2(dB)
34368	G.823 ETSI-TBR-24	100	300	3к	800K	0.5	-19.5
44736	GR-499, Cat I GR-499, Cat II GR-253 CORE	10 10 10	10k 56.6k 40	- - -	15k 300k 15k	0.1 0.1 0.1	- - -
51840	GR-253 CORE	10	40k	-	400k	0.1	-

The jitter attenuator within the XRT75R12 meets the latest jitter attenuation specifications and/or jitter transfer characteristics as shown in the Figure 28.

FIGURE 28. JITTER TRANSFER REQUIREMENTS AND JITTER ATTENUATOR PERFORMANCE



5.3.1 JITTER GENERATION

Jitter Generation is defined as the process whereby jitter appears at the output port of the digital equipment in the absence of applied input jitter. Jitter Generation is measured by sending jitter free data to the clock and data recovery circuit and measuring the amount of jitter on the output clock or the re-timed data. Since this is essentially a noise measurement, it requires a definition of bandwidth to be meaningful. The bandwidth is set according to the data rate. In general, the jitter is measured over a band of frequencies.

REV. 1.0.4

6.0 DIAGNOSTIC FEATURES

6.1 PRBS Generator and Detector

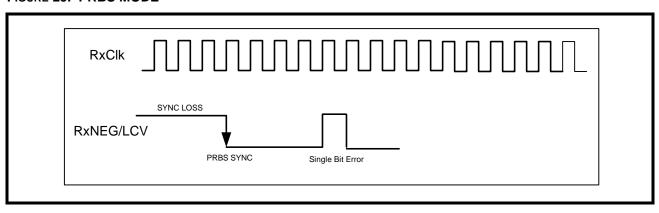
The XRT75R12 contains an on-chip Pseudo Random Binary Sequence (PRBS) generator and detector for diagnostic purpose. With the PRBSEN_n bit = "1", the transmitter will send out PRBS of 2^{23} -1 in E3 rate or 2^{15} -1 in STS-1/DS3 rate. At the same time, the receiver PRBS detector is also enabled. When the correct PRBS pattern is detected by the receiver, the RNEG/LCV pin will go "Low" to indicate PRBS synchronization has been achieved. When the PRBS detector is not in sync the PRBSLS bit will be set to "1" and RNEG/LCV pin will go "High".

With the PRBS mode enabled, the user can also insert a single bit error by toggling "INSPRBS" bit. This is done by writing a "1" to INSPRBS bit. The receiver at RNEG/LCV pin will pulse "High" for one RxClk cycle for every bit error detected. Any subsequent single bit error insertion must be done by first writing a "0" to INSPRBS bit and followed by a "1".

Figure 29 shows the status of RNEG/LCV pin when the XRT75R12 is configured in PRBS mode.

Note: In PRBS mode, the device is forced to operate in Single-Rail Mode.

FIGURE 29. PRBS MODE



6.2 LOOPBACKS

The XRT75R12 offers three loopback modes for diagnostic purposes. The loopback modes are selected via the RLB_n and LLB_n bits n the Channel control registers select the loopback modes.

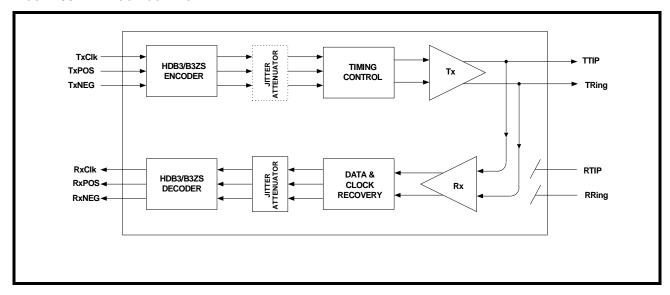
6.2.1 ANALOG LOOPBACK

In this mode, the transmitter outputs TTIP_n and TRing_n are internally connected to the receiver inputs RTIP_n and RRing_n as shown in Figure 30. Data and clock are output at RxClk_n, RxPOS_n and RxNEG_n pins for the corresponding transceiver. Analog loopback exercises most of the functional blocks of the device including the jitter attenuator which can be selected in either the transmit or receive path.

NOTES:

- 1. In the Analog loopback mode, data is also output via TTIP_n and TRing_n pins.
- 2. Signals on the RTIP_n and RRing_n pins are ignored during analog loopback.

FIGURE 30. ANALOG LOOPBACK

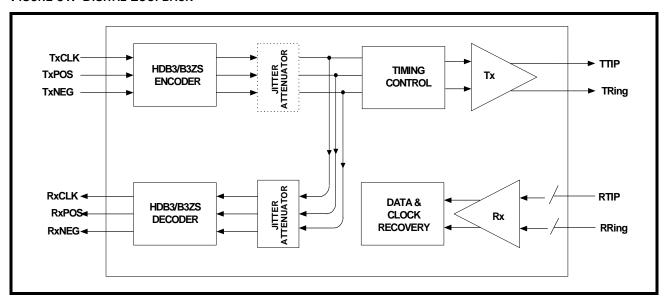


REV. 1.0.4

6.2.2 DIGITAL LOOPBACK

When the Digital Loopback is selected, the transmit clock TxClk_n and transmit data inputs (TxPOS_n & TxNEG_n are looped back and output onto the RxClk_n, RxPOS_n and RxNEG_n pins as shown in Figure 31.

FIGURE 31. DIGITAL LOOPBACK

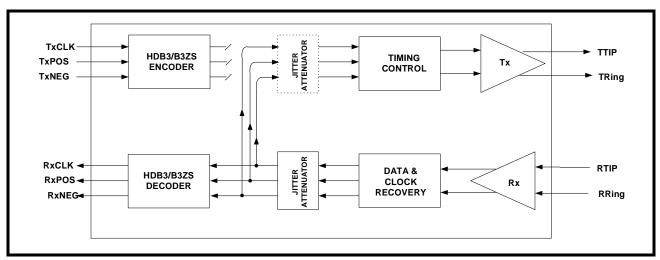


6.2.3 REMOTE LOOPBACK

With Remote loopback activated as shown in Figure 32, the receive data on RTIP and RRing is looped back after the jitter attenuator (if selected in receive or transmit path) to the transmit path using RxClk as transmit timing. The receive data is also output via the RxPOS and RxNEG pins.

Note: Input signals on TxClk, TxPOS and TxNEG are ignored during Remote loopback.

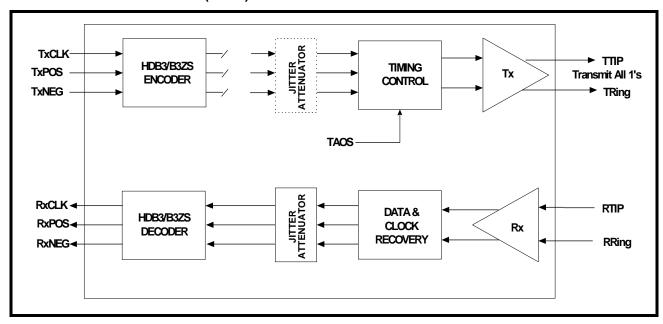
FIGURE 32. REMOTE LOOPBACK



6.3 TRANSMIT ALL ONES (TAOS)

Transmit All Ones (TAOS) can be set by setting the TAOS_n control bits to "1" in the Channel control registers. When the TAOS is set, the Transmit Section generates and transmits a continuous AMI all "1's" pattern on TTIP_n and TRing_n pins. The frequency of this ones pattern is determined by TxClk_n. the TAOS data path is shown in Figure 33. TAOS does not operate in Analog loopback or Remote loopback modes, however will function in Digital loopback mode.

FIGURE 33. TRANSMIT ALL ONES (TAOS)



REV. 1.0.4

7.0 MICROPROCESSOR INTERFACE BLOCK

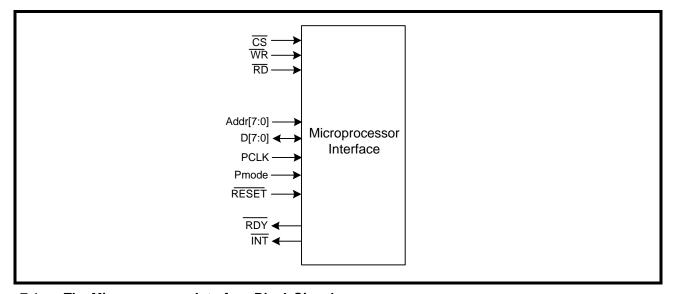
The Microprocessor Interface section supports communication between the local microprocessor (μ P) and the LIU. The XRT75R12 supports a parallel interface asynchronously or synchronously timed to the LIU. The microprocessor interface is selected by the state of the Pmode input pin. Selecting the microprocessor interface mode is shown in Table 13.

TABLE 13: SELECTING THE MICROPROCESSOR INTERFACE MODE

PMODE	MICROPROCESSOR MODE
"Low"	Asynchronous Mode
"High"	Synchronous Mode

The local μP configures the LIU by writing data into specific addressable, on-chip Read/Write registers. The μP provides the signals which are required for a general purpose microprocessor to read or write data into these registers. The μP also supports polled and interrupt driven environments. A simplified block diagram of the microprocessor is shown in Figure 34.

FIGURE 34. SIMPLIFIED BLOCK DIAGRAM OF THE MICROPROCESSOR INTERFACE BLOCK



7.1 The Microprocessor Interface Block Signals

The LIU may be configured into different operating modes and have its performance monitored by software through a standard microprocessor using data, address and control signals. These interface signals are described below in Table 14. The microprocessor interface can be configured to operate in Asynchronous mode or Synchronous mode.

TABLE 14: XRT75R12 MICROPROCESSOR INTERFACE SIGNALS

PIN NAME	Түре	DESCRIPTION
Pmode	I	Microprocessor Interface Mode Select Input pin This pin is used to specify the microprocessor interface mode.
D[7:0]	I/O	Bi-Directional Data Bus for register "Read" or "Write" Operations.
Addr[7:0]	I	Eight-Bit Address Bus Inputs The XRT75R12 LIU microprocessor interface uses a direct address bus. This address bus is provided to permit the user to select an on-chip register for Read/Write access.

TABLE 14: XRT75R12 MICROPROCESSOR INTERFACE SIGNALS

PIN NAME	Түре	DESCRIPTION
<u>CS</u>	I	Chip Select Input This active low signal selects the microprocessor interface of the XRT75R12 LIU and enables Read/Write operations with the on-chip register locations.
RD	I	Read Signal This active low input functions as the read signal from the local μP. When this pin is pulled "Low" (if \overline{CS} is "Low") the LIU is informed that a read operation has been requested and begins the process of the read cycle.
WR	I	Write Signal This active low input functions as the write signal from the local µP. When this pin is pulled "Low" (if \overline{CS} is "Low") the LIU is informed that a write operation has been requested and begins the process of the write cycle.
RDY	0	Ready Output This active low signal is provided by the LIU device. It indicates that the current read or write cycle is complete, and the LIU is waiting for the next command.
ĪNT	0	Interrupt Output This active low signal is provided by the LIU to alert the local mP that a change in alarm status has occured. This pin is Reset Upon Read (RUR) once the alarm status registers have been cleared.
RESET	1	Reset Input This active low input pin is used to Reset the LIU.

7.2 Asynchronous and Synchronous Description

Whether the LIU is configured for Asynchronous or Synchronous mode, the following descriptions apply. The synchronous mode requires an input clock (PCLK) to be used as the microprocessor timing reference. Read and Write operations are described below.

Read Cycle (For Pmode = "0" or "1")

Whenever the local µP wishes to read the contents of a register, it should do the following.

- 1. Place the address of the target register on the address bus input pins Addr[7:0].
- 2. While the $\underline{\mu P}$ is placing this address value on the address bus, the address decoding circuitry should assert the \overline{CS} pin of the LIU, by toggling it "Low". This action enables communication between the μP and the LIU microprocessor interface block.
- 3. Next, the μP should indicate that this current bus cycle is a Read operation by toggling the RD input pin "Low". This action enables the bi-directional data bus output drivers of the LIU.
- **4.** After the μ P toggles the Read signal "Low", the LIU will toggle the \overline{RDY} output pin "Low". The LIU does this to inform the μ P that the data is available to be read by the μ P, and that it is ready for the next command.
- 5. After the μP detects the RDY signal and has read the data, it can terminate the Read Cycle by toggling the RD input pin "High".
- **6.** The $\overline{\text{CS}}$ input pin must be pulled "High" before a new command can be issued.

Write Cycle (For Pmode = "0" or "1")

Whenever a local μP wishes to write a byte or word of data into a register within the LIU, it should do the following.

- 1. Place the address of the target register on the address bus input pins Addr[7:0].
- 2. While the μP is placing this address value on the address bus, the address decoding circuitry should assert the \overline{CS} pin of the LIU, by toggling it "Low". This action enables communication between the μP and the LIU microprocessor interface block.
- 3. The μ P should then place the byte or word that it intends to write into the target register, on the bi-directional data bus D[7:0].
- **4.** Next, the μ P should indicate that this current bus cycle is a Write operation by toggling the \overline{WR} input pin "Low". This action enables the bi-directional data bus input drivers of the LIU.

REV. 1.0.4

- 5. After the μP toggles the Write signal "Low", the LIU will toggle the \overline{RDY} output pin "Low". The LIU does this to inform the μP that the data has been written into the internal register location, and that it is ready for the next command.
- **6.** The \overline{CS} input pin must be pulled "High" before a new command can be issued.

FIGURE 35. ASYNCHRONOUS µP INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

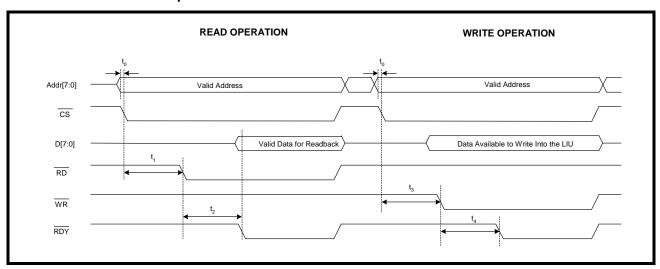


TABLE 15: ASYNCHRONOUS TIMING SPECIFICATIONS

SYMBOL	PARAMETER	Min	Max	Units
t ₀	Valid Address to CS Falling Edge	0	-	ns
t ₁	CS Falling Edge to RD Assert	0	-	ns
t ₂	RD Assert to RDY Assert	-	65	ns
NA	RD Pulse Width (t ₂)	70	-	ns
t ₃	CS Falling Edge to WR Assert	0	-	ns
t ₄	WR Assert to RDY Assert	-	65	ns
NA	WR Pulse Width (t ₄)	70	-	ns

FIGURE 36. SYNCHRONOUS µP INTERFACE SIGNALS DURING PROGRAMMED I/O READ AND WRITE OPERATIONS

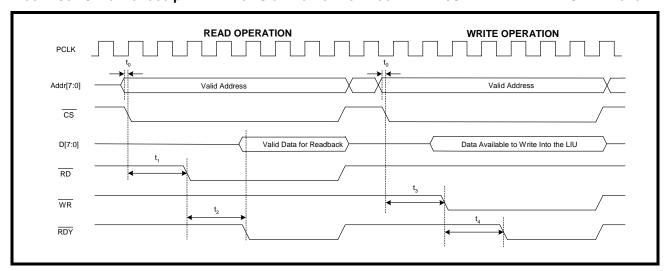


TABLE 16: SYNCHRONOUS TIMING SPECIFICATIONS

SYMBOL	PARAMETER	Min	Max	Units
t_0	Valid Address to CS Falling Edge	0	-	ns
t ₁	CS Falling Edge to RD Assert	0	-	ns
t ₂	RD Assert to RDY Assert	-	35	ns, see note 1
NA	RD Pulse Width (t ₂)	40	-	ns
t ₃	CS Falling Edge to WR Assert	0	-	ns
t ₄	WR Assert to RDY Assert	-	35	ns, see note 1
NA	WR Pulse Width (t ₄)	40	-	ns
	PCLK Period	15		ns
	PCLK Duty Cycle			
	PCLK "High/Low" time			

Note: 1. This timing parameter is based on the frequency of the synchronous clock (PCLK). To determine the access time, use the following formula: (PCLK_{period} * 2) + 5ns

7.3 Register Map

TABLE 17: COMMAND REGISTER ADDRESS MAP, WITHIN THE XRT75R12

Address (Hex)	COMMAND REGISTER (DECIMAL)	LABEL	Түре	REGISTER NAME			
0x00	CR0	APST	R/W	APS Transmit Redundancy Control Register 0-5			
	CHANNEL 0 CONTROL REGISTERS						
0x01	CR1	IER0	R/W	Source Level Interrupt Enable Register - Ch 0			
0x02	CR2	ISR0	RUR	Source Level Interrupt Status Register Ch 0			

REV. 1.0.4

Address (Hex)	COMMAND REGISTER (DECIMAL)	LABEL	Түре	REGISTER NAME
0x03	CR3	AS0	R/O	Alarm Status Register - Ch 0
0x04	CR4	TC0	R/W	Transmit Control Register - Ch 0
0x05	CR5	RC0	R/W	Receive Control Register - Ch 0
0x06	CR6	CC0	R/W	Channel Control Register - Ch 0
0x07	CR7	JA0	R/W	Jitter Attenuator Control Register - Ch 0
0x08	CR8	APSR	R/W	APS Receive Redundancy Control Register 0-5
0x09				
0x0A	CR10	EM0	R/W	Error counter MS Byte Ch 0
0x0B	CR11	EL0	R/W	Error counter LS Byte
0x0C	CR12	EH0	R/W	Error counter Holding register
0x0D				
0x0E				
0x0F	0x0F			
0x10				
	Сна	NNEL 1 Co	NTROL REG	GISTERS
0x11	CR17	IER1	R/W	Source Level Interrupt Enable Register - Ch 1
0x12	CR18	ISR1	RUR	Source Level Interrupt Status Register - Ch 1
0x13	CR19	AS1	R/O	Alarm Status Register - Ch 1
0x14	CR20	TC0	R/W	Transmit Control Register - Ch 1
0x15	CR21	RC1	R/W	Receive Control Register - Ch 1
0x16	CR22	CC1	R/W	Channel Control Register - Ch 1
0x17	CR23	JA1	R/W	Jitter Attenuator Control Register - Ch 1
0x18				
0x19				
0x1A	CR26	EM1	R/W	Error counter MSByte Ch 1
0x1B	CR27	EL1	R/W	Error counter LSbyte
0x1C	CR28	EH1	R/W	Error counter Holding register
0x1D				
0x1E				
0x1F				
0x20				
	Сна	NNEL 2 Co	NTROL REG	GISTERS

Address (Hex)	COMMAND REGISTER (DECIMAL)	I ABEL TYPE REGISTER NAME			
0x21	CR33	IER2	R/W	Source Level Interrupt Enable Register - Ch 2	
0x22	CR34	ISR2	RUR	Source Level Interrupt Status Register - Ch 2	
0x23	CR35	AS2	R/O	Alarm Status Register - Ch 2	
0x24	CR36	TC2	R/W	Transmit Control Register - Ch 2	
0x25	CR37	RC2	R/W	Receive Control Register - Ch 2	
0x26	CR38	CC2	R/W	Channel Control Register - Ch 2	
0x27	CR39	JA2	R/W	Jitter Attenuator Control Register - Ch 2	
0x28					
0x29					
0x2A	CR42	EM2	R/W	Error counter MSByte Ch 2	
0x2B	CR43	EL2	R/W	Error counter LSbyte	
0x2C	CR44	EH2	R/W	Error counter Holding register	
0x2D					
0x2E					
0x2F					
0x30					
	Сна	NNEL 3 CO	NTROL REG	GISTERS	
0x31	CR49	IER3	R/W	Source Level Interrupt Enable Register - Ch 3	
0x32	CR50	ISR3	RUR	Source Level Interrupt Status Register - Ch 3	
0x33	CR51	AS3	R/O	Alarm Status Register - Ch 3	
0x34	CR52	TC3	R/W	Transmit Control Register - Ch 3	
0x35	CR53	RC3	R/W	Receive Control Register - Ch 3	
0x36	CR54	CC3	R/W	Channel Control Register - Ch 3	
0x37	CR55	JA3	R/W	Jitter Attenuator Control Register - Ch 3	
0x38					
0x39					
0x3A	CR58	EM3	R/W	Error counter MSByte Ch 3	
0x3B	CR59	EL3	R/W	Error counter LSbyte	
0x3C	CR60	EH3	R/W	Error counter Holding register	
0x3D					
0x3E					
0x3F					

REV. 1.0.4

Address (Hex)	COMMAND REGISTER (DECIMAL)	LABEL	Түре	REGISTER NAME					
0x40									
	CHANNEL 4 CONTROL REGISTERS								
0x41	CR65	IER4	R/W	Source Level Interrupt Enable Register - Ch 4					
0x42	CR66	ISR4	RUR	Source Level Interrupt Status Register - Ch 4					
0x43	CR67	AS4	R/O	Alarm Status Register - Ch 4					
0x44	CR68	TC4	R/W	Transmit Control Register - Ch 4					
0x45	CR69	RC4	R/W	Receive Control Register - Ch 4					
0x46	CR70	CC4	R/W	Channel Control Register - Ch 4					
0x47	CR71	JA4	R/W	Jitter Attenuator Control Register - Ch 4					
0x48									
0x49									
0x4A	0x4A CR74			Error counter MSByte Ch 4					
0x4B	0x4B CR75			Error counter LSbyte					
0x4C	0x4C CR76		R/W	Error counter Holding register					
0x4D									
0x4E									
0x4F									
0x50									
	Сна	NNEL 5 CO	NTROL REG	GISTERS					
0x51	CR81	IER5	R/W	Source Level Interrupt Enable Register - Ch 5					
0x52	CR82	ISR5	RUR	Source Level Interrupt Status Register - Ch 5					
0x53	CR83	AS5	R/O	Alarm Status Register - Ch 5					
0x54	CR84	TC5	R/W	Transmit Control Register - Ch 5					
0x55	CR85	RC5	R/W	Receive Control Register - Ch 5					
0x56	CR86	CC5	R/W	Channel Control Register - Ch 5					
0x57	CR87	JA5	R/W	Jitter Attenuator Control Register - Ch 5					
0x58									
0x59									
0x5A	CR90	EM5	R/W	Error counter MSByte Ch 5					
0x5B	CR91	EL5	R/W	Error counter LSbyte					
0x5C	CR92	EH5	R/W	Error counter Holding register					
0x5D									

Address (Hex)	COMMAND REGISTER (DECIMAL)	LABEL	Түре	REGISTER NAME
0x5E				
0x5F				
0x60	CR96	CIE	R/W	Channel 0-5 Interrupt Enable flags
0x61	CR97	CIS	R/O	Channel 0-5 Interrupt status flags
0x62				
0x63				
0x64				
0x65				
0x66				
0x67				
0x68				
0x65				
0x69				
0x6A				
0x6B				
0x6C				
0x6D				
0x6E	CR110	PN	R/O	Device Part Number Register
0x6F	CR111	VN	R/O	Chip Revision Number Register
0x70				
0x71				
0x72				
0x73				
0x74				
0x75				
0x76				
0x77				
0x78				
0x75				
0x79				
0x7A				
0x7B				

REV. 1.0.4

Address (Hex)	COMMAND REGISTER (DECIMAL)	LABEL	Түре	REGISTER NAME					
0x7C									
0x7D									
0x7E									
0x7F									
0x80	CR128	APST	R/W	APS Transmit Redundancy Control Register 6-11					
	CHANNEL 6 CONTROL REGISTERS								
0x81	CR129	IER6	R/W	Source Level Interrupt Enable Register - Ch 6					
0x82	0x82 CR130			Source Level Interrupt Status Register - Ch 6					
0x83	CR131	AS6	R/O	Alarm Status Register - Ch 6					
0x84	CR132	TC6	R/W	Transmit Control Register - Ch 6					
0x85	CR133	RC6	R/W	Receive Control Register - Ch 6					
0x86	CR134	CC6	R/W	Channel Control Register - Ch 6					
0x87	CR135	JA6	R/W	Jitter Attenuator Control Register - Ch 6					
0x88	CR136	APSR	R/W	APS Receive Redundancy Control Register 6-11					
0x89									
0x8A	CR138	EM6	R/W	Error counter MSByte Ch 6					
0x8B	CR139	EL6	R/W	Error counter LSbyte					
0x8C	CR140	EH6	R/W	Error counter Holding register					
0x8D									
0x8E									
0x8F									
0x90									
	Сна	NNEL 7 Co	NTROL REG	GISTERS					
0x91	CR145	IER7	R/W	Source Level Interrupt Enable Register - Ch 7					
0x92	CR146	ISR7	RUR	Source Level Interrupt Status Register - Ch 7					
0x93	CR147	AS7	R/O	Alarm Status Register - Ch 7					
0x94	CR148	TC7	R/W	Transmit Control Register - Ch 7					
0x95	CR149	RC7	R/W	Receive Control Register - Ch 7					
0x96	CR150	CC7	R/W	Channel Control Register - Ch 7					
0x97	CR151	JA7	R/W	Jitter Attenuator Control Register - Ch 7					
0x98									
0x99									

Address (Hex)	COMMAND REGISTER (DECIMAL)	LABEL	Түре			
0x9A	CR154	EM7	R/W	Error counter MSByte Ch 7		
0x9B	CR155	EL7	R/W	Error counter LSbyte		
0x9C	CR156	EH7	R/W	Error counter Holding register		
0x9D						
0x9E						
0x9F						
0xA0						
	Сна	NNEL 8 CC	NTROL REG	GISTERS		
0xA1	CR161	IER8	R/W	Source Level Interrupt Enable Register - Ch 8		
0xA2	CR162	ISR8	RUR	Source Level Interrupt Status Register - Ch 8		
0xA3	CR163	AS8	R/O	Alarm Status Register - Ch 8		
0xA4	CR164	TC8	R/W	Transmit Control Register - Ch 8		
0xA5	CR165	RC8	R/W	Receive Control Register - Ch 8		
0xA6	CR166	CC8	R/W	Channel Control Register - Ch 8		
0xA7	CR167	JA8	R/W	Jitter Attenuator Control Register - Ch 8		
0xA8						
0xA9						
0xAA	CR170	EM8	R/W	Error counter MSByte Ch 8		
0xAB	CR171	EL8	R/W	Error counter LSbyte		
0xAC	CR172	EH8	R/W	Error counter Holding register		
0xAD						
0xAE						
0xAF						
0xB0						
	Сна	NNEL 9 CC	NTROL REG	GISTERS		
0xB1	CR177	IER9	R/W	Source Level Interrupt Enable Register - Ch 9		
0xB2	CR178	ISR9	RUR	Source Level Interrupt Status Register - Ch 9		
0xB3	CR179	AS9	R/O	Alarm Status Register - Ch 9		
0xB4	CR180	TC9	R/W	Transmit Control Register - Ch 9		
0xB5	CR181	RC9	R/W	Receive Control Register - Ch 9		
0xB6	CR182	CC9	R/W	Channel Control Register - Ch 9		
0xB7	CR183	JA9	R/W	Jitter Attenuator Control Register - Ch 9		

REV. 1.0.4

Address (Hex)	COMMAND REGISTER (DECIMAL)	LABEL	Түре	REGISTER NAME	
0xB8					
0xB9					
0xBA	CR186	EM9	R/W	Error counter MSByte Ch 9	
0xBB	CR187	EL9	R/W	Error counter LSbyte	
0xBC	CR188	EH9	R/W	Error counter Holding register	
0xBD					
0xBE					
0xBF					
0xC0					
	Снал	NEL 10 C	ONTROL RE	GISTERS	
0xC1	CR193	IER10	R/W	Source Level Interrupt Enable Register - Ch 10	
0xC2	CR194	ISR10	RUR	Source Level Interrupt Status Register - Ch 10	
0xC3	CR195	AS10	R/O	Alarm Status Register - Ch 10	
0xC4	CR196	TC10	R/W	Transmit Control Register - Ch 10	
0xC5	CR197	RC10	R/W	Receive Control Register - Ch 10	
0xC6	CR198	CC10	R/W	Channel Control Register - Ch 10	
0xC7	CR199	JA10	R/W	Jitter Attenuator Control Register - Ch 10	
0xC8					
0xC9					
0xCA	CR202	EM10	R/W	Error counter MSByte Ch 10	
0xCB	CR203	EL10	R/W	Error counter LSbyte	
0xCC	CR204	EH10	R/W	Error counter Holding register	
0xCD					
0xCE					
0xCF					
0xD0					
CHANNEL 11 CONTROL REGISTERS					
0xD1	CR209	IER11	R/W	Source Level Interrupt Enable Register - Ch 11	
0xD2	CR210	ISR11	RUR	Source Level Interrupt Status Register - Ch 11	
0xD3	CR211	AS11	R/O	Alarm Status Register - Ch 11	
0xD4	CR212	TC11	R/W	Transmit Control Register - Ch 11	
0xD5	CR213	RC11	R/W	Receive Control Register - Ch 11	

Address (Hex)	COMMAND REGISTER (DECIMAL)	LABEL	Түре	REGISTER NAME
0xD6	CR214	CC11	R/W	Channel Control Register - Ch 11
0xD7	CR215	JA11	R/W	Jitter Attenuator Control Register - Ch 11
0xD8				
0xD9				
0xDA	CR218	EM11	R/W	Error counter MSByte Ch 11
0xDB	CR219	EL11	R/W	Error counter LSbyte
0xDC	CR229	EH11	R/W	Error counter Holding register
0xDD				
0xDE				
0xDF				
0xE0	CR224	CIE	R/W	Channel 6-11 Interrupt enable flags
0xE1	CR225	CIS	R/O	Channel 6-11 Interrupt status flags
0xE2				
0xE3				
0xE4				
0xE5				
0xE6				
0xE7				
0xE8				
0xE5				
0xE9				
0xEA				
0xEB				
0xEC				
0xED				
0xEE				
0xEF				
0xF0				
0xF1				
0xF2				
0xF3				
0xF4				

REV. 1.0.4

TABLE 17: COMMAND REGISTER ADDRESS MAP, WITHIN THE XRT75R12

Address (Hex)	COMMAND REGISTER (DECIMAL)	LABEL	Түре	REGISTER NAME
0xF5				
0xF6				
0xF7				
0xF8				
0xF5				
0xF9				
0xFA				
0xFB				
0xFC				
0xFD				
0xFE				
0xFF				

THE GLOBAL/CHIP-LEVEL REGISTERS

The register set, within the XRT75R12 contains ten global or chip-level registers. These registers control operations in more than one channel or apply to the complete chip. This section will present detailed information on the Global Registers.

TABLE 18: LIST AND ADDRESS LOCATIONS OF GLOBAL REGISTERS

Address	COMMAND REGISTER	LABEL	Түре	REGISTER NAME
0x00	CR0	APST	R/W	APS Transmit Redundancy Control Register 0-5
0x08	CR8	APSR	R/W	APS Receive Redundancy Control Register 0-5
0x80	CR128	APST	R/W	APS Transmit Redundancy Control Register 6-11
0x88	CR136	APSR	R/W	APS Receive Redundancy Control Register 6-11
0x60	CR96	CIE	R/W	Channel 0-5 Interrupt Enable flags
0x61	CR97	CIS	R/O	Channel 0-5 Interrupt status flags
0xE0	CR224	CIE	R/W	Channel 6-11 Interrupt Enable flags
0xE1	CR225	CIS	R/O	Channel 6-11 Interrupt status flags
0x6E	CR110	PN	ROM	Device Part Number Register
0x6F	CR111	VN	ROM	Chip Revision/Version Number Register

REGISTER DESCRIPTION - GLOBAL REGISTERS

TABLE 19: APS/REDUNDANCY TRANSMIT CONTROL REGISTER - CR0 (ADDRESS LOCATION = 0x00)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Reserved	Reserved	TxON Ch 5	TxON Ch 4	TxON Ch 3	TxON Ch 2	TxON Ch 1	TxON Ch 0
		R/W	R/W	R/W	R/W	R/W	R/W

BIT Number	NAME	Түре	DESCRIPTION
7,6	Reserved		
5 4 3 2 1 0	TxON Ch 5 TxON Ch 4 TxON Ch 3 TxON Ch 2 TxON Ch 1 TxON Ch 0	R/W	Transmit Section ON - Channel n This READ/WRITE bit-field is used to turn on or turn off the Transmit Driver associated with Channel n. If the user turns on the Transmit Driver, then Channel n will transmit DS3, E3 or STS-1 pulses on the line via the TTIP_n and TRING_n output pins. Conversely, if the user turns off the Transmit Driver, then the TTIP_n and TRING_n output pins will be tri-stated. 0 - Shuts off the Transmit Driver associated with Channel n and tri-states the TTIP_n and TRING_n output pins. 1 - Turns on the Transmit Driver associated with Channel n. NOTE: The master TxON control pin(pin # P4) must be in a high state (logic 1) for this operation to turn on any channel.

TABLE 20: APS/REDUNDANCY RECIEVE CONTROL REGISTER - CR8 (ADDRESS LOCATION = 0x08)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Reserved	Reserved	RxON Ch 5	RxON Ch 4	RxON Ch 3	RxON Ch 2	RxON Ch 1	RxON Ch 0
		R/W	R/W	R/W	R/W	R/W	R/W

BIT Number	NAME	Түре	DESCRIPTION
7,6	Reserved		
5	RxON Ch 5	R/W	Receive Section ON - Channel n
4	RxON Ch 4		This READ/WRITE bit-field is used to turn on or turn off the Receiver associated with
3	RxON Ch 3		Channel n on a per channel basis. If the user turns on the Receiver, then Channel n
2	RxON Ch 2		will Receive DS3, E3 or STS-1 pulses on the line via the RTIP_n and RRING_ n input
1	RxON Ch 1		pins. Conversely if the year turns off the Bessiver Driver (for channel s), the BTID is and
0	RxON Ch 0		Conversely, if the user turns off the Receiver Driver (for channel n), the RTIP_n and RRING_n input pins will be in a high impedance state.
			0 - Shuts off the Receive Driver associated with Channel n and puts the RTIP_n and RRING_ n input pins in a high impedance state.
			1 - Turns on the Receive Driver associated with Channel n.

REV. 1.0.4

TABLE 21: APS/REDUNDANCY TRANSMIT CONTROL REGISTER - CR128 (ADDRESS LOCATION = 0x80)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Reserved	Reserved	TxON Ch 11	TxON Ch 10	TxON Ch 9	TxON Ch 8	TxON Ch 7	TxON Ch 6
		R/W	R/W	R/W	R/W	R/W	R/W

BIT Number	NAME	Түре	DESCRIPTION
7,6	Reserved		
5 4 3 2 1 0	TxON Ch 11 TxON Ch 10 TxON Ch 9 TxON Ch 8 TxON Ch 7 TxON Ch 6	R/W	Transmit Section ON - Channel n This READ/WRITE bit-field is used to turn on or turn off the Transmit Driver associated with Channel n. If the user turns on the Transmit Driver, then Channel n will transmit DS3, E3 or STS-1 pulses on the line via the TTIP_n and TRING_n output pins. Conversely, if the user turns off the Transmit Driver, then the TTIP_n and TRING_n output pins will be tri-stated. 0 - Shuts off the Transmit Driver associated with Channel n and tri-states the TTIP_n and TRING_n output pins. 1 - Turns on the Transmit Driver associated with Channel n. NOTE: The master TxON control pin(pin # P4) must be in a high state (logic 1) for this operation to turn on any channel.

TABLE 22: APS/REDUNDANCY RECIEVE CONTROL REGISTER - CR136 (ADDRESS LOCATION = 0x88)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Reserved	Reserved	RxON Ch 11	RxON Ch 10	RxON Ch 9	RxON Ch 8	RxON Ch 7	RxON Ch 6
		R/W	R/W	R/W	R/W	R/W	R/W

BIT Number	NAME	Түре	DESCRIPTION
7,6	Reserved		
5	RxON Ch 11	R/W	Receive Section ON - Channel n
4	RxON Ch 10		This READ/WRITE bit-field is used to turn on or turn off the Receiver associated with
3	RxON Ch 9		Channel n on a per channel basis. If the user turns on the Receiver, then Channel n
2	RxON Ch 8		will Receive DS3, E3 or STS-1 pulses on the line via the RTIP_n and RRING_ n input
1	RxON Ch 7		pins.
0	RxON Ch 6		Conversely, if the user turns off the Receiver Driver (for channel n), the RTIP_n and RRING_n input pins will be in a high impedance state.
			0 - Shuts off the Receive Driver associated with Channel n and puts the RTIP_n and RRING_ n input pins in a high impedance state.
			1 - Turns on the Receive Driver associated with Channel n.

TABLE 23: CHANNEL LEVEL INTERRUPT ENABLE REGISTER - CR96 (ADDRESS LOCATION = 0x60)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Reserved	Reserved	Channel 5 Interrupt Enable	Channel 4 Interrupt Enable	Channel 3 Interrupt Enable	Channel 2 Interrupt Enable	Channel 1 Interrupt Enable	Channel 0 Interrupt Enable
		R/W	R/W	R/W	R/W	R/W	R/W

channel n Interrupt Enable Bit: his READ/WRITE bit is used to: To enable Channel n for Interrupt Generation at the Channel Level To disable all Interrupts associated with Channel n within the XRT75R12 his is a "master" enable bit for <i>each</i> channel. This bit allows ontrol on a per channel basis to signal the Host of selected error onditions. a bit is cleared, no interrupts from that channel will be sent to the lost via the INT. the bit is set (logic 1), any generated interrupt in channel n that as been enabled in the Interrupt Enable register (IERn) for the hannel will activate the INT pin to the Host Disables all Channel n related Interrupts Enables Channel n-related Interrupts. The user must enable
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REV. 1.0.4

TABLE 24: CHANNEL LEVEL INTERRUPT STATUS REGISTER - CR97 (ADDRESS LOCATION = 0x61)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Reserved	Reserved	Channel 5 Interrupt Sta- tus	Channel 4 Interrupt Sta- tus	Channel 3 Interrupt Sta- tus	Channel 2 Interrupt Sta- tus	Channel 1 Interrupt Sta- tus	Channel 0 Interrupt Sta- tus
		R/O	R/O	R/O	R/O	R/O	R/O

BIT Number	Name	Түре	DESCRIPTION
7, 6	Reserved		
5 4 3 2 1 0	Channel 5 Interrupt Status Channel 4 Interrupt Status Channel 3 Interrupt Status Channel 2 Interrupt Status Channel 1 Interrupt Status Channel 0 Interrupt Status	R/O	Channel n Interrupt Status Bit: This READ-ONLY bit-field indicates whether the XRT75R12 has a pending Channel n-related interrupt that is awaiting service. The first six channels are serviced through this location and the other six at address 0xE1. These two registers are used by the Host to identify the source channel of an active interrupt. 0 - Indicates that there is NO Channel n-related Interrupt awaiting service. 1 - Indicates that there is at least one Channel n-related Interrupt awaiting service. In this case, the user's Interrupt Service routine should be written such that the Microprocessor will now proceed to read out the contents of the Source Level Interrupt Status Register - Channel n (Address Locations = 0xn2) to determine the exact source of the interrupt request. Note: Once this bit-field is set to "1", it will not be cleared back to "0" until the user has read out the contents of the Source-Level Interrupt Status Register bit, that corresponds to the interrupt request channel.

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TABLE 25: CHANNEL LEVEL INTERRUPT ENABLE REGISTER - CR224 (ADDRESS LOCATION = 0xE0)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Reserved	Reserved	Channel 11 Interrupt Enable	Channel 10 Interrupt Enable	Channel 9 Interrupt Enable	Channel 8 Interrupt Enable	Channel 7 Interrupt Enable	Channel 6 Interrupt Enable
		R/W	R/W	R/W	R/W	R/W	R/W

BIT Number	NAME	Түре	DESCRIPTION
7,6	Reserved		
5 4 3 2 1 0	Channel 11 Interrupt Enable Channel 10 Interrupt Enable Channel 9 Interrupt Enable Channel 8 Interrupt Enable Channel 7 Interrupt Enable Channel 6 Interrupt Enable	R/W	Channel n Interrupt Enable Bit: This READ/WRITE bit is used to: • To enable Channel n for Interrupt Generation at the Channel Level • To disable all Interrupts associated with Channel n within the XRT75R12 This is a "master" enable bit for each channel. This bit allows control on a per channel basis to signal the Host of selected error conditions. If a bit is cleared, no interrupts from that channel will be sent to the Host via the INT pin. If the bit is set (logic 1), any generated interrupt in channel n that has been enabled in the Interrupt Enable register (IERn) for the channel will activate the INT pin to the Host. 0 - Disables all Channel n related Interrupts. 1 - Enables Channel n-related Interrupts at the source level, before

REV. 1.0.4

TABLE 26: CHANNEL LEVEL INTERRUPT STATUS REGISTER - CR225 (ADDRESS LOCATION = 0xE1)

Віт 7	Віт 6	Віт 5	Віт 4	BIT 3 BIT 2		Віт 1	Віт 0
Reserved	Reserved		Channel 10 Interrupt Status	Channel 9 Interrupt Status	Channel 8 Interrupt Status	Channel 7 Interrupt Status	Channel 6 Interrupt Status
		R/O	R/O	R/O	R/O	R/O	R/O

BIT Number	NAME	Түре	DESCRIPTION
7, 6	Reserved		
5 4 3 2 1 0	Channel 11 Interrupt Status Channel 10 Interrupt Status Channel 9 Interrupt Status Channel 8 Interrupt Status Channel 7 Interrupt Status Channel 6 Interrupt Status	R/O	Channel n Interrupt Status Bit: This READ-ONLY bit-field indicates whether the XRT75R12 has a pending Channel n-related interrupt that is awaiting service. The last six channels are serviced through this location and the other six at address 0x61. These two registers are used by the Host to identify the source channel of an active interrupt. 0 - Indicates that there is NO Channel n-related Interrupt awaiting service. 1 - Indicates that there is at least one Channel n-related Interrupt awaiting service. In this case, the user's Interrupt Service routine should be written such that the Microprocessor will now proceed to read out the contents of the Source Level Interrupt Status Register - Channel n (Address Locations = 0xn2) to determine the exact source of the interrupt request. Note: Once this bit-field is set to "1", it will not be cleared back to "0" until the user has read out the contents of the Source-Level Interrupt Status Register bit, that corresponds to the interrupt request channel.

TABLE 27: DEVICE/PART NUMBER REGISTER - CR110 (ADDRESS LOCATION = 0x6E)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Part Number ID Value									
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
0	1	1	1	1	0	0	0		

BIT NUMBER	Name	Түре	DEFAULT VALUE	DESCRIPTION
7 - 0	Part Number ID Value	R/O		Part Number ID Value: This READ-ONLY register contains a unique value for the XRT75R12. This value will always be 0x78.

Table 28: Chip Revision Number Register - CR111 (Address Location = 0x6F)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0		
Chip Revision Number Value									
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O		
0	0	0	0	Х	Х	Х	Х		

BIT NUMBER	NAME	Түре	DEFAULT VALUE	DESCRIPTION
7 - 0	Chip Revision Number Value	R/O	0x0#	Chip Revision Number Value: This READ-ONLY register contains a value that represents the current revision of this XRT75R12. This revision number will always be in the form of "0x0#", where "#" is a hexadecimal value that specifies the current revision of the chip. For example, the very first revision of this chip will contain the value "0x01".

XRT75R12



TWELVE CHANNEL E3/DS3/STS-1 LINE INTERFACE UNIT WITH JITTER ATTENUATOR

REV. 1.0.4

THE PER-CHANNEL REGISTERS

The XRT75R12 consists of 120 per-Channel Registers (12 channels and 10 registers per channel). Table 29 presents the overall Register Map with the Per-Channel Registers unshaded.

REGISTER DESCRIPTION - PER CHANNEL REGISTERS

TABLE 29: XRT75R12 REGISTER MAP SHOWING INTERRUPT ENABLE REGISTERS (IER_N)

Address Location	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	E	F
0x0-	APST	IER0	ISR0	AS0	TC0	RC0	CC0	JA0	APSR		EM0	EL0	EH0			
0x1-		IER1	ISR1	AS1	TC1	RC1	CC1	JA1			EM1	EL1	EH1			
0x2-		IER2	ISR2	AS2	TC2	RC2	CC2	JA2			EM2	EL2	EH2			
0x3-		IER3	ISR3	AS3	TC3	RC3	CC3	JA3			ЕМ3	EL3	EH3			
0x4-		IER4	ISR4	AS4	TC4	RC4	CC4	JA4			EM4	EL4	EH4			
0x5-		IER5	ISR5	AS5	TC5	RC5	CC5	JA5			EM5	EL5	EH5			
0x6-	CIE	CIS													PN	VN
0x7-																
0x8-	APST	IER6	ISR6	AS6	TC6	RC6	CC6	JA6	APSR		EM6	EL6	EH6			
0x9-		IER7	ISR7	AS7	TC7	RC7	CC7	JA7			EM7	EL7	EH7			
0xA-		IER8	ISR8	AS8	TC8	RC8	CC8	JA8			EM8	EL8	EH8			
0xB-		IER9	ISR9	AS9	TC9	RC9	CC9	JA9			EM9	EL9	EH9			
0xC-		IER10	ISR10	AS10	TC10	RC10	CC10	JA10			EM10	EL10	EH10			
0xD-		IER11	ISR11	AS11	TC11	RC11	CC11	JA11			EM11	EL11	EH11			
0xE-	CIE	CIS														
0xF-																

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TABLE 30: SOURCE LEVEL INTERRUPT ENABLE REGISTER - CHANNEL n ADDRESS LOCATION = 0xm1 (n = [0:11] & M= 0-5 & 8-D)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Rese	erved		Change of FL	Change of LOL	Change of LOS	Change of
				Condition	Condition	Condition	DMO Condition
				Interrupt Enable	Interrupt Enable	Interrupt Enable	Interrupt Enable
				Ch n	Ch n	Ch n	Ch n
				R/W	R/W	R/W	R/W

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 4	Reserved	R/O	
3	Change of FL Condition Interrupt Enable - Ch n	R/W	 Change of FL (FIFO Limit Alarm) Condition Interrupt Enable - Ch n: This READ/WRITE bit-field is used to enable or disable the Change of FIFO Limit Alarm Condition Interrupt. If the user enables this interrupt, the XRT75R12 will generate an interrupt if any of the following events occur. Whenever the Jitter Attenuator (within Channel n) declares the FL (FIFO Limit Alarm) condition. Whenever the Jitter Attenuator (within Channel n) clears the FL (FIFO Limit Alarm) condition. Disables the Change in FL Condition Interrupt. Enables the Change in FL Condition Interrupt.
2	Change of LOL Condition Interrupt Enable	R/W	Change of Receive LOL (Loss of Lock) Condition Interrupt Enable - Channel n: This READ/WRITE bit-field is used to enable or disable the Change of Receive LOL Condition Interrupt. If the user enables this interrupt, then the XRT75R12 will generate an interrupt any time any of the following events occur. • Whenever the Receive Section (within Channel n) declares the Loss of Lock Condition. • Whenever the Receive Section (within Channel n) clears the Loss of Lock Condition. 0 - Disables the Change in Receive LOL Condition Interrupt. 1 - Enables the Change in Receive LOL Condition Interrupt.

REV. 1.0.4

BIT NUMBER	NAME	Түре	DESCRIPTION
1	Change of LOS Condition Interrupt Enable	R/W	Change of the Receive LOS (Loss of Signal) Defect Condition Interrupt Enable - Ch 0: This READ/WRITE bit-field is used to enable or disable the Change of the Receive LOS Defect Condition Interrupt. If the user enables this interrupt, then the XRT75R12 will generate an interrupt any time any of the following events occur. • Whenever the Receive Section (within Channel n) declares the LOS Defect Condition. • Whenever the Receive Section (within Channel n) clears the LOS Defect condition. 1 - Disables the Change in the LOS Defect Condition Interrupt.
0	Change of DMO Condition Interrupt Enable	R/W	Change of Transmit DMO (Drive Monitor Output) Condition Interrupt Enable - Ch n: This READ/WRITE bit-field is used to enable or disable the Change of Transmit DMO Condition Interrupt. If the user enables this interrupt, then the XRT75R12 will generate an interrupt any time any of the following events occur. • Whenever the Transmit Section toggles the DMO output pin (or bit-field) to "1". • Whenever the Transmit Section toggles the DMO output pin (or bit-field) to "0". 0 - Disables the Change in the DMO Condition Interrupt. 1 - Enables the Change in the DMO Condition Interrupt.

TABLE 31: XRT75R12 REGISTER MAP SHOWING INTERRUPT STATUS REGISTERS (ISR_n)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
	Rese	erved		Change of FL	Change of LOL	Change of LOS	Change of DMO
				Condition	Condition	Condition	Condition
				Interrupt Status	Interrupt Status	nterrupt Status	Interrupt Status
				Ch_n	Ch_n	Ch_n	Ch_n
				RUR	RUR	RUR	RUR



Table 32: Source Level Interrupt Status Register - Channel n Address Location = 0xm2 (n = [0:11] & m=0-5 & 8-D)

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 4	Reserved		
3	Change of FL Condition Interrupt Status	RUR	Change of FL (FIFO Limit Alarm) Condition Interrupt Status - Ch n: This RESET-upon-READ bit-field indicates whether or not the Change of FL Condition Interrupt (for Channel n) has occurred since the last read of this register. 0 - Indicates that the Change of FL Condition Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Change of FL Condition Interrupt has occurred since the last read of this register. Note: The user can determine the current state of the FIFO Alarm condition by reading out the contents of Bit 3 (FL Alarm Declared) within the Alarm Status Register.(n)
2	Change of LOL Condition Interrupt Status	RUR	Change of Receive LOL (Loss of Lock) Condition Interrupt Status - Ch n: This RESET-upon-READ bit-field indicates whether or not the Change of Receive LOL Condition Interrupt (for Channel n) has occurred since the last read of this register. 0 - Indicates that the Change of Receive LOL Condition Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Change of Receive LOL Condition Interrupt has occurred since the last read of this register. Note: The user can determine the current state of the Receive LOL Defect condition by reading out the contents of Bit 2 (Receive LOL Defect Declared) within the Alarm Status Register.(n)
1	Change of LOS Condition Interrupt Status	RUR	Change of Receive LOS (Loss of Signal) Defect Condition Interrupt Status: Ch_n This RESET-upon-READ bit-field indicates whether or not the Change of the Receive LOS Defect Condition Interrupt (for Channel n) has occurred since the last read of this register. 0 - Indicates that the Change of the Receive LOS Defect Condition Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Change of the Receive LOS Defect Condition Interrupt has occurred since the last read of this register. Note: The user can determine the current state of the Receive LOS Defect condition by reading out the contents of Bit 1 (Receive LOS Defect Declared) within the Alarm Status Register.(n)
0	Change of DMO Condition Interrupt Status	RUR	Change of Transmit DMO (Drive Monitor Output) Condition Interrupt Status - Ch n: This RESET-upon-READ bit-field indicates whether or not the Change of the Transmit DMO Condition Interrupt (for Channel n) has occurred since the last read of this register. 0 - Indicates that the Change of the Transmit DMO Condition Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Change of the Transmit DMO Condition Interrupt has occurred since the last read of this register. Note: The user can determine the current state of the Transmit DMO Condition by reading out the contents of Bit 0 (Transmit DMO Condition) within the Alarm Status Register.(n)

TABLE 33: XRT75R12 REGISTER MAP SHOWING ALARM STATUS REGISTERS (AS_n)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Reserved	Loss of PRBS Pattern Sync	Digital LOS Defect Declared	Analog LOS Defect Declared	FL (FIFO Limit) Alarm Declared	Receive LOL Defect Declared	Receive LOS Defect Declared	Transmit DMO Condition
	R/O	R/O	R/O	R/O	R/O	R/O	R/O

Table 34: Alarm Status Register - Channel n Address Location = 0xm3 (n = [0:11] & m=0-5 & 8-D)

BIT NUMBER	NAME	Түре	DESCRIPTION
7	Reserved		
6	Loss of PRBS Pattern Lock	R/O	Loss of PRBS Pattern Lock Indicator: This READ-ONLY bit-field indicates whether or not the PRBS Receiver (within the Receive Section of Channel n) is declaring PRBS Lock within the incoming PRBS pattern. If the PRBS Receiver detects a very large number of bit-errors within its incoming data-stream, then it will declare the Loss of PRBS Lock Condition. Conversely, if the PRBS Receiver were to detect its pre-determined PRBS pattern with the incoming DS3, E3 or STS-1 data-stream, (with little or no bit errors) then the PRBS Receiver will clear the Loss of PRBS Lock condition. 0 - Indicates that the PRBS Receiver is currently declaring the PRBS Lock condition within the incoming DS3, E3 or STS-1 data-stream. 1 - Indicates that the PRBS Receiver is currently declaring the Loss of PRBS Lock condition within the incoming DS3, E3 or STs-1 data-stream. Note: This register bit is only valid if all of the following are true. a. The PRBS Generator block (within the Transmit Section of the Chip is enabled). b. The PRBS Receiver is enabled. c. The PRBS Pattern (that is generated by the PRBS Generator) is somehow looped back into the Receive Path (via the Line-Side) and

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TABLE 34: ALARM STATUS REGISTER - CHANNEL n ADDRESS LOCATION = 0xm3 (n = [0:11] & M= 0-5 & 8-D)

BIT NUMBER	NAME	Түре	DESCRIPTION	
5	Digital LOS Defect Declared	R/O	Digital LOS Defect Declared: This READ-ONLY bit-field indicates whether or not the Digital LOS (Los Signal) detector is declaring the LOS Defect condition. For DS3 and STS-1 applications, the Digital LOS Detector will declare LOS Defect condition whenever it detects an absence of pulses (within incoming DS3 or STS-1 data-stream) for 160 consecutive bit-periods. Further, (again for DS3 and STS-1 applications) the Digital LOS Detect will clear the LOS Defect condition whenever it determines that the pulsedensity (within the incoming DS3 or STS-1 signal) is at least 33%. 0 - Indicates that the Digital LOS Detector is NOT declaring the LOS Decondition. 1 - Indicates that the Digital LOS Detector is currently declaring the LO Defect condition. NOTES:	
			 LOS Detection (within each channel of the XRT75R12) is performed by both an Analog LOS Detector and a Digital LOS Detector. The LOS state of a given Channel is simply a WIRED-OR of the LOS Defect Declare states of these two detectors. The current LOS Defect Condition (for the channel) can be determined by reading out the contents of Bit 1 (Receive LOS Defect Declared) within this register. 	
4	Analog LOS Defect Declared	R/O	Analog LOS Defect Declared: This READ-ONLY bit-field indicates whether or not the Analog LOS (Loss of Signal) detector is declaring the LOS Defect condition. For DS3 and STS-1 applications, the Analog LOS Detector will declare the LOS Defect condition whenever it determines that the amplitude of the pulses (within the incoming DS3/STS-1 line signal) drops below a certain Analog LOS Defect Declaration threshold level. Conversely, (again for DS3 and STS-1 applications) the Analog LOS Detector will clear the LOS Defect condition whenever it determines that the amplitude of the pulses (within the incoming DS3/STS-1 line signal) has risen above a certain Analog LOS Defect Clearance threshold level. It should be noted that, in order to prevent "chattering" within the Analog LOS Detector output, there is some built-in hysteresis between the Analog LOS Defect Declaration and the Analog LOS Defect Clearance threshold levels. 0 - Indicates that the Analog LOS Detector is NOT declaring the LOS Defect Condition. 1 - Indicates that the Analog LOS Detector is currently declaring the LOS Defect condition. Notes: 1. LOS Detection (within each channel of the XRT75R12) is performed by both an Analog LOS Detector and a Digital LOS Detector. The LOS state of a given Channel is simply a WIRED-OR of the LOS Defect Declare states of these two detectors. 2. The current LOS Defect Condition (for the channel) can be determined by reading out the contents of Bit 1 (Receive LOS Defect Declared) within this register.	

TWELVE CHANNEL E3/DS3/STS-1 LINE INTERFACE UNIT WITH JITTER ATTENUATOR

REV. 1.0.4

Table 34: Alarm Status Register - Channel n Address Location = 0xm3 (n = [0:11] & m= 0-5 & 8-D)

BIT NUMBER	NAME	Түре	DESCRIPTION
3	FL Alarm Declared	R/O	FL (FIFO Limit) Alarm Declared: This READ-ONLY bit-field indicates whether or not the Jitter Attenuator block (within Channel_n) is currently declaring the FIFO Limit Alarm. The Jitter Attenuator block will declare the FIFO Limit Alarm anytime the Jitter Attenuator FIFO comes within two bit-periods of either overflowing or under-running. Conversely, the Jitter Attenuator block will clear the FIFO Limit Alarm anytime the Jitter Attenuator FIFO is NO longer within two bit-periods of either overflowing or under-running. Typically, this Alarm will only be declared whenever there is a very serious problem with timing or jitter in the system. 0 - Indicates that the Jitter Attenuator block (within Channel_n) is NOT currently declaring the FIFO Limit Alarm condition. 1 - Indicates that the Jitter Attenuator block (within Channel_n) is currently declaring the FIFO Limit Alarm condition. Note: This bit-field is only active if the Jitter Attenuator (within Channel_n) has been enabled.
2	Receive LOL Condition Declared	R/O	Receive LOL (Loss of Lock) Condition Declared: This READ-ONLY bit-field indicates whether or not the Receive Section (within Channel_n) is currently declaring the LOL (Loss of Lock) condition. The Receive Section (of Channel_n) will declare the LOL Condition, if the frequency of the Recovered Clock signal differs from that of the reference clock programmed for that channel (from the appropriate oscillator or the SFM clock synthesizer if in that mode) by 0.5% (or 5000ppm) or more . 0 - Indicates that the Receive Section of Channel_n is NOT currently declaring the LOL Condition. 1 - Indicates that the Receive Section of Channel_n is currently declaring the LOL Condition and the recovered clock differs by more than 0.5%

TWELVE CHANNEL E3/DS3/STS-1 LINE INTERFACE UNIT WITH JITTER ATTENUATOR

Table 34: Alarm Status Register - Channel n Address Location = 0xm3 (n = [0:11] & m=0-5 & 8-D)

BIT NUMBER	NAME	TYPE	DESCRIPTION
1	Receive LOS Defect Condition Declared	R/O	 Receive LOS (Loss of Signal) Defect Condition Declared: This READ-ONLY bit-field indicates whether or not the Receive Section (within Channel_n) is currently declaring the LOS defect condition. The Receive Section (of Channel_n) will declare the LOS defect condition, if any one of the following conditions is met. If the Digital LOS Detector declares the LOS defect condition (for DS3 or STS-1 applications) If the Analog LOS Detector declares the LOS defect condition (for DS3 or STS-1 applications) If the ITU-T G.775 LOS Detector declares the LOS defect condition (for E3 applications). Indicates that the Receive Section of Channel_n is NOT currently declaring the LOS Defect Condition. Indicates that the Receive Section of Channel_n is currently declaring
0	Transmit DMO Condition Declared	R/O	Transmit DMO (Drive Monitor Output) Condition Declared: This READ-ONLY bit-field indicates whether or not the Transmit Section of Channel_n is currently declaring the DMO Alarm condition. As configured, the Transmit Section will either internally (via the TTIP_n and TRING_n) or externally (via the MTIP_n and MRING_n) check the Transmit Output DS3/E3/STS-1 Line signal for bipolar pulses. If the Transmit Section were to detect no bipolar for 128 consecutive bit-periods, then it will declare the Transmit DMO Alarm condition. This particular alarm can be used to check for fault conditions on the Transmit Output Line Signal path. The Transmit Section will clear the Transmit DMO Alarm condition upon detecting bipolar activity on the Transmit Output Line signal. 0 - Indicates that the Transmit Section of Channel_n is NOT currently declaring the Transmit DMO Alarm condition. 1 - Indicates that the Transmit Section of Channel_n is currently declaring the Transmit DMO Alarm condition.

TABLE 35: XRT75R12 REGISTER MAP SHOWING TRANSMIT CONTROL REGISTERS (TC_n)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Rese	erved	Internal Transmit Drive Monitor	Insert PRBS Error	Reserved	TAOS	TxCLKINV	TxLEV
		R/W	R/W		R/W	R/W	R/W

TABLE 36: TRANSMIT CONTROL REGISTER - CHANNEL n ADDRESS LOCATION = 0×4 (n = [0:11] & M= 0.5 & 8-D)

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 6	Reserved		
5	Internal Transmit Drive Monitor Enable	R/W	Internal Transmit Drive Monitor Enable - Channel_n: This READ/WRITE bit-field is used to configure the Transmit Section of Channel_n to either internally or externally monitor the TTIP_n and TRING_n output pins for bipolar pulses, in order to determine whether to declare the Transmit DMO Alarm condition. If the user configures the Transmit Section to externally monitor the TTIP_n and TRING_n output pins (for bipolar pulses) then the user must connect the MTIP_n and MRING_n input pins to their corresponding TTIP_n and TRING_n output pins (via a 270 ohm series resistor). If the user configures the Transmit Section to internally monitor the TTIP_n and TRING_n output pins (for bipolar pulses), the user does NOT need to conect the MTIP_n and MRING_n input pins. This monitoring will be performed internally at the TTIP_n and TRING_n pads. 0 - Configures the Transmit Drive Monitor to externally monitor the TTIP_n and TRING_n output pins for bipolar pulses. 1 - Configures the Transmit Drive Monitor to internally monitor the TTIP_n and TRING_n output pins for bipolar pulses.
4	Insert PRBS Error	R/W	Insert PRBS Error - Channel_n: A "0 to 1" transition within this bit-field causes the PRBS Generator (within the Transmit Section of Channel_n) to generate a single bit error within the outbound PRBS pattern-stream. Notes: 1. This bit-field is only active if the PRBS Generator and Receiver have been enabled within the corresponding Channel. 2. After writing the "1" into this register, the user must execute a write operation to clear this particular register bit to "0" in order to facilitate the next "0 to 1" transition in this bit-field.
3	Reserved		

TWELVE CHANNEL E3/DS3/STS-1 LINE INTERFACE UNIT WITH JITTER ATTENUATOR

Table 36: Transmit Control Register - Channel n Address Location = 0xm4 (n = [0:11] & m= 0-5 & 8-D)

BIT NUMBER	NAME	Түре	DESCRIPTION
2	TAOS	R/W	Transmit All OneS Pattern - Channel_n: This READ/WRITE bit-field is used to command the Transmit Section of Channel_n to generate and transmit an unframed, All Ones pattern via the DS3, E3 or STS-1 line signal (to the remote terminal equipment). Whenever the user implements this configuration setting, the Transmit Section will ignore the data that it is accepting from the System-side equipment and output the "All Ones" Pattern. 0 - Configures the Transmit Section to transmit the data that it accepts from the System-side Interface. 1 - Configures the Transmit Section to generate and transmit the Unframed, All Ones pattern.
1	TxCLKINV	R/W	Transmit Clock Invert Select - Channel_n: This READ/WRITE bit-field is used to select the edge of the TxCLK_n input that the Transmit Section of Channel_n will use to sample the TxPOS_n and TxNEG_n input pins, as described below. 0 - Configures the Transmit Section (within the corresponding channel) to sample the TxPOS_n and TxNEG_n input pins upon the falling edge of TxCLK_n. 1 - Configures the Transmit Section (within the corresponding channel) to sample the TxPOS_n and TxNEG_n input pins upon the rising edge of TxCLK_n. Note: This is done on a per-channel basis.
0	TxLEV	R/W	Transmit Line Build-Out Select - Channel_n: This READ/WRITE bit-field is used to enable or disable the Transmit Line Build-Out (e.g., pulse-shaping) circuit within the corresponding channel. The user should set this bit-field to either "0" or to "1" based upon the following guidelines. 0 - If the cable length between the Transmit Output (of the corresponding Channel) and the DSX-3/STSX-1 location is 225 feet or less. 1 - If the cable length between the Transmit Output (of the corresponding Channel) and the DSX-3/STSX-1 location is more than 225 feet . The user must follow these guidelines in order to insure that the Transmit Section (of Channel_n) will always generate a DS3 pulse that complies with the Isolated Pulse Template requirements per Bellcore GR-499-CORE, or an STS-1 pulse that complies with the Pulse Template requirements per Telcordia GR-253-CORE. Note: This bit-field is ignored if the channel has been configured to operate in the E3 Mode.

TABLE 37: XRT75R12 REGISTER MAP SHOWING RECEIVE CONTROL REGISTERS (RC_n)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Rese	erved	Disable DLOS Detector	Disable ALOS Detector	RxCLKINV	LOSMUT Enable	Receive Monitor Mode Enable	Receive Equalizer Enable
		R/W	R/W	R/W	R/W	R/W	R/W

TABLE 38: RECEIVE CONTROL REGISTER - CHANNEL n ADDRESS LOCATION = 0×5 (n = [0:11] & M= 0.5 & 8-D)

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 6	Reserved		
5	Disable DLOS Detector	R/W	Disable Digital LOS Detector - Channel_n: This READ/WRITE bit-field is used to enable or disable the Digital LOS (Loss of Signal) Detector within Channel_n, as described below. 0 - Enables the Digital LOS Detector within Channel_n. 1 - Disables the Digital LOS Detector within Channel_n. Note: This bit-field is only active if Channel_n has been configured to operate in the DS3 or STS-1 Modes.
4	Disable ALOS Detector	R/W	Disable Analog LOS Detector - Channel_n: This READ/WRITE bit-field is used to either enable or disable the Analog LOS (Loss of Signal) Detector within Channel_n, as described below. 0 - Enables the Analog LOS Detector within Channel_n. 1 - Disables the Analog LOS Detector within Channel_n. Note: This bit-field is only active if Channel_n has been configured to operate in the DS3 or STS-1 Modes.
3	RxCLKINV	R/W	Receive Clock Invert Select - Channel_n: This READ/WRITE bit-field is used to select the edge of the RxCLK_n output that the Receive Section of Channel_n will use to output the recovered data via the RxPOS_n and RxNEG_n output pins, as described below. 0 - Configures the Receive Section (within the corresponding channel) to output the recovered data via the RxPOS_n and RxNEG_n output pins upon the rising edge of RCLK_n. 1 - Configures the Receive Section (within the corresponding channel) to output the recovered data via the RxPOS_n and RxNEG_n output pins upon the falling edge of RCLK_n.

TWELVE CHANNEL E3/DS3/STS-1 LINE INTERFACE UNIT WITH JITTER ATTENUATOR

Table 38: Receive Control Register - Channel n Address Location = 0xm5 (n = [0:11] & m=0-5 & 8-D)

BIT NUMBER	NAME	Түре	DESCRIPTION
2	LOSMUT Enable	R/W	Muting upon LOS Enable - Channel_n: This READ/WRITE bit-field is used to configure the Receive Section (within Channel_n) to automatically pull their corresponding Recovered Data Output pins (e.g., RxPOS_n and RxNEG_n) to GND for the duration that the Receive Section declares the LOS defect condition. In other words, this feature (if enabled) will cause the Receive Channel to automatically mute the Recovered data anytime the Receive Section declares the LOS defect condition. 0 - Disables the Muting upon LOS feature. In this setting the Receive Section will NOT automatically mute the Recovered Data whenever it is declaring the LOS defect condition. 1 - Enables the Muting upon LOS feature. In this setting the Receive Section will automatically mute the Recovered Data whenever it is declaring the LOS defect condition.
1	Receive Monitor Mode Enable	R/W	Receive Monitor Mode Enable - Channel_n: This READ/WRITE bit-field is used to configure the Receive Section of Channel_n to operate in the Receive Monitor Mode. If the user configures the Receive Section to operate in the Receive Monitor Mode, then it will be able to receive a nominal DSX-3/STSX-1 signal that has been attenuated by 20dB of flat loss along with 6dB of cable loss, in an error-free manner. However, internal LOS circuitry is suppressed and LOS will never assert nor LOS be declared when operating under this mode. 0 - Configures the corresponding channel to operate in the Normal Mode. 1 - Configure the corresponding channel to operate in the Receive Monitor Mode.
0	Receive Equalizer Enable	R/W	Receive Equalizer Enable - Channel_n: This READ/WRITE register bit is used to enable or disable the Receive Equalizer block within the Receive Section of Channel_n, as listed below. 0 - Disables the Receive Equalizer within the corresponding channel. 1 - Enables the Receive Equalizer within the corresponding channel. Note: For virtually all applications, we recommend that the user set this bit-field to "1" (for all channels) and enable the Receive Equalizer.



TABLE 39: XRT75R12 REGISTER MAP SHOWING CHANNEL CONTROL REGISTERS (CC_n)

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Reserved		PRBS Enable Ch_n	RLB_n	LLB_n	E3_n	STS-1/DS3_n	SR/DR_n
		R/W	R/W	R/W	R/W	R/W	R/W

Table 40: Channel Control Register - Channel n Address Location = 0xm6 (n = [0:11] & m= 0-5 & 8-D)

BIT NUMBER	NAME	Түре	DESCRIPTION
7 - 6	Reserved		
5	PRBS Enable	R/W	PRBS Generator and Receiver Enable - Channel_n: This READ/WRITE bit-field is used to enable or disable the PRBS Generator and Receiver within a given Channel of the XRT75R12. If the user enables the PRBS Generator and Receiver, then the following will happen. 1. The PRBS Generator (which resides within the Transmit Section of the Channel) will begin to generate an unframed, 2^15-1 PRBS Pattern (for DS3 and STS-1 applications) and an unframed, 2^23-1 PRBS Pattern (for E3 applications). 2. The PRBS Receiver (which resides within the Receive Section of the Channel) will now be enabled and will begin to search the incoming data for the above-mentioned PRBS patterns. 0 - Disables both the PRBS Generator and PRBS Receiver within the corresponding channel. 1 - Enables both the PRBS Generator and PRBS Receiver within the corresponding channel.
			 Notes: To check and monitor PRBS Bit Errors, DR (Dual Rail) mode will be over-ridden and Single Rail mode forced for the duration of this mode. This will configure the RNEG/LCV_n output pin to function as a PRBS Error Indicator. All errors will be flagged on this pin. The errors will also be accumulated in the 16 bit Error counter for the channel. If the user enables the PRBS Generator and PRBS Receiver, the Channel will ignore the data that is being accepted from the System-side Equipment (via the TxPOS_n and TxNEG_n input pins) and will overwrite this outbound data with the PRBS Pattern. The system must provide an accurate and stable data-rate clock to the TxClk_n pin during this operation.

TWELVE CHANNEL E3/DS3/STS-1 LINE INTERFACE UNIT WITH JITTER ATTENUATOR

Table 40: Channel Control Register - Channel n Address Location = 0xm6 (n = [0:11] & m = 0.5 & 8-D)

BIT NUMBER	NAME	Түре				DESCRIPTION	
4	RLB_n	R/W	Loop-Back Select - RLB Bit - Channel_n: This READ/WRITE bit-field along with the corresponding LLB_n bit-field is used to configure a given channel into various loop-back modes ass shown by the following table.				
			LLB_n RLB_n Loop-back Mode				
			0 0 Normal (No Loop-back) Mode				
				0	1	Remote Loop-back Mode	
				1	0	Analog Local Loop-back Mode	
				1	1	Digital Local Loop-back Mode	
3	LLB_n	R/W	Loop-Back Select - LLB Bit-field - Channel_n: See the table (above) for RLB_n.				
2	E3_n	R/W	E3 Mode Select - Channel_n: This READ/WRITE bit-field, along with Bit 1 (STS-1/DS3_n) within this register, is used to configure a given channel into either the DS3, E3 or STS-1 Modes. 0 - Configures Channel_n to operate in either the DS3 or STS-1 Modes, depending upon the state of Bit 1 (STS-1/DS3_n) within this same register. 1- Configures Channel_n to operate in the E3 Mode.				

TWELVE CHANNEL E3/DS3/STS-1 LINE INTERFACE UNIT WITH JITTER ATTENUATOR

REV. 1.0.4

Table 40: Channel Control Register - Channel n Address Location = 0xm6 (n = [0:11] & m=0-5 & 8-D)

BIT NUMBER	NAME	Түре	DESCRIPTION
1	STS-1/DS3_n	R/W	STS-1/DS3 Mode Select - Channel_n: This READ/WRITE bit-field, along with Bit 2 (E3_n) is used to configure a given channel into either the DS3, E3 or STS-1 Modes. This bit-field is ignored if Bit 2 (E3_n) has been set to "1". If Bit 2 (E3_n) is a 0: 0 - Configures Channel_n to operate in the DS3 Mode. 1 - Configures Channel_n to operate in the STS-1 Mode.
0	SR/DR_n	R/W	Single-Rail/Dual-Rail Select - Channel_n: This READ/WRITE bit-field is used to configure Channel_n to operate in either the Single-Rail or Dual-Rail Mode. If the user configures the Channel to operate in the Single-Rail Mode, the following will happen. • The B3ZS/HDB3 Encoder and Decoder blocks (within Channel_n) will be enabled. • The Transmit Section of Channel_n will accept all of the outbound data (from the System-side Equipment) via the TxPOS_n input pin. • The Receive Section of each channel will output all of the recovered data (to the System-side Equipment) via the RxPOS_n output pin. • The corresponding RNEG/LCV_n output pin will now function as the LCV (Line Code Violation or Excessive Zero Event) indicator output pin for Channel_n. If the user configures Channel_n to operate in the Dual-Rail Mode, the following will happen. • The B3ZS/HDB3 Encoder and Decoder blocks of Channel_n will be disabled. • The Transmit Section of Channel_n will be configured to accept positive-polarity data via the TxPOS_n input pin and negative-polarity data via the TxNEG_n input pin. • The Receive Section of Channel_n will pulse the RxPOS_n output pin "High" (for one period of RCLK_n) for each time a positive-polarity pulse is received via the RTIP_n/RRING_n input pins. Likewise, the Receive Section of each channel will pulse the RxNEG_n output pin "High" (for one period of RxCLK_n) for each time a negative-polarity pulse is received via the RTIP_n/RRING_n input pins. 0 - Configures Channel_n to operate in the Dual-Rail Mode.

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TABLE 41: XRT75R12 REGISTER MAP SHOWING JITTER ATTENUATOR CONTROL REGISTERS (JA_n)

Віт 7	Віт 6	BIT 6 BIT 5 BIT 4		Віт 3	Віт 2	Віт 1	Віт 0
	Rese	erved		JA RESET Ch_n	JA1 Ch_n	JA in Tx Path Ch_n	JA0 Ch_n
				R/W	R/W	R/W	R/W

TABLE 42: JITTER ATTENUATOR CONTROL REGISTER - CHANNEL n ADDRESS LOCATION = 0xm7 (n = [0:11] & m= 0-5 & 8-D)

BIT NUMBER	NAME	Түре				DESCRIPTION	_			
7 - 4	Reserved									
3	JA RESET Ch_n	R/W	Writing a "(Attenuator Whenever occur. The REA be reset The cont NOTE: The	Attenuator RESET - Channel_n: g a "0 to 1" transition within this bit-field will configure the Jitter lator (within Channel_n) to execute a RESET operation. ever the user executes a RESET operation, then following will READ and WRITE pointers (within the Jitter Attenuator FIFO) we seet to their default values. contents of the Jitter Attenuator FIFO will be flushed. The user must follow up any "0 to 1" transition with appropriate write operate to set this bit-field back to "0", in ord to resume normal operation with the Jitter Attenuator.						
2	JA1 Ch_n	R/W	, , , , , , , , , , , , , , , , , , ,							
				JA0	JA1	Jitter Attenuator Mode				
				0 0 FIFO Depth = 16 bits						
				0 1 FIFO Depth = 32 bits						
				1	0	Disabled				
				1	1	Disabled				

TWELVE CHANNEL E3/DS3/STS-1 LINE INTERFACE UNIT WITH JITTER ATTENUATOR

REV 104

Table 42: JITTER ATTENUATOR CONTROL REGISTER - CHANNEL n Address Location = 0xm7 (n = [0:11] & m= 0-5 & 8-D)

BIT NUMBER	NAME	Түре	DESCRIPTION
1	JA in Tx Path Ch_n	R/W	Jitter Attenuator in Transmit/Receive Path Select Bit: This input pin is used to configure the Jitter Attenuator (within Channel_n) to operate in either the Transmit or Receive path, as described below. 0 - Configures the Jitter Attenuator (within Channel_n) to operate in the Receive Path. 1 - Configures the Jitter Attenuator (within Channel_n) to operate in the Transmit Path.
0	JA0 Ch_n	R/W	Jitter Attenuator Configuration Select Input - Bit 0: See the description for Bit 2 (JA1 Ch_n).

TABLE 43: XRT75R12 REGISTER MAP SHOWING ERROR COUNTER MSBYTE REGISTERS (EM_N)

Address Location	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	E	F
0x0-	APST	IER0	ISR0	AS0	TC0	RC0	CC0	JA0	APSR		EM0	EL0	EH0			•
0x1-		IER1	ISR1	AS1	TC1	RC1	CC1	JA1			EM1	EL1	EH1			•
0x2-		IER2	ISR2	AS2	TC2	RC2	CC2	JA2			EM2	EL2	EH2			
0x3-		IER3	ISR3	AS3	TC3	RC3	CC3	JA3			ЕМ3	EL3	EH3			
0x4-		IER4	ISR4	AS4	TC4	RC4	CC4	JA4			EM4	EL4	EH4			
0x5-		IER5	ISR5	AS5	TC5	RC5	CC5	JA5			EM5	EL5	EH5			
0x6-	CIE	CIS													PN	VN
0x7-																
0x8-	APST	IER6	ISR6	AS6	TC6	RC6	CC6	JA6	APSR		EM6	EL6	EH6			
0x9-		IER7	ISR7	AS7	TC7	RC7	CC7	JA7			EM7	EL7	EH7			
0xA-		IER8	ISR8	AS8	TC8	RC8	CC8	JA8			EM8	EL8	EH8			
0xB-		IER9	ISR9	AS9	TC9	RC9	CC9	JA9			EM9	EL9	EH9			
0xC-		IER10	ISR10	AS10	TC10	RC10	CC10	JA10			EM10	EL10	EH10			
0xD-		IER11	ISR11	AS11	TC11	RC11	CC11	JA11			EM11	EL11	EH11			
0xE-	CIE	CIS														
0xF-																

TABLE 44: ERROR COUNTER MSBYTE REGISTER - CHANNEL N ADDRESS LOCATION = 0xmA

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Msb							9th bit
R/W							

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TABLE 45: XRT75R12 REGISTER MAP SHOWING ERROR COUNTER LSBYTE REGISTERS (EL_N)

Address Location	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	E	F
0x0-	APST	IER0	ISR0	AS0	TC0	RC0	CC0	JA0	APSR		EM0	EL0	EH0			
0x1-		IER1	ISR1	AS1	TC1	RC1	CC1	JA1			EM1	EL1	EH1			
0x2-		IER2	ISR2	AS2	TC2	RC2	CC2	JA2			EM2	EL2	EH2			
0x3-		IER3	ISR3	AS3	TC3	RC3	CC3	JA3			ЕМ3	EL3	EH3			
0x4-		IER4	ISR4	AS4	TC4	RC4	CC4	JA4			EM4	EL4	EH4			
0x5-		IER5	ISR5	AS5	TC5	RC5	CC5	JA5			EM5	EL5	EH5			
0x6-	CIE	CIS													PN	٧N
0x7-																
0x8-	APST	IER6	ISR6	AS6	TC6	RC6	CC6	JA6	APSR		EM6	EL6	EH6			
0x9-		IER7	ISR7	AS7	TC7	RC7	CC7	JA7			EM7	EL7	EH7			
0xA-		IER8	ISR8	AS8	TC8	RC8	CC8	JA8			EM8	EL8	EH8			
0xB-		IER9	ISR9	AS9	TC9	RC9	CC9	JA9			EM9	EL9	EH9			
0xC-		IER10	ISR10	AS10	TC10	RC10	CC10	JA10			EM10	EL10	EH10			
0xD-		IER11	ISR11	AS11	TC11	RC11	CC11	JA11			EM11	EL11	EH11			
0xE-	CIE	CIS														
0xF-																

TABLE 46: ERROR COUNTER LSBYTE REGISTER - CHANNEL N ADDRESS LOCATION = 0xmB

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
8th bit							Ls bit
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

TABLE 47: XRT75R12 REGISTER MAP SHOWING ERROR COUNTER HOLDING REGISTERS (EH_N)

Address Location	0	1	2	3	4	5	6	7	8	9	Α	В	С	D	Е	F
0x0-	APST	IER0	ISR0	AS0	TC0	RC0	CC0	JA0	APSR		EM0	EL0	EH0			
0x1-		IER1	ISR1	AS1	TC1	RC1	CC1	JA1			EM1	EL1	EH1			
0x2-		IER2	ISR2	AS2	TC2	RC2	CC2	JA2			EM2	EL2	EH2			
0x3-		IER3	ISR3	AS3	TC3	RC3	CC3	JA3			ЕМ3	EL3	EH3			
0x4-		IER4	ISR4	AS4	TC4	RC4	CC4	JA4			EM4	EL4	EH4			
0x5-		IER5	ISR5	AS5	TC5	RC5	CC5	JA5			EM5	EL5	EH5			
0x6-	CIE	CIS													PN	VN
0x7-																
0x8-	APST	IER6	ISR6	AS6	TC6	RC6	CC6	JA6	APSR		EM6	EL6	EH6			
0x9-		IER7	ISR7	AS7	TC7	RC7	CC7	JA7			EM7	EL7	EH7			
0xA-		IER8	ISR8	AS8	TC8	RC8	CC8	JA8			EM8	EL8	EH8			
0xB-		IER9	ISR9	AS9	TC9	RC9	CC9	JA9			EM9	EL9	EH9			
0xC-		IER10	ISR10	AS10	TC10	RC10	CC10	JA10			EM10	EL10	EH10			
0xD-		IER11	ISR11	AS11	TC11	RC11	CC11	JA11			EM11	EL11	EH11			
0xE-	CIE	CIS														
0xF-																

TABLE 48: ERROR COUNTER HOLDING REGISTER - CHANNEL N ADDRESS LOCATION = 0XMC

Віт 7	Віт 6	Віт 5	Віт 4	Віт 3	Віт 2	Віт 1	Віт 0
Msb							Ls bit
R/W							

Each channel contains a dedicated 16 bit PRBS error counter. When enabled this counter will accumulate PRBS errors (as well as excess zeros and LCVs). The LS byte will "carry" a one over to the MS byte each time it rolls over from 255 to zero until the MS byte also reaches 255. When both counters reach 255, no further errors will be accumulated and "all ones" will signify an overflow condition.

The counter can be read while in the active count mode. Either register may be read "on the fly" and the other byte will be simultaneously transferred into the channel's Error Holding register. The holding register may then be read to supply the Host with a correct 16 bit count (as of the instant of reading). With this mechanism, the Host could rapidly cycle thru reading all twelve counters in order (storing the read byte in scratch RAM) and then come back and read the second byte from each holding register to form the 16 bit accumulation in the Host system.

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8.0 ELECTRICAL CHARACTERISTICS

TABLE 49: ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN	MAX	UNITS	COMMENTS
V_{DD}	Supply Voltage	-0.5	6.0	V	Note 1
V _{IN}	Input Voltage at any Pin	-0.5	5.5	V	Note 1
I _{IN}	Input current at any pin		100	mA	Note 1
S _{TEMP}	Storage Temperature	-65	150	0C	Note 1
A _{TEMP}	Ambient Operating Temperature	-40	85	0C	Industrial Temp Grade
Theta JA	Thermal Resistance: Junction-to-Ambient		7.5	⁰ C/W	linear air flow 200ft/min (See Note 3 below)
Theta JC	Thermal Resistance: Junction-to-Case		0.5	⁰ C/W	All conditions
M _{LEVL}	Exposure to Moisture	5		level	EIA/JEDEC JESD22-A112-A
ESD	ESD Rating	2000		V	Note 2

Notes:

- 1. Exposure to or operating near the Min or Max values for extended period may cause permanent failure and impair reliability of the device.
- 2. ESD testing method is per MIL-STD-883D,M-3015.7
- 3. Linear Air flow of 200 ft/min recommended for Industrial Applications. Theta JA = 9.4 C/W with 0 Lft/min, Theta JA = 7.1 ℃/W with 400Lft/min.

TABLE 50: DC ELECTRICAL CHARACTERISTICS:

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
DV_DD	Digital Supply Voltage	3.135	3.3	3.465	V
AV_DD	Analog Supply Voltage	3.135	3.3	3.465	V
I _{CC_DS3}	DS3 current consumption using PRBS 2 ²³ -1 pattern ³		1016	1117	mA
I _{CC_DS3JA}	DS3 current consumption using PRBS 2 ²³ -1 pattern ⁴		1172	1290	mA
I _{CC_E3}	E3 current consumption using PRBS 2 ²³ -1 pattern ³		1040	1140	mA
I _{CC_E3JA}	E3 current consumption using PRBS 2 ²³ -1 pattern ⁴		1180	1300	mA
I _{CC_STS1}	STS1 current consumption using PRBS 2 ²³ -1 pattern ³		1100	1210	mA
I _{CC_STS1JA}	STS1 current consumption using PRBS 2 ²³ -1 pattern ⁴		1300	1430	mA
P _{CC_DS3}	DS3 Power Consumption ⁵		3.35	3.87	W
P _{CC_DS3JA}	DS3 Power Consumption with Jitter Attenuator Enabled ⁵		3.87	4.47	W
P _{CC_E3}	E3 Power Consumption ⁵		3.43	3.95	W
P _{CC_E3JA}	E3 Power Consumption with Jitter Attenuator Enabled ⁵		3.89	4.50	W

XRT75R12

TWELVE CHANNEL E3/DS3/STS-1 LINE INTERFACE UNIT WITH JITTER ATTENUATOR

REV. 1.0.4

TABLE 50: DC ELECTRICAL CHARACTERISTICS:

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
P _{CC_STS1}	STS1 Power Consumption ⁵		3.63	4.19	W
P _{CC_STS1JA}	STS1 Power Consumption with Jitter Attenuator Enabled ⁵		4.29	4.95	W
V _{IL}	Input Low Voltage ²			0.8	V
V _{IH}	Input High Voltage ² 2.0			5.5	V
V _{OL}	Output Low Voltage, I _{OUT} = - 4mA			0.4	V
V _{OH}	Output High Voltage, I _{OUT} = 4 mA	2.4			V
Ι _L	Input Leakage Current ¹			±10	μΑ
C _I	Input Capacitance			10	pF
C_{L}	Load Capacitance			10	pF

Notes:

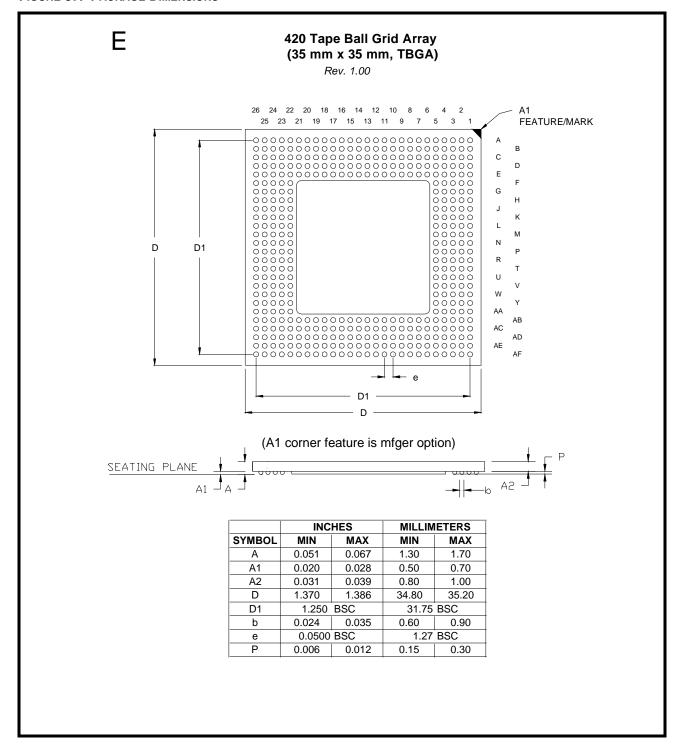
- 1. Not applicable for pins with pull-up or pull-down resistors.
- 2. The Digital inputs are TTL 5V compliant.
- 3. With Jitter Attenuator Disabled.
- 4. With Jitter Attenuator Enabled.
- 5. These values are **not** a measure of Power Dissipation. These values represent the Total Power Consumption. i.e. $P_{CC \ Consumption} = P_{DD \ Dissipation} + P_{LD \ Delivered \ to \ Load}$



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT75R12IB	420 TBGA	-40°C to +85°C

FIGURE 37. PACKAGE DIMENSIONS



REVISION HISTORY

REVISION	DATE	COMMENTS
1.0.0	05/10/05	Final Release Version of XRT75R12 datasheet.
1.0.1	April 2006	1.Added current and power consumption on Table 50, "DC Electrical Characteristics:," on page 84.
		2. Revised Receive Monitor Enable Bit functional description and Section 3.3.1 description.
		3. Updated Table 3, "The ALOS (Analog LOS) Declaration and Clearance Thresholds for a given setting of REQEN (DS3 and STS-1 Applications)," on page 23.
		4. Minor corrections on Transmitter Section of Features Summary on page 2.
		5. Minor typo corrections in STS1Clk/12M pin description and in Section 1.0, 3.3, and 4.5, Table 7 and Table 9.
		6. Added Table 2, "Reference Clock Performance Specifications," on page 19.
1.0.2	12/07/06	1.Corrected package thermal resistance specification.
1.0.3	6/11/07	Corrected global register 0x08 and added global registers 0x80 & 0x88.
		2. Added (N = [0:11] & M = 0-5 & 8-D) to channelized register titles.
1.0.4	10/26/07	1.Theta-jC thermal value added.

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