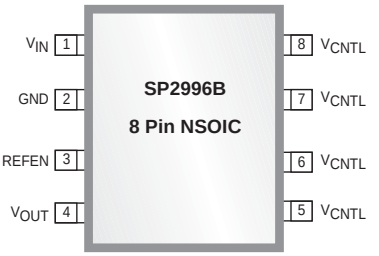
SP2996B

2 Amp DDR Bus Termination Regulator

FEATURES

- Capable of sourcing and sinking 2A Continuous current
- Supports both DDR1 ($1.25V_{TT}$) and DDR2 ($0.9V_{TT}$) requirements
- Low Output Voltage Offset, ± 20mV
- Thermal and Current Limit Protection
- Integrated Power MOSFETs
- Generates Termination for SSTL-2
- High Accuracy Output at Full Load
- Adjustable V_{OUT} by External Resistors
- Minimal External Components
- Available in 8 pin NSOIC package



Now Available in Lead Free Packaging

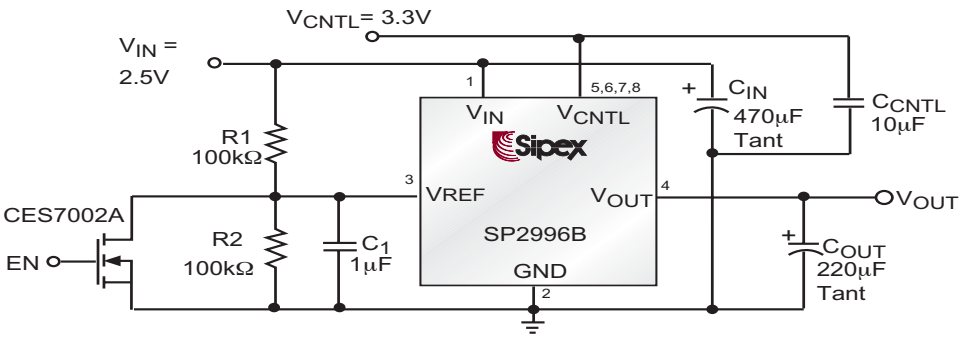
APPLICATIONS

- DDR Memory Termination
- Active Bus Termination
- Supply Splitter

DESCRIPTION

The SP2996B voltage regulator is designed to convert voltage supplies ranging from 1.6V to 6V into a desired output voltage which is adjusted by an external resistor divider. The regulator is capable of sourcing or sinking up to 2A of Continuous current while regulating an output voltage to within 20mV. The SP2996B provides an excellent voltage source for active termination schemes of high speed transmission lines such as those seen in high speed memory buses and distributed backplane designs when used in conjunction with series termination resistors. The voltage output of the regulator can be used as a termination voltage for DDR SDRAM, and it meets the JEDEC SSTL-2 and SSTL-3 specifications . Current limits in both sourcing and sinking mode, plus on-chip thermal shutdown make the circuit tolerant of output fault conditions.

TYPICAL APPLICATIONS CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... -0.4V to 7V
Operating Temperature Range.....-40°C to +85°C
Junction Temperature ....125°C
Storage Temperature Range.....-65°C to +150°C

ELECTRICAL CHARACTERISTICS

V_{IN} = 2.5V, V_{CTRL} = 3.3V, V_{REF} = 0.5V_{IN}, C_{OUT} = 10µF (Ceramic), T_A = 25ºC, unless otherwise specified. (Note 1)

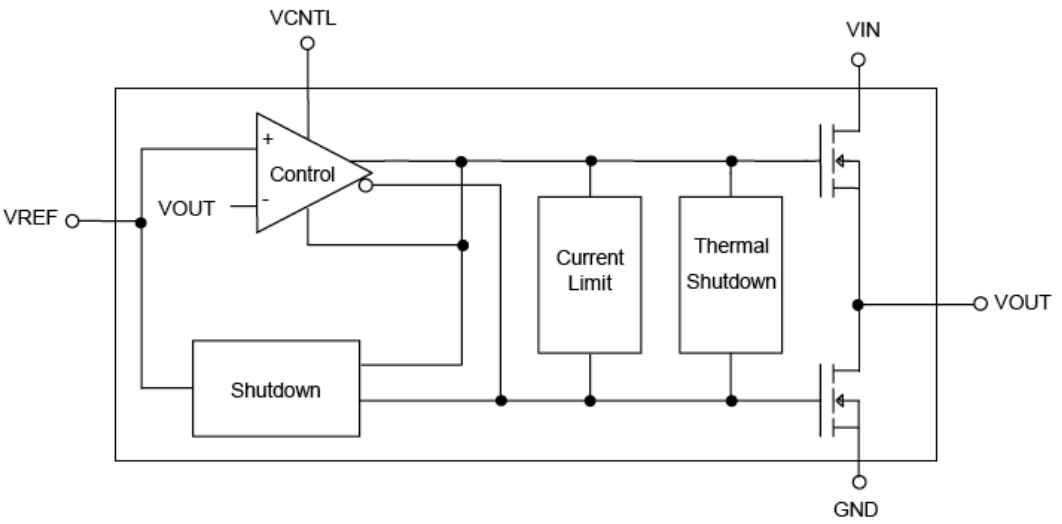
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input Voltage Range (DDR 1/2) (Note 5)	V_{IN}	Keep V_{CTRL} ≥ V_{IN} on operation power on and power off sequences	1.6	2.5/1.8	-	V
	V_{CNTL}	I_{OUT} = 0mA	3.0	3.3	6	
Output Voltage	V_{OUT}	I_{OUT} = 0mA		V_{REF}		V
Output Offset Voltage	V_{OS}	No Load	-20	-	20	mV
Load Regulation (DDR 1/2)	Δ V_{LOR}	I_{OUT} = 0.1mA to +2A	-	10	25	mV
		I_{OUT} = 0.1mA to -2A	-	10	25	
Quiescent Current	I_Q	V_{REF} < 0.2V, V_{OUT} = OFF	-	8	30	µA
Operating Current of V_{CNTL}	I_{CNTL}	No Load	-	3	10	mA
Bias Current of V_{REF}		V_{REF} = 1.25V	-	-	1	µA
Current Limit	I_{IL}	Note 4	2.2	3	4.5	A
Thermal Protection						
Thermal Shutdown Temperature (Note 5)	T_{SD}	3.3V ≤ V_{CNTL} ≤ 5V Guaranteed by design	125	150	-	ºC
Thermal Shutdown Hysteresis		Guaranteed by design	-	30	-	ºC
Shutdown Specifications						
Shutdown Threshold	$V_{TRIGGER}$	Output ON (V_{REF} = ZeroV ----->1 .25V)	0.8	-	-	V
Shutdown Threshold	$V_{TRIGGER}$	Output OFF (V_{REF} = 1.25V ----> ZeroV)	-	-	0.2	
Thermal Resistance	θJA			160		ºC/W
	θJC			40		

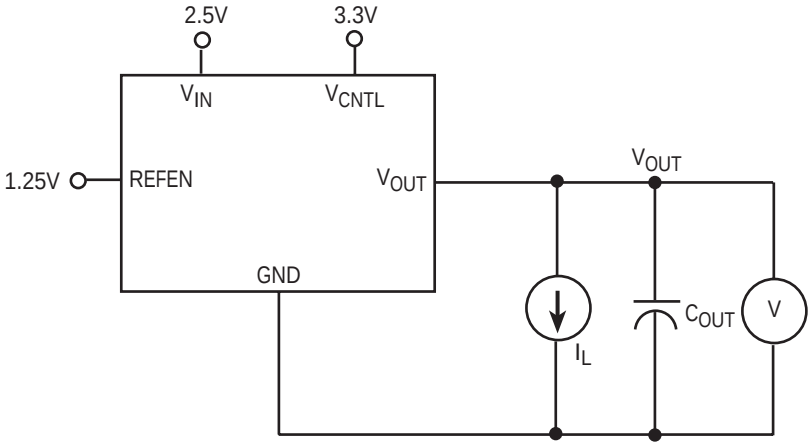
Note 1 . Specifications are tested for production at T_A = 25ºC . Specifications over the -40ºC to 85ºC operating temperature range are assured by design, characterization and correlation with Statistical Quality Controls (SQC).
Note 2. V_{OS} offset is the voltage measurement defined as V_{OUT} subtracted from V_{REF}.
Note 3. Load regulation is measured at constant junction temperature, using pulse testing with a low ON time.
Note 4. Current limit is measured by pulsing a short time.
Note 5. In order to safely operate your system, V_{CTRL} must be > V_{IN}.

PIN DESCRIPTIONS

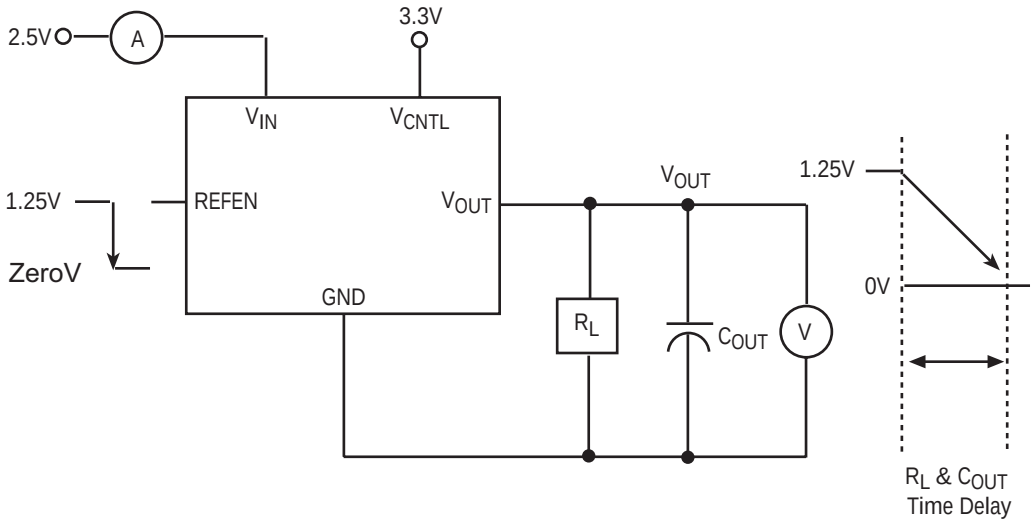
Pin Name	Pin Number	Description (8 pin NSOIC)
V_{IN}	1	Power Input Voltage
GND	2	Ground
REFEN	3	Reference Voltage Input
V_{OUT}	4	Output Voltage
V_{CNTL}	5	Voltage for the driver circuit and all analog blocks
V_{CNTL}	6	Voltage for the driver circuit and all analog blocks
V_{CNTL}	7	Voltage for the driver circuit and all analog blocks
V_{CNTL}	8	Voltage for the driver circuit and all analog blocks

BLOCK DIAGRAM

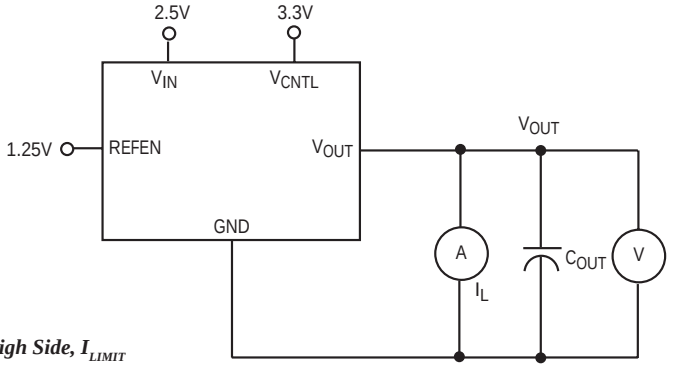




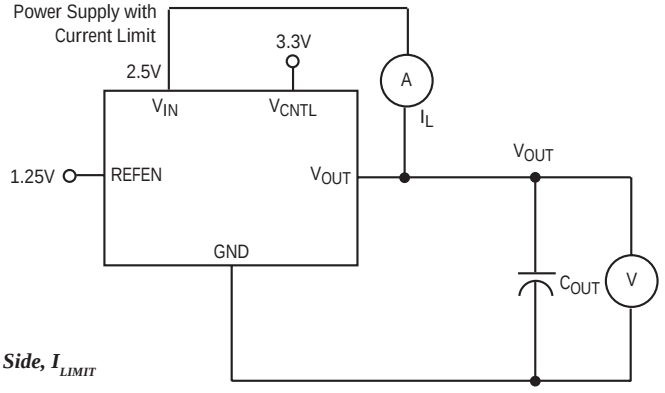
Testing Output Voltage Tolerance, ΔV_{LOAD}



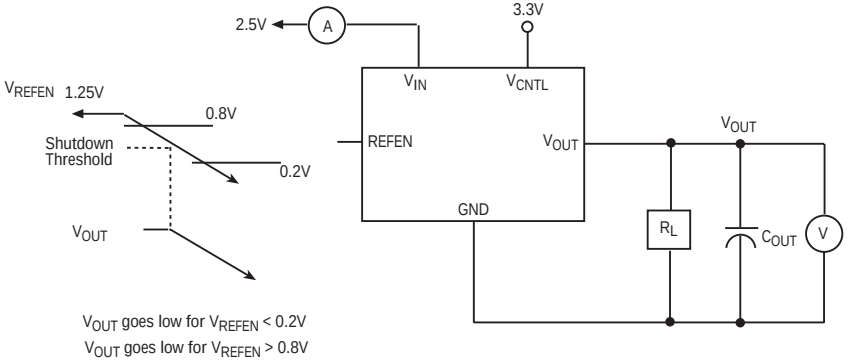
Testing Current in Shutdown Mode, I_{SHDN}



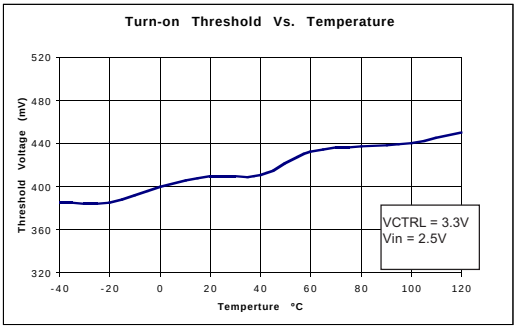
Testing Current Limit for High Side, I_{LIMIT}

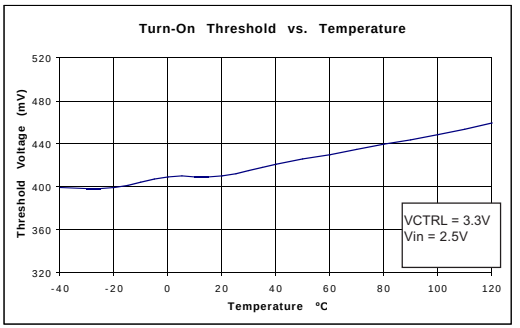


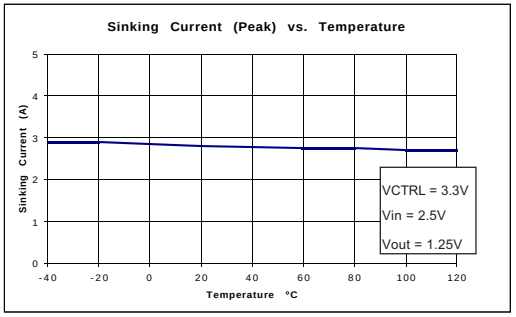
Testing Current Limit for Low Side, I_{LIMIT}

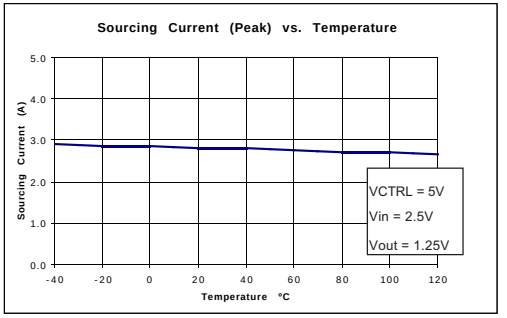


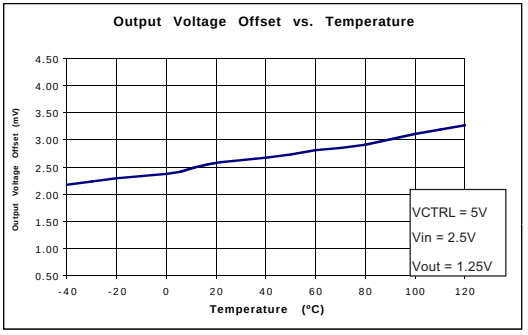
Testing REFEN Pin Shutdown Threshold, , $V_{TRIGGER}$

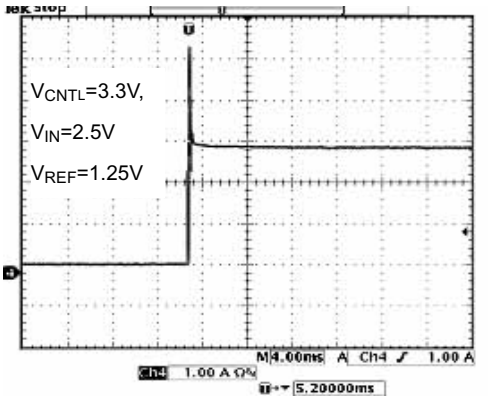




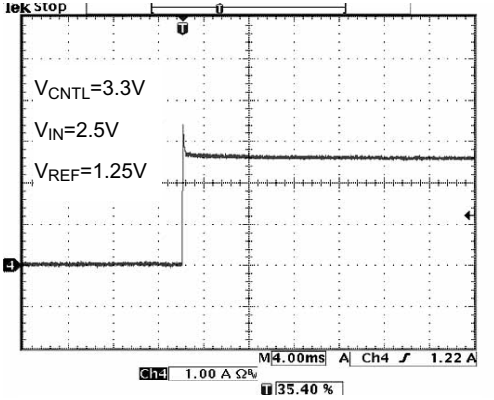




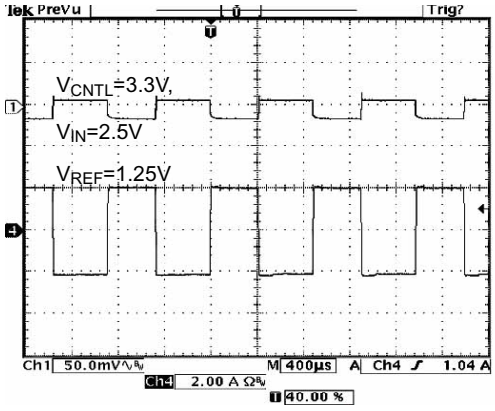




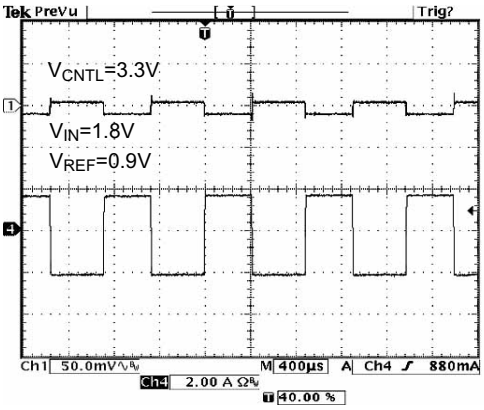
Output Short-Circuit (Sinking)



Output Short-Circuit (Sourcing)



Transient Response at $1.25V_{TT}$/2A



Transient Response at $0.9V_{TT}$/2A

Internal parasitic diode

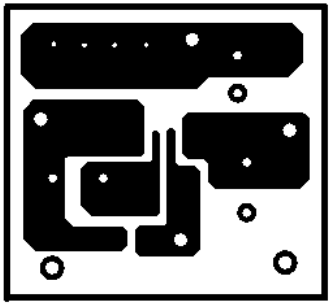
Avoid forward-biasing the internal parasitic diode, V_{OUT} to $V_{CNTL,}$ and V_{OUT} to V_{IN}. Positive voltage should not be applied to the output if V_{IN} and V_{CNTL} are not present.

Considerations for designing, resistance of voltage divider

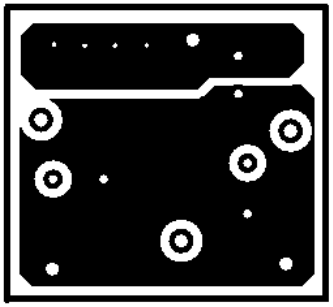
When the reference voltage is programmed below 0.2V the pulldown capability of the internal NMOS transistor is limited. It is recommened to place a filter capacitor from V_{RE} to ground in order to reduce sensitivity to noise and improve power up characteristics (soft start).

Layout Considerations

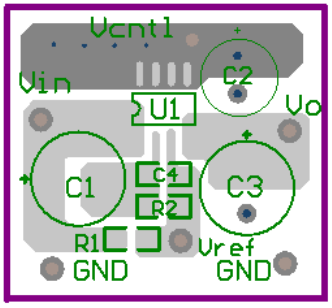
The SP2996B is offered in the NSOIC-8 package , resulting in attention needing to be paid to dissipating heat effectively when it operates in high current. In order to prevent maximum junction temperature from being exceeded, suitable copper area is necessary. The large copper area at V_{CNTL} pins is available, and by taking advantage of this, much heat dissipation is attained. Use vias to direct heat into the bottom layer as the layout examples show below. All capacitors should be placed as close as possible to relative pins.



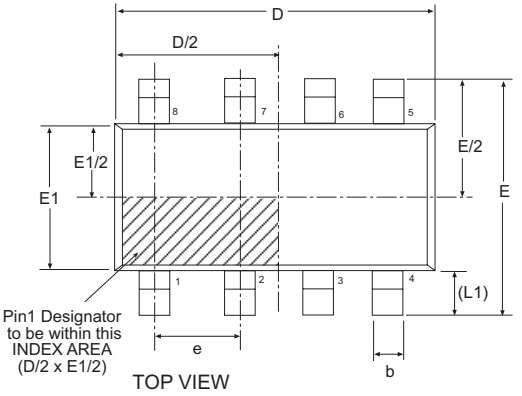
Top layer

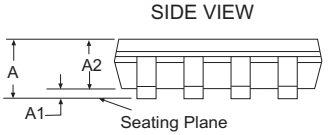


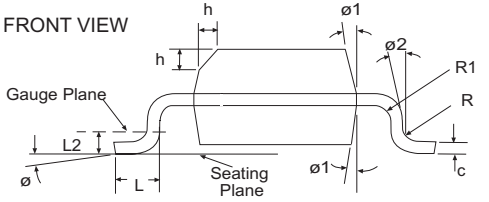
Bottom layer



Placement







8 Pin NSOIC		JEDEC MS-012		Variation AA		
SYMBOL	Dimensions in Millimeters: Controlling Dimension			Dimensions in Inches Conversion Factor: 1 Inch = 25.40 mm		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	-	1.75	0.053	-	0.069
A1	0.10	-	0.25	0.004	-	0.010
A2	1.25	-	1.65	0.049	-	0.065
b	0.31	-	0.51	0.012	-	0.020
c	0.17	-	0.25	0.007	-	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25		0.50	0.010	-	0.020
L	0.40	-	1.27	0.016	-	0.050
L1	1.04 REF			0.041 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	-	-	0.003	-	-
R1	0.07	-	-	0.003	-	-
ø	0º	-	8º	0º	-	8º
ø1	5º	-	15º	5º	-	15º
ø2	0º	-	-	0º	-	-
D	4.90 BSC			0.193 BSC		
SIPEX Pkg Signoff Date/Rev:				JL Aug16-05 / Rev A		

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
SP2996BEN	-40ºC to 85ºC	8 Lead NSOIC
SP2996BEN/TR	-40ºC to 85ºC	8 Lead NSOIC

Available in lead free packaging. To order add "-L" suffix to part number.
Example: SP2996BEN/TR = standard; SP2996BEN-L/TR = lead free.

/TR = Tape and Reel
Pack quantity is 2,500 for NSOIC.

Appendix and Web Link Information

For further assistance:

Email:	Sipexsupport@sipex.com
WWW Support page:	http://www.sipex.com/content.aspx?p=support
Sipex Application Notes:	http://www.sipex.com/applicationNotes.aspx
Product Change Notices:	http://www.sipex.com/content.aspx?p=pcn

Sipex Corporation
Headquarters and
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Milpitas, CA95035
tel: (408) 934-7500
faX: (408) 935-7600

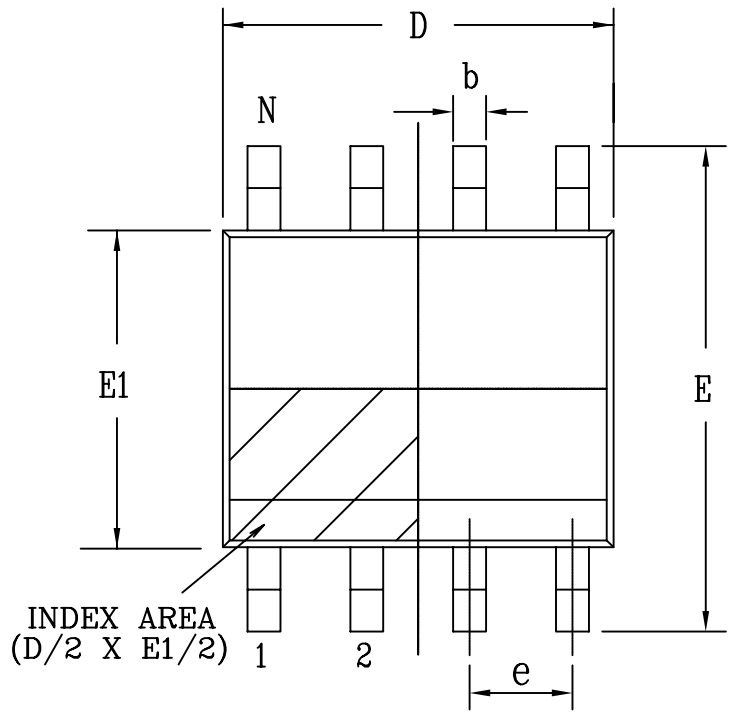
The following sections contain information which is more changeable in nature and is therefore generated as appendices.

1) **Package Outline Drawings**
2) **Ordering Information**

If Available:

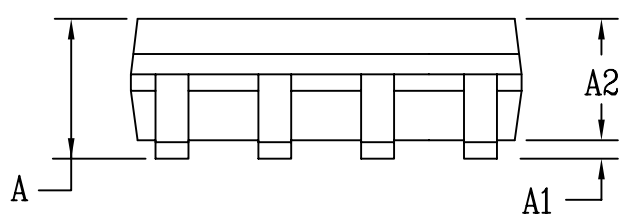
3) **Frequently Asked Questions**
4) **Evaluation Board Manuals**
5) **Reliability Reports**
6) **Product Characterization Reports**
7) **Application Notes for this product**
8) **Design Solutions for this product**

REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	08/16/05	JL
B	DRAWING FORMAT MODIFICATION	07/19/06	JL

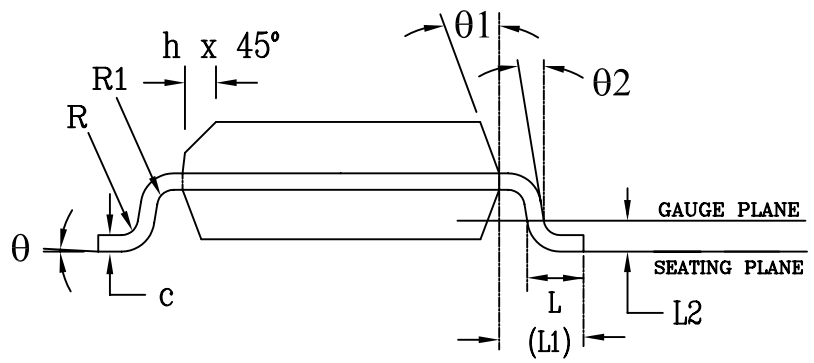


Top View

8 Pin SOICN JEDEC MS-012 Variation AA						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	—	1.75	0.053	—	0.069
A1	0.10	—	0.25	0.004	—	0.010
A2	1.25	—	1.65	0.049	—	0.065
b	0.31	—	0.51	0.012	—	0.020
c	0.17	—	0.25	0.007	—	0.010
E	6.00 BSC			0.236 BSC		
E1	3.90 BSC			0.154 BSC		
e	1.27 BSC			0.050 BSC		
h	0.25	—	0.50	0.010	—	0.020
L	0.40	—	1.27	0.016	—	0.050
L1	1.04 REF			0.041 REF		
L2	0.25 BSC			0.010 BSC		
R	0.07	—	—	0.003	—	—
R1	0.07	—	—	0.003	—	—
θ	0°	—	8°	0°	—	8°
θ1	5°	—	15°	5°	—	15°
θ2	0°	—	—	0°	—	—
D	4.90 BSC			0.193 BSC		
N	8			8		



Side View



Front View

Solved by Sipex		SIPEX CORPORATION	
		8 PIN SOICN PACKAGE OUTLINE	
Packaging Approval:		Drawing No: 8-PIN SOICN	
By: JL	Date: 07/19/06	Revision: B	Sheet: 1 OF 1

Low Cost, High Performance DDR Termination Using SP2996B

Introduction

Double Data Rate (DDR) SDRAM is finding its way into more and more consumer appliances, in addition to its traditional market of PCs and servers. This has led to lower cost requirements for DDR power management, in particular DDR termination. High end servers and PCs tend to use DC/DC buck converter solutions, due to higher current demands (>4A). However, these solutions are costly and over-specified for smaller systems where a lower number of memory devices are used. Initial theories suggested that even in such situations, a capability of up to 3A for termination would be required. However when the overall current requirements are considered, as opposed to just the instantaneous peaks, the solution becomes less onerous.

Load Calculations

In DDR DRAM systems, Stub Series Terminated Logic (SSTL) is the preferred termination architecture for critical control and data signals. It dramatically reduces unwanted reflections and Electromagnetic Interference (EMI), thus improving speed and noise margins. The JEDEC SSTL 2 standard defines the termination scheme featured in Figure 1.

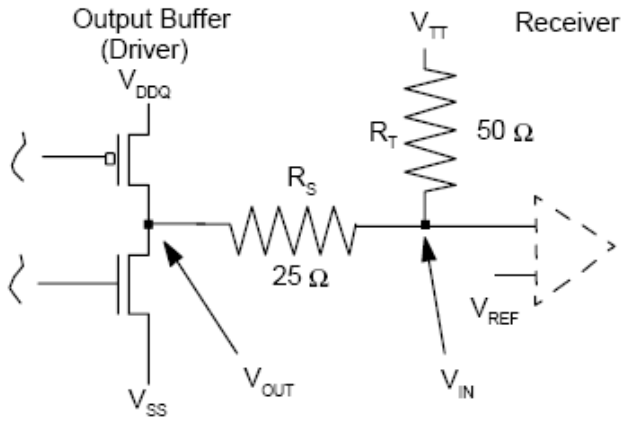


Figure 1 SSTL 2 Standard

In Figure 1, the value of R_T can be either 50Ω (Class 1 Termination) or 25Ω (Class 2 Termination). Since 25Ω represents the greater load for the V_{TT} supply, this value will be used for the remaining calculations.

The requirement is that V_{OUT} has sufficient magnitude when driving into the termination network, to establish V_{IN} as greater than or equal to the minimum threshold at the receiver to guarantee correct recognition of a 1 or 0. From this requirement, using SSTL 2 data [1] we can derive the supply current (I_{TT}) for V_{TT}:

V_{INmin} = 405mV
R_T = 25Ω
R_S = 25Ω

$I_{TT} = (V_{TT} – V_{INmin}) \div R_T$ = 16.9mA

This represents the minimum current required, in practice the figure is closer to 20mA.

Consider the case for 1Gb 32 bit system. This is typically organised as 13 multiplexed address lines, 32 data lines, 12 strobe/mask and various command signals (RAS, CAS, WE, CKE, BA, etc). The total is around 64 depending upon exact implementation. With each terminated signal consuming ~20mA, this gives a total load of 1.28A max. This brings into consideration linear solutions, such as SP2996B, which as can be seen from Figure 2, offers a simpler, smaller and much more cost effective solution than any switching equivalent. Additional benefits over buck converters are improved speed, lower noise and vastly reduced possibility of EMI issues.

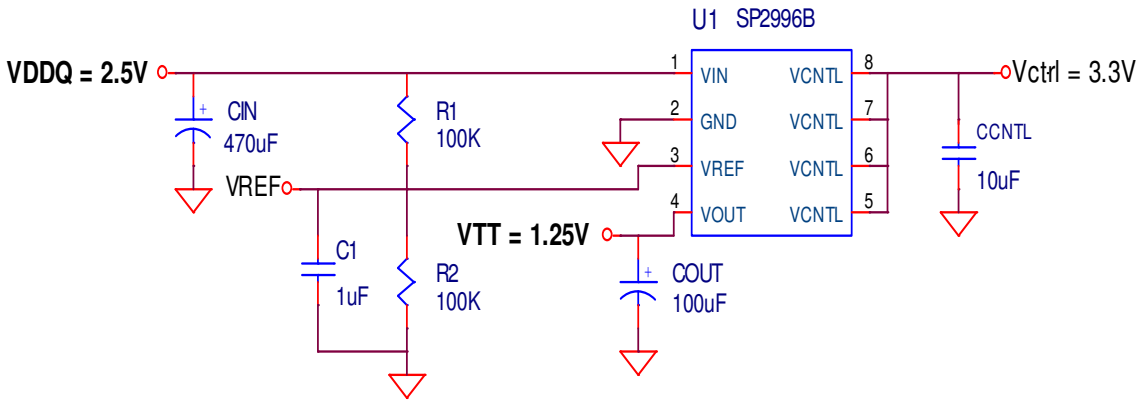


Figure 2 SP2996B Schematic

Averaging Considerations

The above calculations represent a true worst case scenario, which in practice is unlikely to occur, and certainly cannot persist. This figure assumes that all the data, address and control lines are at the same state in a single instant. This is clearly not possible. Further, even if the data and address lines were all at 1, for example, this would only be a momentary incidence. Typically the data and address lines average out over a period of time to an RMS voltage much closer to Vtt (empirical research and measurements suggest the maximum peak load of 1.3A translates to an average load of around 250mA). In order to deliver peak currents, (DDR cycles last only in the order of tens of ns) an output capacitor of reasonable value could absorb the instantaneous changes and average them out to the lower, average current demand. This will then become the average current supplied by the SP2996B. For a DDR cycle that lasts 20ns (dependent on clock speed), even with a worst case 1.26A load, this results in <30nC of charge, which would deplete a 100uF cap by <500uV. Thus a number of repetitive cycles could be tolerated before the regulator must top up the capacitor.

Power Calculations

The max V_{DD} is 2.5V, with a regulation of 250mA down to the 1.25 volts required for V_{TT}, the power dissipated is 313mW. This is easily within the capability of the SP2996B which has a θ_{JA} of 128˚C/W, giving a 40˚C rise over ambient temperature.

DDR2 Specifications

In order to facilitate lower power consumption and higher data rates, DDR2 operates from 1.8V supply with V_{TT} = 0.9V. The revised JEDEC SSTL 1.8 termination load is now as shown in Figure 3. With the lower value of V_{DDQ} (1.8V nominal) it is likely that the output transistors will now operate more in the linear region. Thus a specification for the ON resistance (R_{ON}) is defined as <21R to ensure the required current delivery (I_{TT})into the termination network. Using this value, along with RS and RT gives the following:

V_{DDQ} = 1.8V
V_{TT} = 0.9V
$I_{TT} = V_{TT} /(R_T + R_S + R_{ON})$ = 13.6ma.

This represents a minimum value, (ie R_{ON} = 21Ω), typically values are around 16mA.

Using the same 1Gb scenario as earlier, this gives a total peak load of 64 x 16mA = 1.02A. The same averaging effects apply with DDR2, hence a realistic average termination current would be 210mA. With a V_{DDQ} now equal to 1.8V, the power handling required by the SP2996 goes down to 210mA x 0.9V = 192mW for the DDR2 termination. This would give a temperature rise over ambient of approximately 25°C.

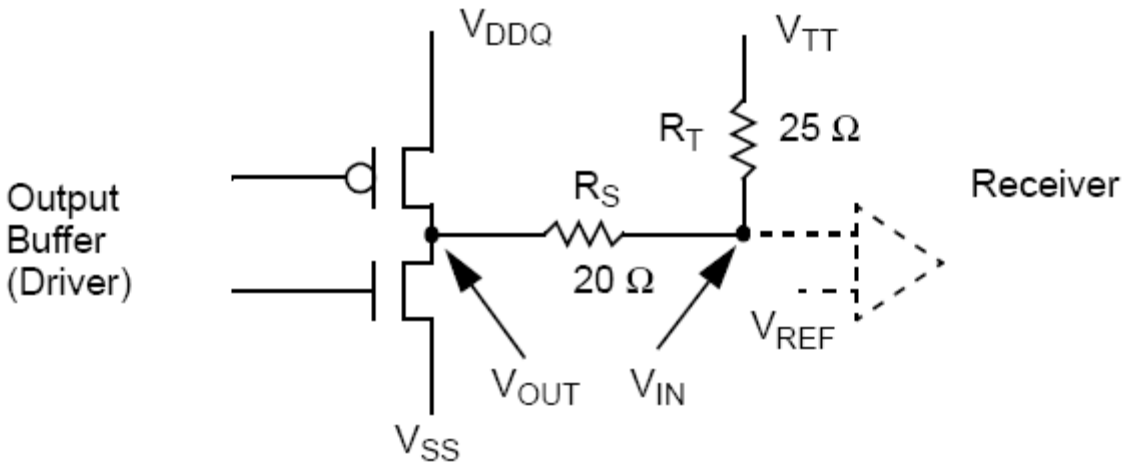


Figure 3 JEDEC SSTL 1.8 Load

System Applications and the Vddq Supply

The demands for V_{DDQ} are somewhat higher than V_{TT}, usually necessitating the use of DC-DC buck solutions. For smaller systems, the load is in the range of 1-3A and can be considerably higher for larger capacity. Figure 4 shows a complete solution for V_{DDQ} and V_{TT} from a 3.3V to 5V supply for systems with a V_{DDQ} requirement of <4A. Figure 5 shows a complete solution derived from a 12V supply for systems with a V_{DDQ} in the 2A to 10A range. This system uses ceramic caps, and its synchronous nature allows it to efficiently develop lower output voltages, thereby making it well suited to DDR2 applications. The same solution can also be used with a 5V input by component value changes to the compensation network. (Contact Sipex applications support for full details.)

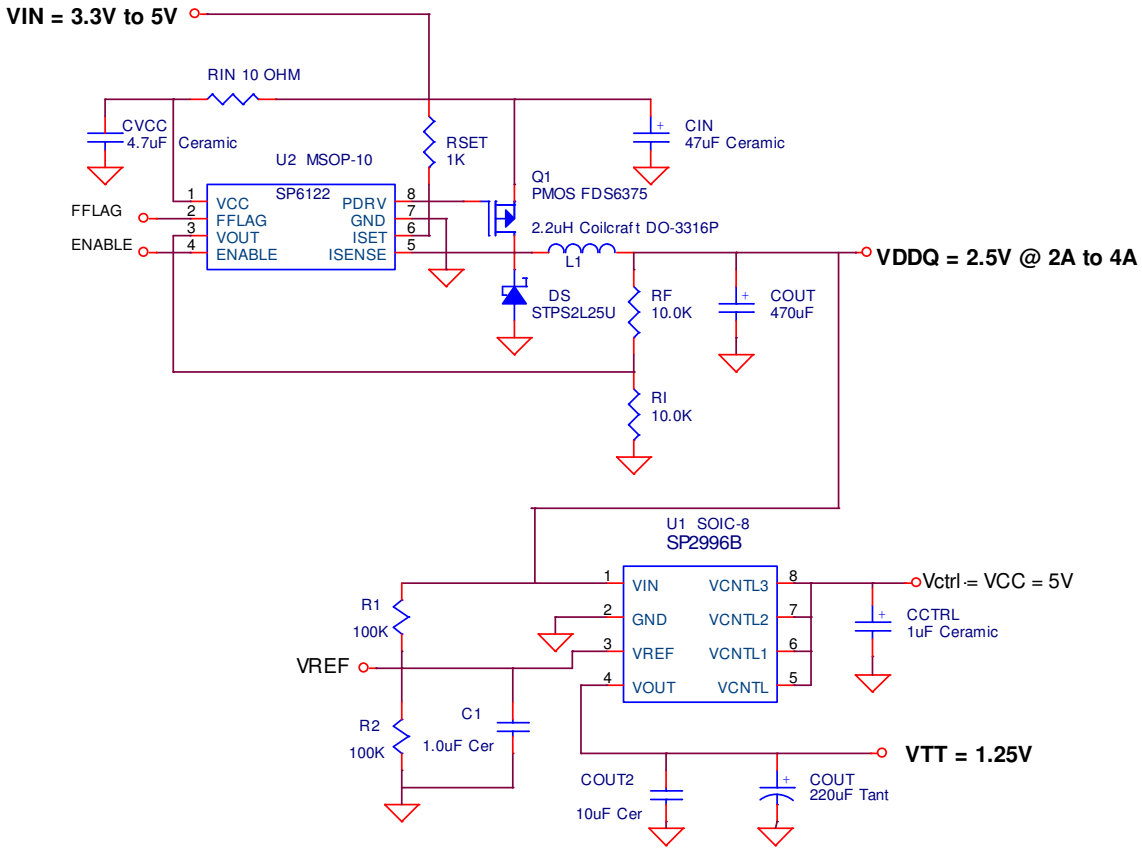


Figure 4 Complete DDR Solution 3.3V to 5V Input, VDDQ <4A

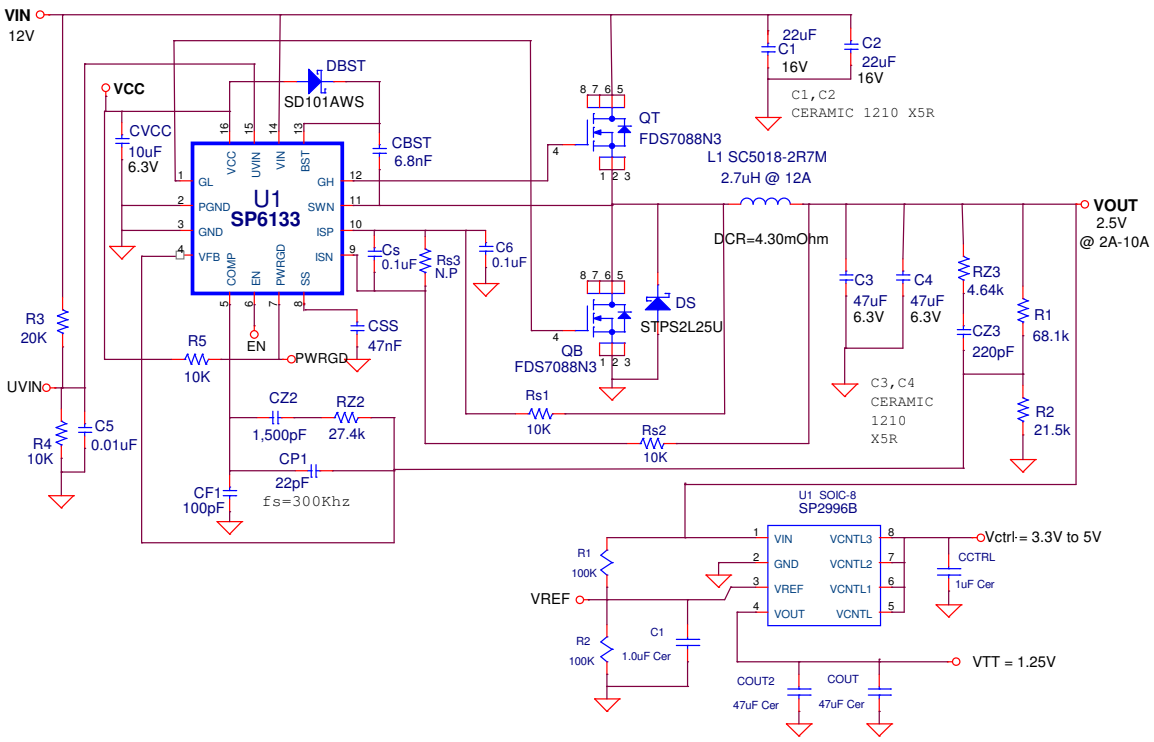


Figure 5 Complete DDR Solution 12V Input, VDDQ <10A

Conclusion

For smaller DDR and DRR2 applications (e.g., Digital Set Top Boxes) the SP2996 offers large space (75%) and cost (60%) savings over DC-DC based implementations. Its simple architecture and high speed reduce component count, while offering fast transient response and zero switching noise. When used in conjunction with either of the V_{DDQ} solutions highlighted, a complete memory power management is realized.

References

[1] JESD8-9B Stub Series Terminated Logic for 2.5V
[2] JESD8-15A Stub Series Terminated Logic for 1.8V

Design Solution 2

SP2996 DDR Termination Circuit Using Ceramic Capacitors

Date: January 2, 2006

Designed by: Mark Boermeester (mboermeester@sipex.com)

Part Number: SP2996B

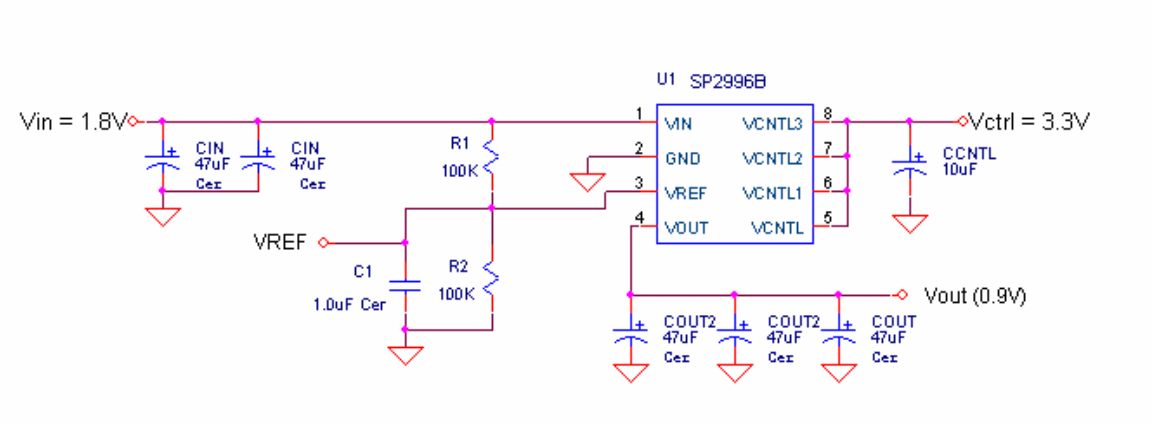
Application Description: Linear regulator for DDR memory termination

Electrical Requirements:

Input Voltage	1.8V
Output Voltage	0.9V
Output Current	2A

Circuit Description:

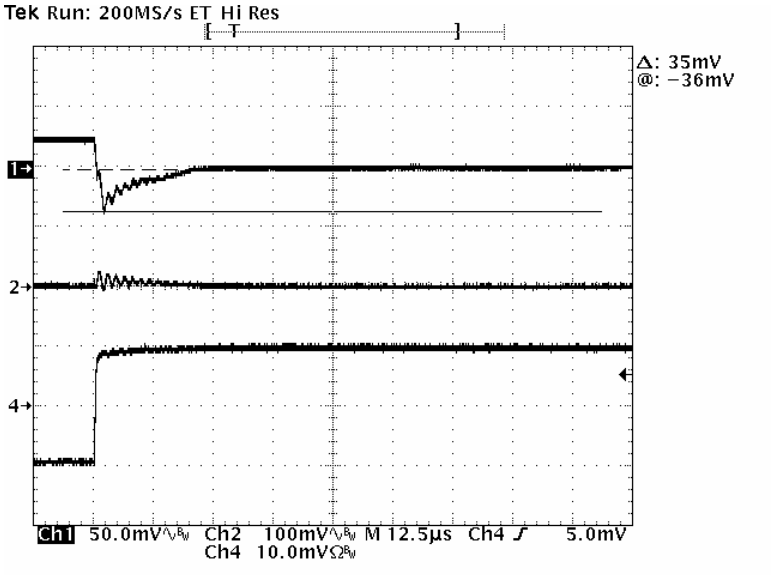
This Design Solution provides transient response measurement for the SP2996B DDR termination device using different values output capacitors. In order to demonstrate stable operation the circuit was tested with ceramic capacitors under transient loads.



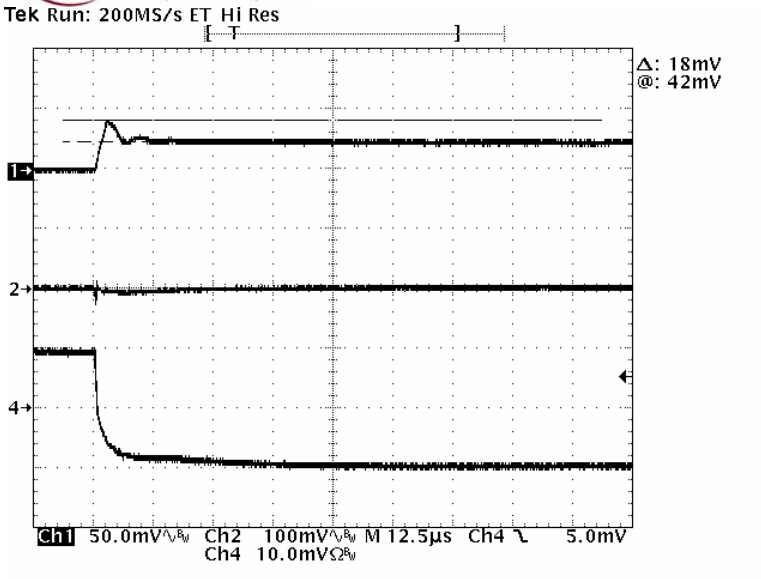
The following figures show scope plots for increase and decrease in load current. Output voltage is represented by channel 1, reference voltage by channel 2 and output current by channel 4 (2A/DIV).

Test 1

Output Capacitance: 3 x 47uF (141 uF total)
Transient Description: Sink to Source
Output Voltage Overshoot: 35mV

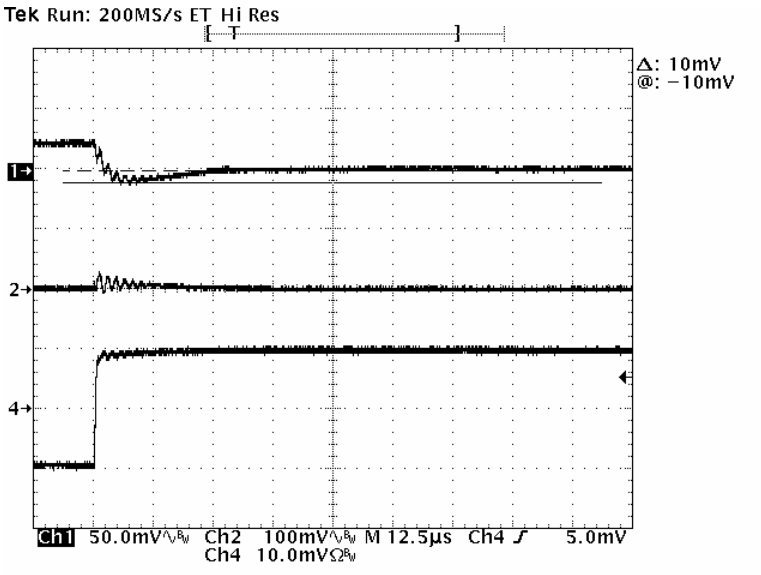


Transient Description: Source to Sink
Output Voltage Overshoot: 18mV

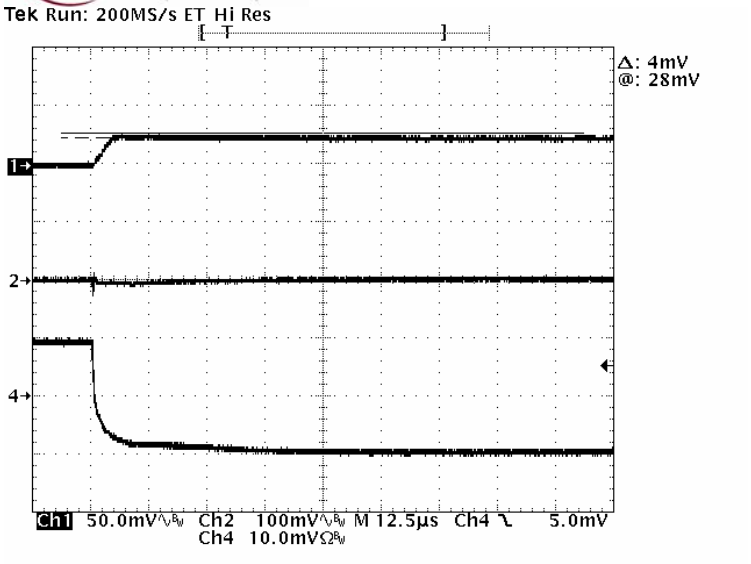


Test 2

Output Capacitance: 4 x 47uF (188uF total)
Transient Description: Sink to Source
Output Voltage Overshoot: 10mV

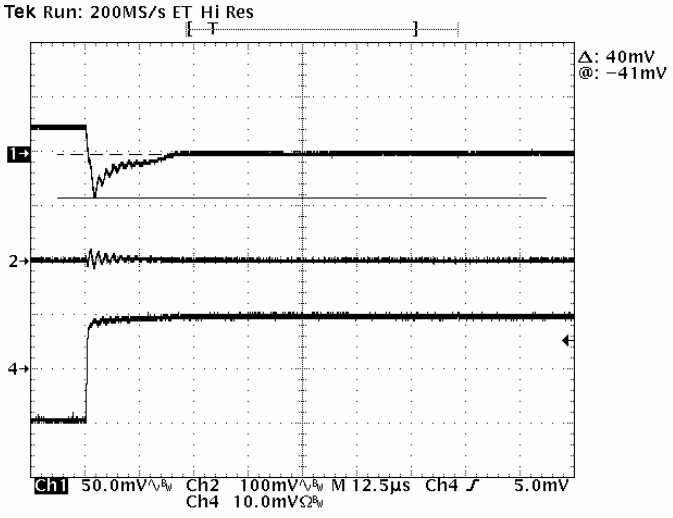


Transient Description: Source to Sink
Output Voltage Overshoot = 4mV

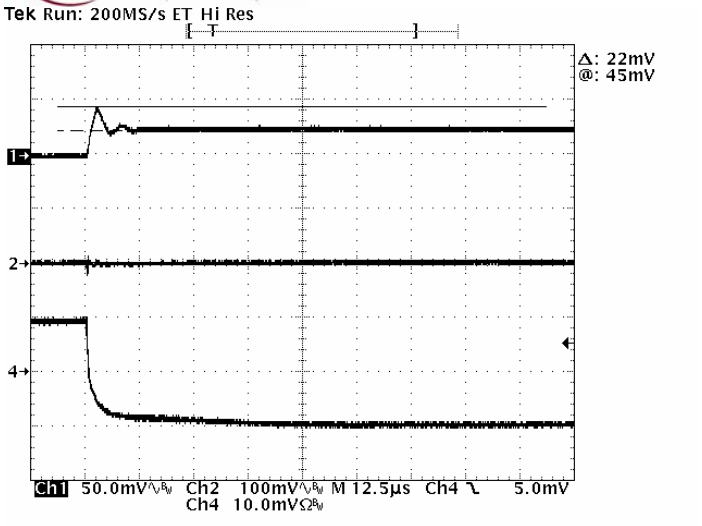


Test 3

Output Capacitance: 2 x 47uF (96uF total)
Transient Description: Sink to Source
Output Voltage Overshoot: 40mV



Transient Description: Source to Sink
Output Voltage Overshoot: 22mV


Tek Run: 200MS/s ET Hi Res
Δ: 22mV
@: 45mV
1→
2→
4→
Ch1 50.0mV Ch2 100mV M 12.5µs Ch4 5.0mV
Ch4 10.0mV