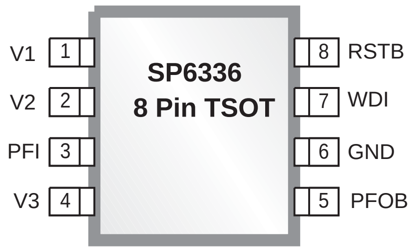
SP6336, SP6337, & SP6338

Triple µPower Supervisory Circuit with Watchdog and Power Fail

FEATURES

- Low operating voltage of 1.6V
- Low operating current of 20µA typical
- Monitors up to 3 supplies simultaneously
- Adjustable inputs monitor down to 0.5V
- Reset asserted down to 0.9V
- 2% accuracy over temperature range
- Power Fail Input Functionality (PFI)
- Power Fail Output function, active low (PFOB)
- Open Drain (OD) or CMOS RSTB output
- 4 Reset Timeout Periods: 50ms, 100ms, 200ms and 400 ms
- Watch Dog Input Functionality
- Available in Lead Free, RoHS Compliant Package: 8 pin TSOT



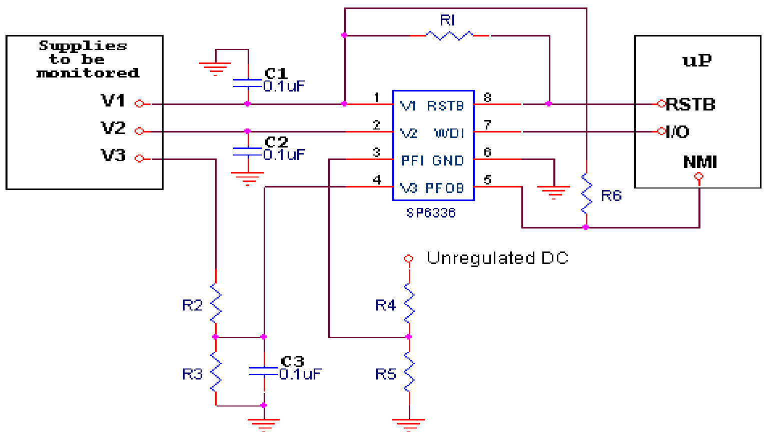
Open Drain $\overline{\text{RESET}}$

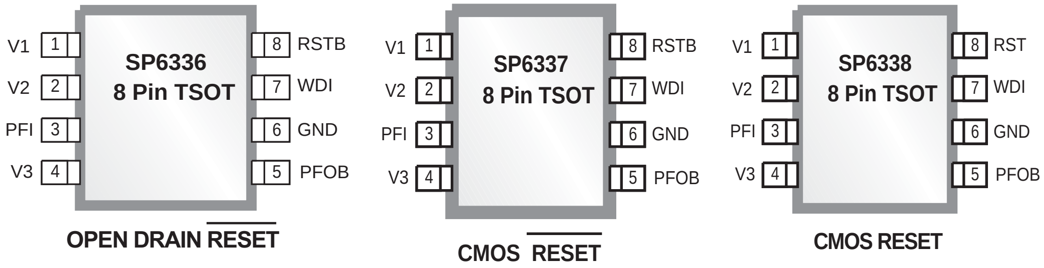
SEE PAGE 2 FOR OTHER AVAILABLE PINOUTS

DESCRIPTION

The SP6336 - SP6337 - SP6338 Triple µPower Supervisory Circuit Family is a family of microprocessor reset supervisory circuits with multiple reset voltages. The family provides low voltage monitoring ability for up-to three supplies with two precision factory-set thresholds and one user defined custom threshold. These circuits perform a single function: if any of the input supply voltages drops below its associated threshold, reset outputs are asserted. The products in the family offer power fail and watchdog functionalities. SP6336 , SP6337 & SP6338 are packaged in an 8-pin TSOT package. All devices are fully specified over -40°C to +85°C temperature range.

TYPICAL APPLICATION CIRCUIT





PART NUMBER	V1	V2	V3	Reset	WatchDog Input	Power Fail Input	Power Fail Output BAR
SP6336	√	√	√	OD Active Low	√	√	√
SP6337	√	√	√	CMOS Active Low	√	√	√
SP6338	√	√	√	CMOS Active High	√	√	√

Feature and Pinout Diagram

ABSOLUTE MAXIMUM RATINGS

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections of the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability and cause permanent damage to the device.

Terminal Voltage (with respect to GND)
V1, V2.. -0.3 to +6V

Open-Drain RSTB, PFOB.......................-0.3 to +6V

CMOS RST, RSTB...................... -0.3 to (V1+0.3V)

Input Current/Output
Current.................................,,.......................20mA

V3, V4, PFI, WDI...........................-0.3 to (V1+0.3V)

Operating Temperature
Range..-40°C to +85°C

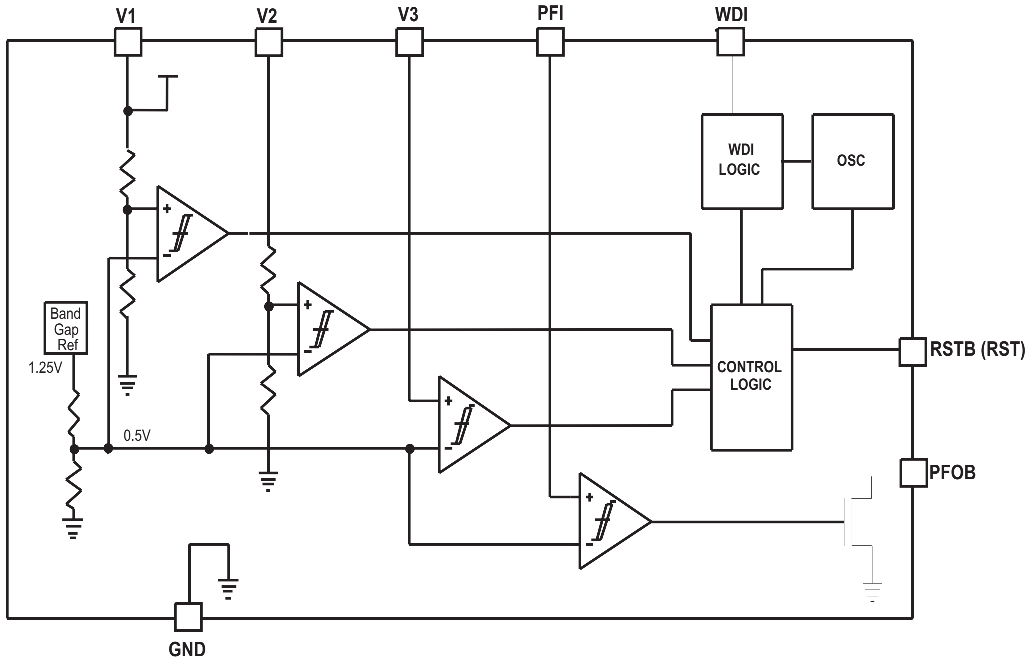
Storage Temperature
Range..-65°C to 150°C

Thermal Resistance θ_{JA} ....134°C/W

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V1 =1.6V to 5.5V; TA = -40ºC to +85ºC; unless otherwise noted. Typical values are at TA =+25ºC					
Operating Voltage Range	0.9		5.5	V	T_A = -40ºC to +85ºC
Supply Current		20	30	uA	V1 < 5.5V, V2 < 3.60V, all I/O pins open
		15	25		V1 < 3.6V, V2 < 2.75V, all I/O pins open
V1 Reset Threshold	4.532	4.625	4.718	V	Z (valid for V1 falling)
	4.287	4.375	4.463		Y (valid for V1 falling)
	3.013	3.075	3.137		X (valid for V1 falling)
	2.866	2.925	2.984		W (valid for V1 falling)
	2.572	2.625	2.678		V (valid for V1 falling)
	2.273	2.320	2.367		U (valid for V1 falling)
	2.146	2.190	2.234		T (valid for V1 falling)
	1.636	1.670	1.704		S (valid for V1 falling)
	1.548	1.580	1.612		R (valid for V1 falling)
V2 Reset Threshold	2.266	2.313	2.360	V	J (valid for V2 falling)
	2.144	2.188	2.232		I (valid for V2 falling)
	1.631	1.665	1.698		H (valid for V2 falling)
	1.543	1.575	1.607		G (valid for V2 falling)
	1.360	1.388	1.416		F (valid for V2 falling)
	1.286	1.313	1.340		E (valid for V2 falling)
	1.087	1.110	1.133		D (valid for V2 falling)
	1.029	1.050	1.071		C (valid for V2 falling)
	0.816	0.833	0.850		B (valid for V2 falling)
	0.772	0.788	0.804		A (valid for V2 falling)
Threshold 1 Tempco		0.06		mV/ºC	
Threshold 2 Tempco		0.04		mV/ºC	
Threshold 1 Hysteresis		0.65		%	reference to Vth1 typical
Threshold 2 Hysteresis		0.5		%	reference to Vth2 typical
V1 to RST/RSTB Delay		50		us	V1 = Vth1 to (Vth1-0.1V), Vth1 = 3.075
V2 to RST/RSTB Delay		50		us	V2 = Vth2 to (Vth2-0.1V), Vth2 = 1.575
Reset Timeout Period (T1)	37	50	63	ms	TOPT-1
Reset Timeout Period (T2)	74	100	126	ms	TOPT-2
Reset Timeout Period (T3)	148	200	252	ms	TOPT-3
Reset Timeout Period (T4)	296	400	504	ms	TOPT-4
V3 RESET COMPARATOR INPUT					
V3 Input Threshold	490	500	510	mV	
V3 Input Current	-50		50	nA	T_A = +25ºC
V3 Threshold Hysteresis		1.5		mV	

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V1 =1.6V to 5.5V; TA = -40ºC to +85ºC; unless otherwise noted. Typical values are at TA =+25ºC					
WDI – WATCHDOG INPUT					
Watchdog Timeout Period	1.2		2	sec	
WDI Pulse Width	0.1			µs	
WDI Input Threshold			0.4	V	
	0.8*V1				
WDI Input Current	-500		+500	µA	WDI = 0.0V or V1
RESET & POWER FAIL OUTPUTS RST / RSTB / WDOB / PFOB					
RSTB (CMOS or OD)			0.4	V	V1 = Vth1 - 0.1V, Isink = 1mA, output asserted
PFOB			0.4		V_PFI=0.4, V1= , Isink = 1mA, PFOB output asserted
RSTB (CMOS)	0.8*V1			V	V1 = Vth1+0.1V, Isource = 1mA, output not asserted
RST (CMOS)	0.8*V1			V	V1 = Vth1-0.1V, Isource = 1mA, output asserted
RST (CMOS)			0.4	V	V1 = Vth1+0.1V, V2 > Vth2, V3 > 0.5 , V4 > 0.5 Isource = 1mA, output not asserted
RSTB / WDOB / PFOB Output Open-Drain Leakage Current		2		nA	Output asserted
PFI - POWER FAIL INPUT					
PFI Input Threshold	490	500	510	mV	
PFI Input Current	-50		50	nA	
PFI Hysteresis		2.5		mV	
PFI to PFOB Delay		4		µs	

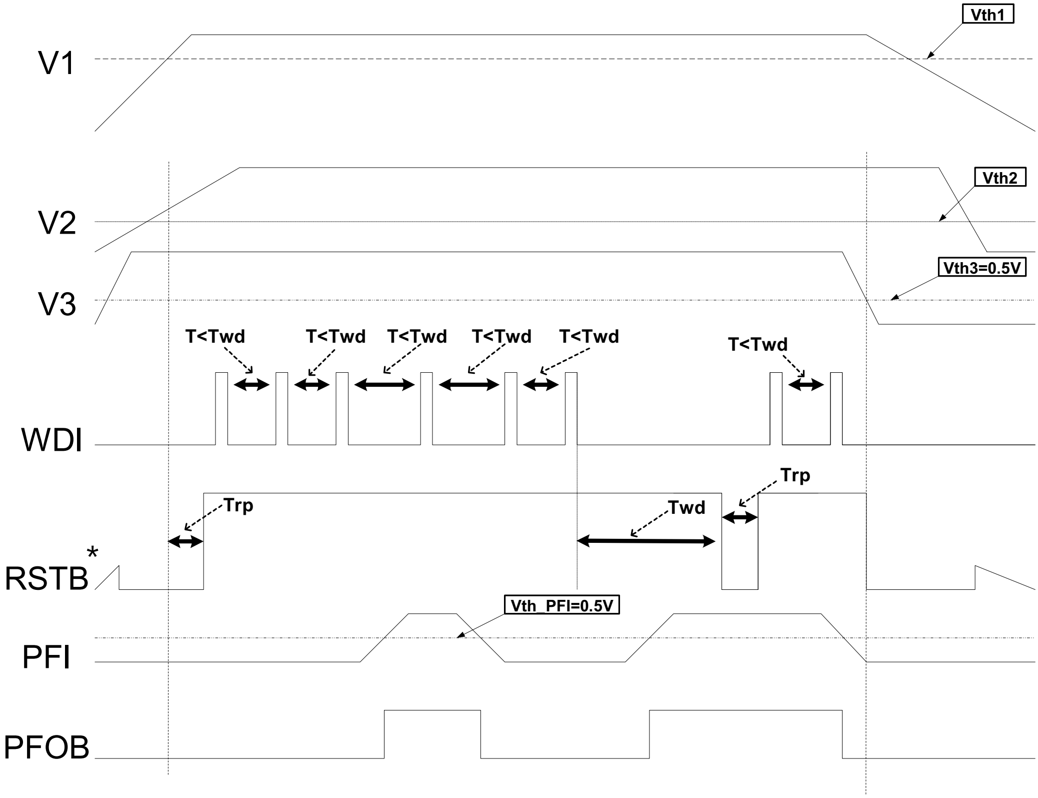
Pin #	Name	Description
1	V1	First supply voltage input. Also powers internal circuitry. Trip threshold voltage is internally set.
2	V2	Second supply voltage input. Trip threshold voltage internally set.
3	PFI	Power Fail Input pin. Trip threshold is 0.5V. When the input voltage at the PFI pin is <0.5V, PFOB is low. Connect to GND or V1 if not used.
4	V3	Input for the third supply voltage. Trip threshold is 0.5V.
5	PFOB	Power Fail Output pin. Active low open drain output. When the input voltage at the PFI pin is <0.5V, PFOB is low.
6	GND	Common ground reference pin.
7	WDI	Watch-Dog Input pin. When no transition is detected at the WDI pin for the duration of WDI timeout period, reset is asserted. Leave open if not used. RST/RSTB output is used to signal watchdog timeout overflow, and its output pulses high/low (depending on the active reset polarity) for the reset timeout period after each watchdog timeout overflow. The watchdog timer clears whenever the reset is asserted or manual reset is asserted or a transition is observed at WDI pin. Watchdog timer functionality can be disabled by leaving this input floating.
8	RST/RSTB	Reset output. Open-Drain or CMOS, active high or low. Reset is asserted when any of the three supply inputs is below its trip threshold. It stays asserted for 200 ms (typical / default) after the last supply input traverses its trip threshold. Reset is guaranteed to be in the correct state for V1>0.9V. RST/RSTB asserts when V1 or V2 or V3 drop below their corresponding reset thresholds, or the watchdog timer triggers a reset. RST/RSTB remains asserted for the reset timeout period after V1 and V2 and V3 exceed their corresponding reset thresholds. Open-drain outputs require an external pull-up resistor. CMOS outputs are referenced to V1.



Block Diagram

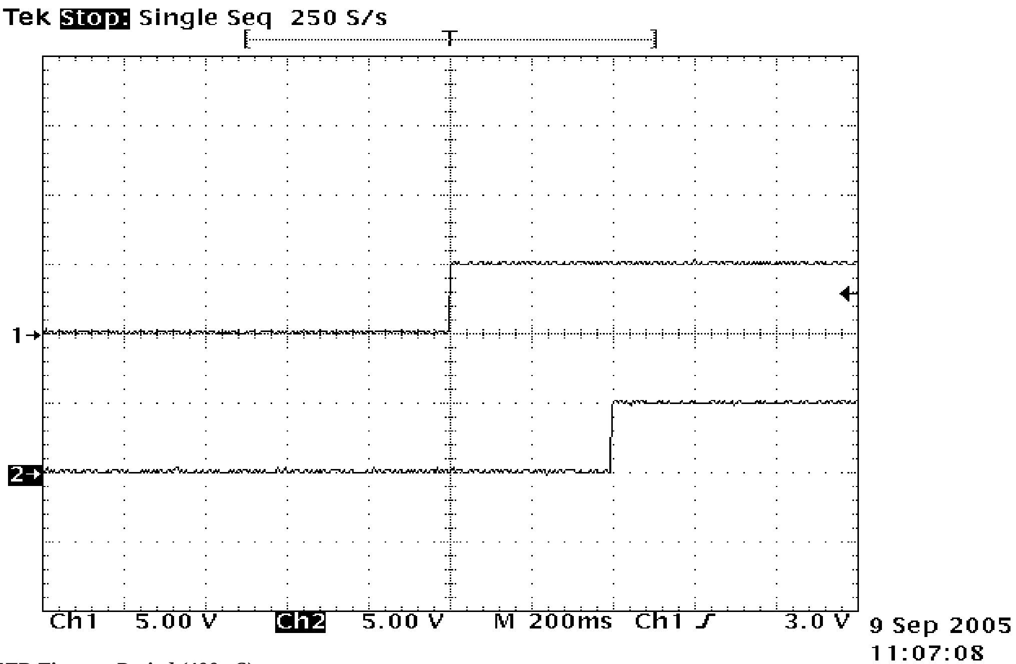
The SP6336/ 6337 / 6338 family includes a low-voltage precision bandgap reference, three precision comparators, an oscillator, a digital counter chain, a logic control block, trimmed resistor divider chains and additional supporting circuitry. The family is designed to supervise up to 3 independent supply voltages. V1 and V2 supply inputs have their resistor dividers on the chip. Their trip thresholds are factory trimmed. V3 input allows users to customize an additional supply threshold to be monitored by means of external resistor dividers. Each part is furnished with power fail indication and watchdog functionalities.

The watchdog timer is serviced internally during the watchdog timeout period when WDI is left unconnected. Thus, watchdog functionality can be disabled via leaving the WDI input floating.

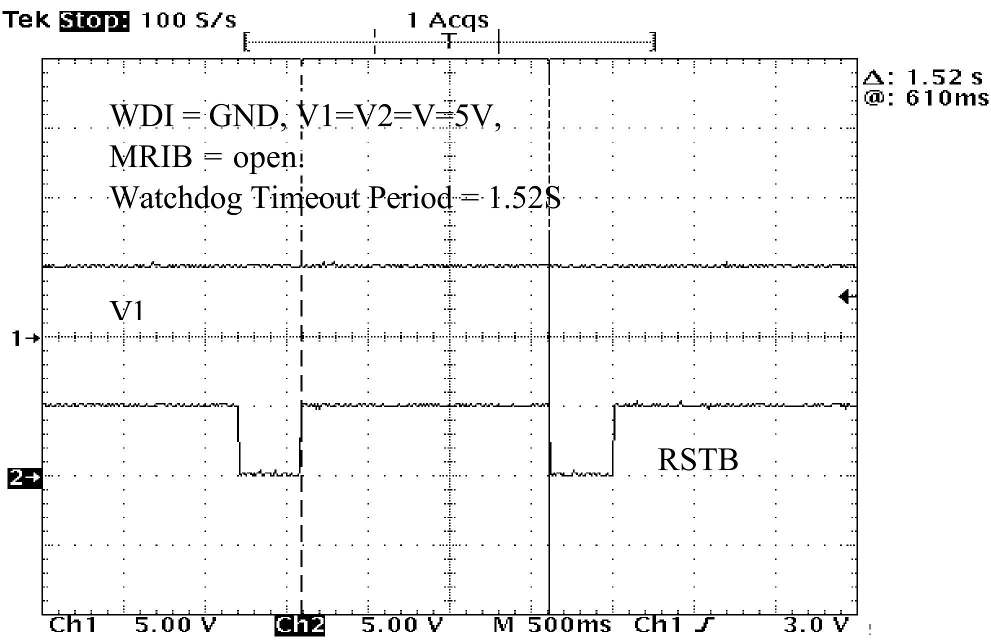


Timing Diagram for SP6336, SP6337, SP6338

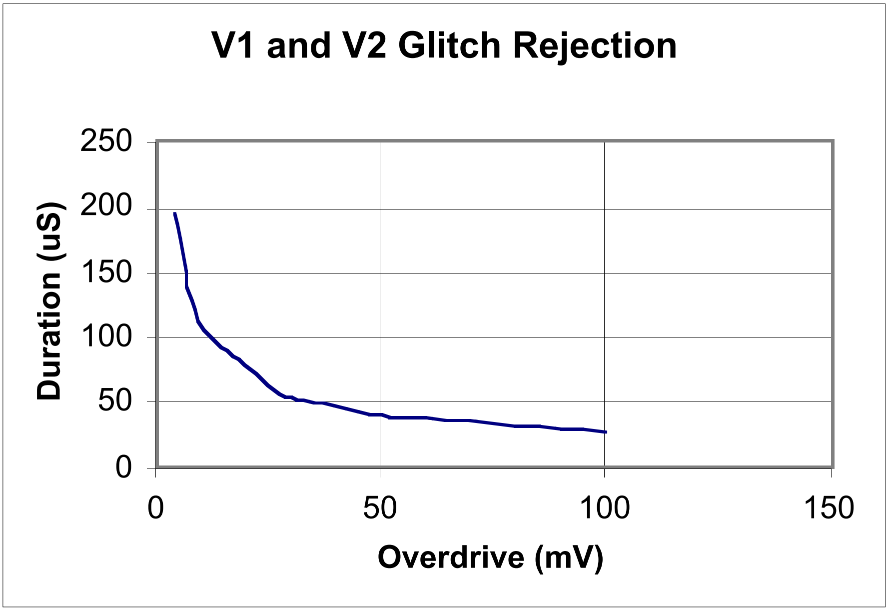
* Reverse Polarity for the SP6338



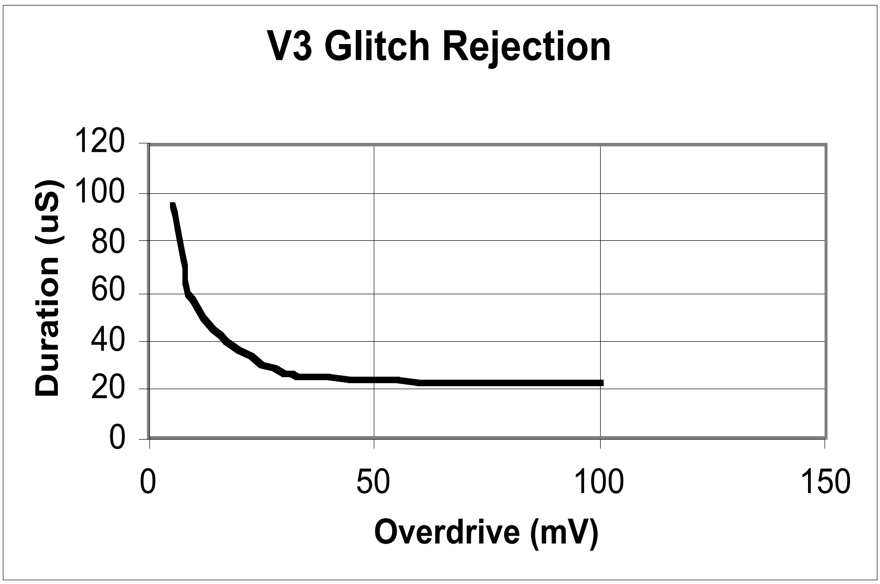
RESETB Timeout Period (400mS)



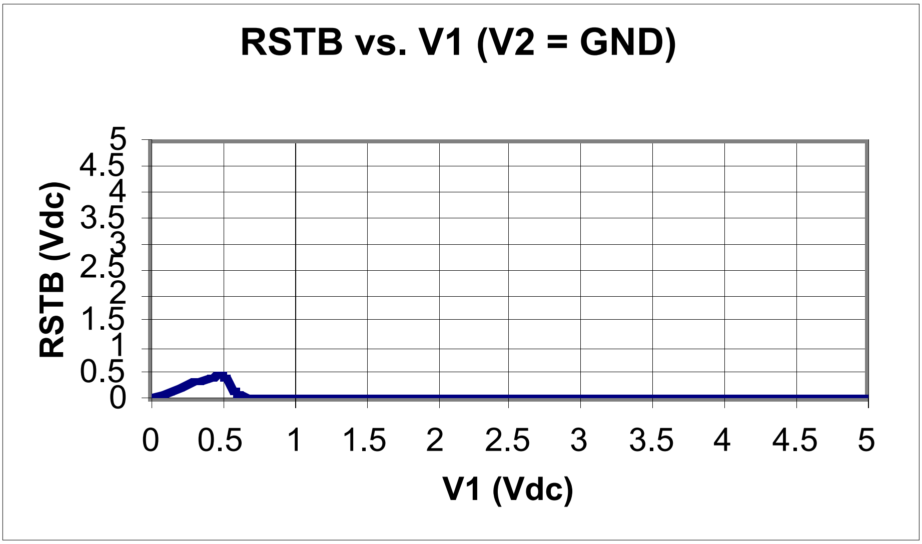
SP6336 Watchdog Timeout Period



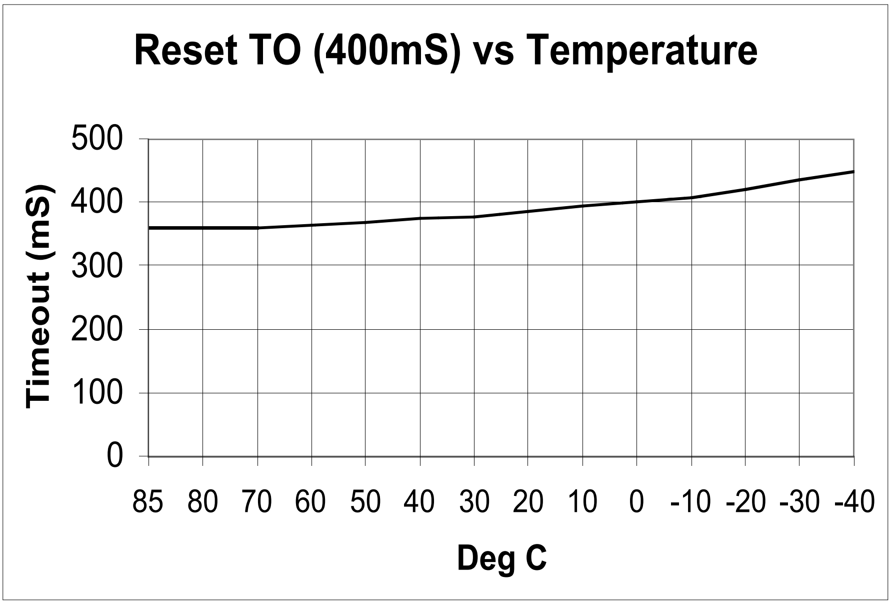
V1 and V2 Glitch Rejection



V3Glitch Rejection



Reset Good



Reset Timeout vs. Temperature

Part Naming Nomenclature

SP63NN - Th1 - Th2 - TOPT

TOPT:
- A -- 50 ms
- B -- 100 ms
- C -- 200 ms
- D -- 400 ms

Th2:
- A -- 0.788 V
- B -- 0.833 V
- C -- 1.050 V
- D -- 1.110 V
- E -- 1.313 V
- F -- 1.388 V
- G -- 1.575 V
- H -- 1.665 V
- I -- 2.188 V
- J -- 2.313 V

Example:
GZJD means:
SP6336 in TSOT-6 lead package
V1 Threshold is 4.625V
V2 Threshold is 2.313V
Reset Timeout is 400ms

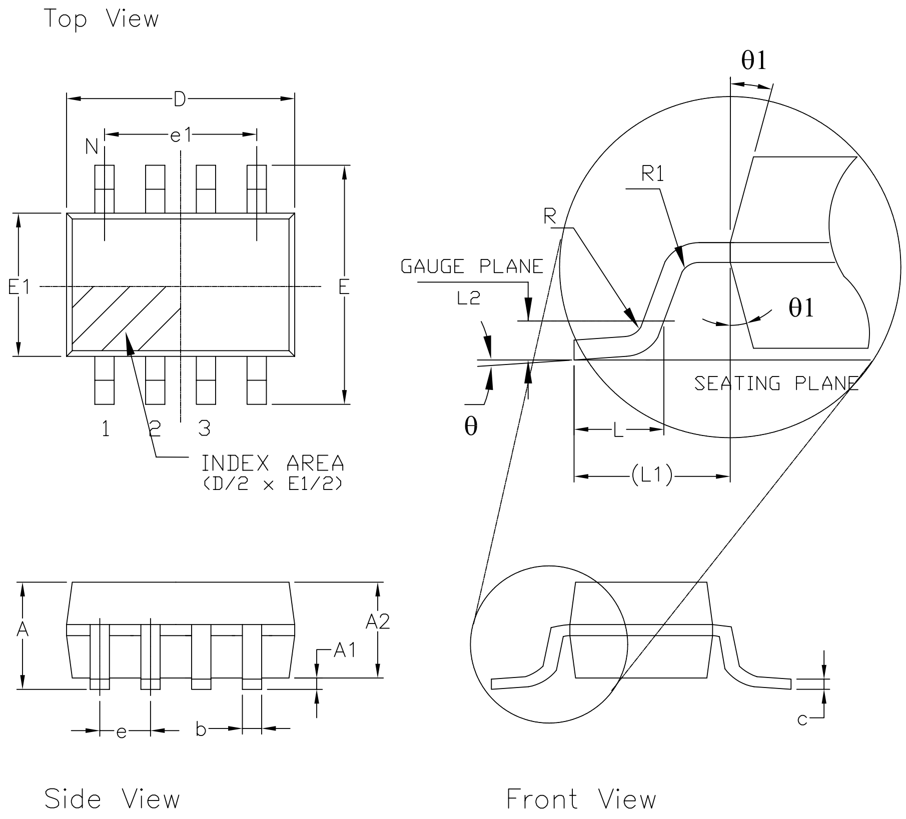
GZJD

Pin 1

Th1:
- Z -- 4.625 V
- Y -- 4.375 V
- X -- 3.075 V
- W -- 2.925 V
- V -- 2.625 V
- U -- 2.320 V
- T -- 2.190 V
- S -- 1.670 V
- R -- 1.580 V

SP63NN:
- A 30 -- Quad Sp, MR, WDI, OD RSTB
- B 31 -- Quad Sp, OD RSTB
- C 32 -- Quad Sp, MR, WDI, CMOS RSTB
- D 33 -- Quad Sp, CMOS RSTB
- E 34 -- Quad Sp, MR, WDI, CMOS RST
- F 35 -- Quad Sp, CMOS RST
- G 36 -- Triple Sp, WDI, PF, OD RSTB
- H 37 -- Triple Sp, WDI, PF, CMOS RSTB
- I 38 -- Triple Sp, WDI, PF, CMOS RST
- J 39 -- Triple Sp, MR, WDI, OD RSTB - WDOB
- K 40 -- Dual Sp, WDI, OD RSTB - WDOB
- L 41 -- Triple Sp, WDI, PF, CMOS RSTB - WDOB
- M 42 -- Dual Sp, WDI, CMOS RSTB - WDOB

REVISION HISTORY			
REV.	DISCRIPTION	DATE	APP'D
A	DRAWING ORIGINATION	10/03/05	JL
B	DRAWING FORMAT MODIFICATION	09/13/06	JL



8 Pin TSOT JEDEC MO−193 Variation BA						
SYMBOLS	DIMENSIONS IN MM (Control Unit)			DIMENSIONS IN INCH (Reference Unit)		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.10	—	—	0.043
A1	0.00	—	0.10	0.000	—	0.004
A2	0.70	0.90	1.00	0.028	0.036	0.039
b	0.22	—	0.38	0.009	—	0.015
c	0.08	—	0.20	0.003	—	0.008
D	2.90 BSC			0.114 BSC		
E	2.80 BSC			0.110 BSC		
E1	1.60 BSC			0.063 BSC		
e	0.65 BSC			0.026 BSC		
e1	1.95 BSC			0.077 BSC		
L	0.30	0.45	0.60	0.012	0.018	0.024
L1	0.60 REF			0.024 REF		
L2	0.25 BSC			0.010 BSC		
R	0.10	—	—	0.004	—	—
R1	0.10	—	0.25	0.004	—	0.010
θ	0°	4°	8°	0°	4°	8°
θ1	4°	10°	12°	4°	10°	12°
N	8			8		

Solved by Sipex	SIPEX CORPORATION
	8 PIN TSOT PACKAGE OUTLINE
Packaging Approval:	Drawing No: 8−PIN TSOT
By: JL / Date: 09/13/06	Revision: B / Sheet: 1 OF 1

ORDERING INFORMATION

Model	Temperature Range	Package Type
SP6336EK1-L-X-X-X	-40°C to +85°C	Lead Free 8-Pin TSOT
SP6336EK1-L-X-X-X/TR	-40°C to +85°C	Lead Free 8-Pin TSOT
SP6337EK1-L-X-X-X	-40°C to +85°C	Lead Free 8-Pin TSOT
SP6337EK1-L-X-X-X/TR	-40°C to +85°C	Lead Free 8-Pin TSOT
SP6338EK1-L-X-X-X	-40°C to +85°C	Lead Free 8-Pin TSOT
SP6338EK1-L-X-X-X/TR	-40°C to +85°C	Lead Free 8-Pin TSOT

Available in lead free packaging only. /TR = Tape and Reel.

Pack quantity 2,500 forTSOT-8

Contact Factory for availability of particular voltage threshold and reset timeout options. Note that the Ordering Information denoting those options corresponds to the Part Naming Nomenclature shown on the previous page.

Ordering example: SP6336EK1-L-W-G-C/TR == W -- 2.925V for Voltage Threshold 1; G -- 1.575V for Voltage Threshold 2; and C -- 200ms reset timeout.

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